High-Level Synthesis Newsletter

No. 2, 30 June 2021

Dear All,

Using HLS design flow to describe logic circuits and accelerators has been growing recently. Several companies and universities have proposed their own solutions and tools. You can see a shortlist of companies providing HLS tools on the last page of this newsletter.

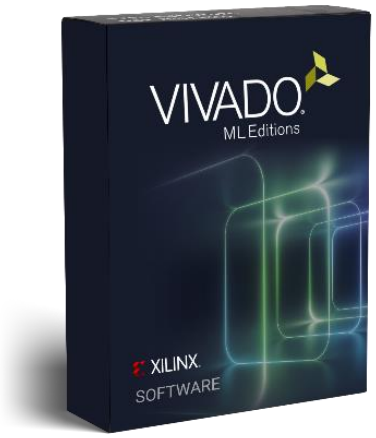
Although the underlying concepts and techniques are almost the same, they use different notations to describe and add optimisation techniques to the underlying design description in C/C++ or SystemC. Therefore, throughout the course, try to learn the HLS techniques as well as the notations and how to describe the techniques in Vitis-HLS.

Most of the HLS techniques can be used in both logic circuit, and accelerator design flows. By now, you have learned some basic HLS representation techniques to describe logic circuits. There is at least one more course in the series focusing on optimisation techniques. The main goal of the third part is to describe a few AI Algorithms using the HLS for logic circuit design flow.

But function acceleration in HLS is a very hot topic that you should learn as soon as possible. Therefore, the next course would be on this subject and will be available by the end of the next week. You can find more details about the course on Page 3.

Mohammad Hosseinabady, PhD

New Release of Vivado



Xilinx has introduced Vivado® ML Editions recently. One of the new features in these editions is supporting the machine-learning (ML) optimisation algorithms. We can use the new versions in our course almost without any problem, as it contains all the available features in the previous releases.

Note that there are two editions of Vivado ML: Standard Edition and Enterprise Edition. The standard edition is free and limited in supporting high-end FPGAs. The Enterprise edition requires a proper license to enable its advanced feature for high-end FPGAs.

The standard edition is enough for our courses.

During the installation, please select Vivado, as shown in Fig. 1. Then select the Vivado ML Standard edition (see Fig. 2). Note that you can also select the Vitis product if you want to, for any reason. The Vitis version also installs Vivado and Vitis-HLS that we use throughout the course.

Fig. 001

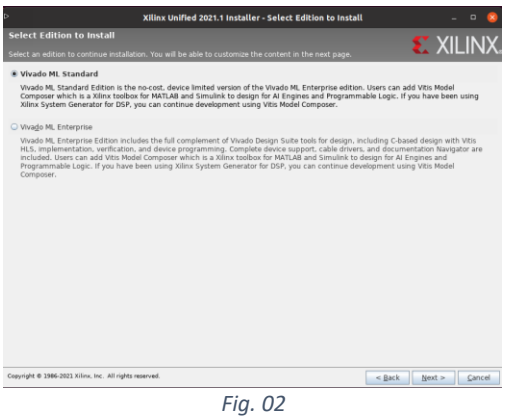


Fig. 02

New Courses

The first course on HLS for function acceleration is going to be ready in the next week. This course explains the basic concepts of HLS techniques to accelerate a complex application on Zynq based embedded systems. The course topics are designed such that we can accelerate the Support Vector Machine, one of the most successful machine-learning tools for classification and regression analysis.

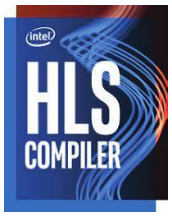
The course uses several examples to explain the HLS concepts and techniques provided by the Xilinx Vitis unified software platform. All examples and designs can be run on Zynq SoC and Zynq UltraScale+ MPSoC. The default FPGA boards considered in the course are Zybo Z7-20 and Ultra96v2. But, if somebody does not have access to an actual FPGA, he or she can still follow the course as all examples will be run in software and hardware Linux-based emulators, as well as the actual FPGA.

This is the list of the main topics that will be explained throughout the new course

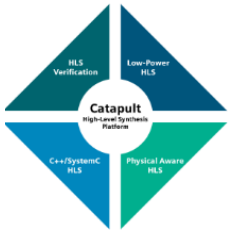
1- Vitis Unified Software Platform
2- Zynq SoC and Zynq MPSoC
3- OpenCL in Vitis
4- Kernel and host OpenCL programs in Vitis
5- Image thresholding example
6- Matrix-vector multiplication on FPGA
7- Sparse matrices
8- Suport Vector Machine (SVM)

HLS in Industry

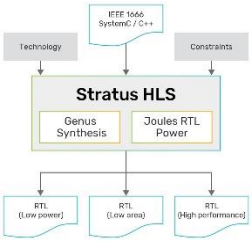
Xilinx is not the only company that provides HLS tools and design flow. Other companies such as Intel, Cadence and Siemens and Synopsys also have their own HLS tools and approaches.



Intel has an HLS Compiler, which is part of the Intel Quartus Prime Design Software. The tool takes the design description in untimed C++ (very similar to Vitis-HLS) and generates the corresponding register transfer level (RTL) code that is optimised for Intel FPGAs.



Siemens own the Catapult High-Level Synthesis (HLS) & High-Level Verification toolset. “Catapult Synthesis solutions from Siemens deliver C++ and SystemC language support, FPGA and ASIC independence, ASIC power estimation and optimisation plus the latest in the Physically aware multi-VT area and performance optimisation.”



Cadence introduces the Stratus High-Level Synthesis toolset. The toolset accepts SystemC and C/C++ as the design description languages and generates the corresponding RTL code. It features the Genus™ Synthesis and Joules™ RTL Power engines that provide logic designs with power, performance, and area equal to or better than those achieved with hand-written RTL.

Synopsys has introduced the Synphony HLS solution to deliver up to 10X higher design productivity than traditional RTL flows for communications and multimedia applications. Their technology integrates M-language and model-based synthesis.