Appendix C: 6502 Opcodes

Opcode	Mnemonic	Addressing Mode	Cycles
79	ADC	aaaa,y	4+
7D	ADC	aaaa,x	4+
69	ADC	#aa	2
61	ADC	(aa,x)	6
71	ADC	(aa),y	5+
75	ADC	aa,x	4
65	ADC	aa	3
6D	ADC	aaaa	4
0B	ANC*	#aa	2
2B	ANC*	#aa	2
39	AND	aaaa,y	4+
3D	AND	aaaa,x	4+
29	AND	#aa	2
21	AND	(aa,x)	6
31	AND	(aa),y	5+
35	AND	aa,x	4
25	AND	aa	3
2D	AND	aaaa	4
8B	ANE*	#aa	0
6B	ARR*	#aa	2
0A	ASL		2
1E	ASL	aaaa,x	7
16	ASL	aa,x	6
06	ASL	aa	5
0E	ASL	aaaa	6
4B	ASR*	#aa	2
90	BCC	branch if carry clear	2++
B0	BCS	branch if carry set	2++
F0	BEQ	branch if equal	2++
24	BIT	aa	3
2C	BIT	aaaa	4
30	BMI	branch if negative	2++

Opcode	Mnemonic	Addressing Mode	Cycles
D0	BNE	branch if not equal	2++
10	BPL	branch if positive	2++
00	BRK		7
50	BVC	branch if overflow clear	2++
70	BVS	branch if overflow set	2++
18	CLC		2
D8	CLD		2
58	CLI		2
B8	CLV		2
D9	CMP	aaaa,y	4+
DD	CMP	aaaa,x	4+
C9	CMP	#aa	2
C1	CMP	(aa,x)	6
D1	CMP	(aa),y	5+
D5	CMP	aa,x	4
C5	CMP	aa	3
CD	CMP	aaaa	4
E0	CPX	#aa	2
E4	CPX	aa	3
EC	CPX	aaaa	4
C0	CPY	#aa	2
C4	CPY	aa	3
CC	CPY	aaaa	4
C3	DCP*	(aa,x)	8+
D3	DCP*	(aa),y	8+
DB	DCP*	aaaa,y	7+
DF	DCP*	aaaa,x	7+
D7	DCP*	aa,x	6+
C7	DCP*	aa	5
CF	DCP*	aaaa	6
DE	DEC	aaaa,x	7
D6	DEC	aa,x	6
C6	DEC	aa	5
CE	DEC	aaaa	3
CA	DEX		2
88	DEY		2

Opcode	Mnemonic	Addressing Mode	Cycles
59	EOR	aaaa,y	4+
5D	EOR	aaaa,x	4+
49	EOR	#aa	2
41	EOR	(aa,x)	6
51	EOR	(aa),y	5+
55	EOR	aa,x	4
45	EOR	aa	3
4D	EOR	aaaa	4
FE	INC	aaaa,x	7
F6	INC	aa,x	6
E6	INC	aa	5
EE	INC	aaaa	6
E8	INX		2
C8	INY		2
E3	ISB*	(aa,x)	8+
F3	ISB*	(aa),y	8+
FB	ISB*	aaaa,y	7+
FF	ISB*	aaaa,x	7+
F7	ISB*	aa,x	6+
E7	ISB*	aa	5
EF	ISB*	aaaa	6
4C	JMP	aaaa	3
6C	JMP	(aaaa)	5
20	JSR	aaaa	6
BB	LAS*	aaaa,y	0
BF	LAX*	aaaa,y	4+
A3	LAX*	(aa,x)	6+
B3	LAX*	(aa),y	5+
B7	LAX*	aa,y	4+
A7	LAX*	aa	3
AF	LAX*	aaaa	4
B9	LDA	aaaa,y	4+
BD	LDA	aaaa,x	4+
A9	LDA	#aa	2
A1	LDA	(aa,x)	6
B1	LDA	(aa),y	5+

Opcode	Mnemonic	Addressing Mode	Cycles
B5	LDA	aa,x	4
A5	LDA	aa	3
AD	LDA	aaaa	4
BE	LDX	aaaa,y	4+
A2	LDX	#aa	2
B6	LDX	aa,y	4
A6	LDX	aa	3
AE	LDX	aaaa	4
BC	LDY	aaaa,x	4+
A0	LDY	#aa	2
B4	LDY	aa,x	4
A4	LDY	aa	3
AC	LDY	aaaa	4
4A	LSR		2
5E	LSR	aaaa,x	7
56	LSR	aa,x	6
46	LSR	aa	5
4E	LSR	aaaa	6
AB	LXA*	#aa	0
EA	NOP		2
1C	NOP*	aaaa,x	4+
3C	NOP*	aaaa,x	4+
5C	NOP*	aaaa,x	4+
7C	NOP*	aaaa,x	4+
DC	NOP*	aaaa,x	4+
FC	NOP*	aaaa,x	4+
80	NOP*	#aa	0
82	NOP*	#aa	0
89	NOP*	#aa	0
C2	NOP*	#aa	0
E2	NOP*	#aa	0
1A	NOP*	-	0
3A	NOP*	-	0
5A	NOP*	-	0
7A	NOP*	-	0
DA	NOP*	-	0

Opcode	Mnemonic	Addressing Mode	Cycles
FA	NOP*	-	0
14	NOP*	aa,x	4
34	NOP*	aa,x	4
54	NOP*	aa,x	4
74	NOP*	aa,x	4
D4	NOP*	aa,x	4
F4	NOP*	aa,x	4
04	NOP*	aa	3
44	NOP*	aa	3
64	NOP*	aa	3
0C	NOP*	aaaa	4
19	ORA	aaaa,y	4+
1D	ORA	aaaa,x	4+
09	ORA	#aa	2
01	ORA	(aa,x)	6
11	ORA	(aa),y	5+
15	ORA	aa,x	4
05	ORA	aa	3
0D	ORA	aaaa	4
48	PHA		3
08	PHP		3
68	PLA		4
28	PLP		4
23	RLA*	(aa,x)	8+
33	RLA*	(aa),y	8+
3B	RLA*	aaaa,y	7+
3F	RLA*	aaaa,x	7+
37	RLA*	aa,x	6+
27	RLA*	aa	5
2F	RLA*	aaaa	6
2A	ROL		2
3E	ROL	aaaa,x	7
36	ROL	aa,x	6
26	ROL	aa	5
2E	ROL	aaaa	6
6A	ROR		2

Opcode	Mnemonic	Addressing Mode	Cycles
7E	ROR	aaaa,x	7
76	ROR	aa,x	6
66	ROR	aa	5
6E	ROR	aaaa	6
63	RRA*	(aa,x)	8+
73	RRA*	(aa),y	8+
7B	RRA*	aaaa,y	7+
7F	RRA*	aaaa,x	7+
77	RRA*	aa,x	6+
67	RRA*	aa	5
6F	RRA*	aaaa	6
40	RTI		6
60	RTS		6
83	SAX*	(aa,x)	6+
97	SAX*	aa,y	4+
87	SAX*	aa	3
8F	SAX*	aaaa	4
F9	SBC	aaaa,y	4+
FD	SBC	aaaa,x	4+
E9	SBC	#aa	2
EB	SBC*	#aa	0
E1	SBC	(aa,x)	6
F1	SBC	(aa),y	5+
F5	SBC	aa,x	4
E5	SBC	aa	3
ED	SBC	aaaa	4
CB	SBX*	#aa	2
38	SEC		2
F8	SED		2
78	SEI		2
93	SHA*	(aa),y	0
9F	SHA*	aaaa,y	0
9B	SHS*	aaaa,y	0
9E	SHX*	aaaa,y	0
9C	SHY*	aaaa,x	0
03	SLO*	(aa,x)	8+

Opcode	Mnemonic	Addressing Mode	Cycles
13	SLO*	(aa),y	8+
1B	SLO*	aaaa,y	7+
1F	SLO*	aaaa,x	7+
17	SLO*	aa,x	6+
07	SLO*	aa	5
0F	SLO*	aaaa	6
43	SRE*	(aa,x)	8+
53	SRE*	(aa),y	8+
5B	SRE*	aaaa,y	7+
5F	SRE*	aaaa,x	7+
57	SRE*	aa,x	6+
47	SRE*	aa	5
4F	SRE*	aaaa	6
81	STA	(aa,x)	6
91	STA	(aa),y	6
95	STA	aa,x	4
85	STA	aa	3
99	STA	aaaa,y	5
9D	STA	aaaa,x	5
8D	STA	aaaa	4
96	STX	aa,y	4
86	STX	aa	3
8E	STX	aaaa	4
94	STY	aa,x	4
84	STY	aa	3
8C	STY	aaaa	4
AA	TAX		2
A8	TAY		2
BA	TSX		2
8A	TXA		2
9A	TXS		2
98	TYA		2

Appendix D: 6502 Instruction Flags

Summary of Documented 6502 Instructions

Mnemonic	Flags Affected	Expression
ADC	NZCV	A += opr
AND	NZ	A &= opr
ASL	NZC	opr «= 1
BCC	-	branch if C==0
BCS	-	branch if C==1
BEQ	-	branch if Z==0
BIT	NZV	(A & opr); V = bit 6
BMI	-	branch if N==1
BNE	-	branch if Z==1
BRK	B	–
BVC	-	branch if V==0
BVS	-	branch if V==1
CLC	C	C = 0
CLD	D	D = 0
CLV	V	V = 0
CMP	NZC	(A - opr)
CPX	NZC	(X - opr)
CPY	NZC	(Y - opr)
DEC	NZ	opr–
DEX	NZ	X–
DEY	NZ	Y–
EOR	NZ	A ^= opr
INC	NZ	opr++
INX	NZ	X++
INY	NZ	Y++
JMP	-	PC = opr
JSR	-	push PC-1; PC = opr
LDA	NZ	A = opr
LDX	NZ	X = opr
LDY	NZ	Y = opr
LSR	NZC	A »= 1

Summary of Documented 6502 Instructions

Mnemonic	Flags Affected	Expression
NOP	-	–
PHA	-	[S–] = A
PHP	-	[S–] = P
PLA	NZ	A = [++S]
PLP	all	P = [++S]
ORA	NZ	A |= opr
ROL	NZC	A = (A«1) | C
ROR	NZC	A = (A»1) | (C*128)
SBC	NZCV	A -= opr
SEC	C	C = 1
SED	D	D = 1
STA	-	opr = A
STX	-	opr = X
STY	-	opr = Y
TAX	NZ	X = A
TAY	NZ	Y = A
TXA	NZ	A = X
TYA	NZ	A = Y
TSX	NZ	X = S
TXS	NZ	S = X

N = Negative (Sign)
Z = Zero
C = Carry
V = Overflow
D = Decimal

Summary of Illegal 6502 Instructions

Mnemonic	Flags Affected	Expression
ANC	NZC	A &= #opr
ASR	NZC	A = (A & #opr) » 1
ARR	NZCV	A = (A & #opr) » 1
DCP	NZC	(A - opr–)
ISC	NZCV	A -= opr++
LAS	NZ	A=X=S = opr & S
LAX	NZ	A=X = opr
RLA	NZC	A = (rol A) & opr
RRA	NZCV	A = (ror A) + opr
SBX	NZC	X = (A & X) - #opr
SLO	NZC	A = (A «= 1) | opr
SRE	NZC	A = (A »= 1) ôpr

N = Negative (Sign)
Z = Zero
C = Carry
V = Overflow