COS10004 - Computer Systems
Lab week 2

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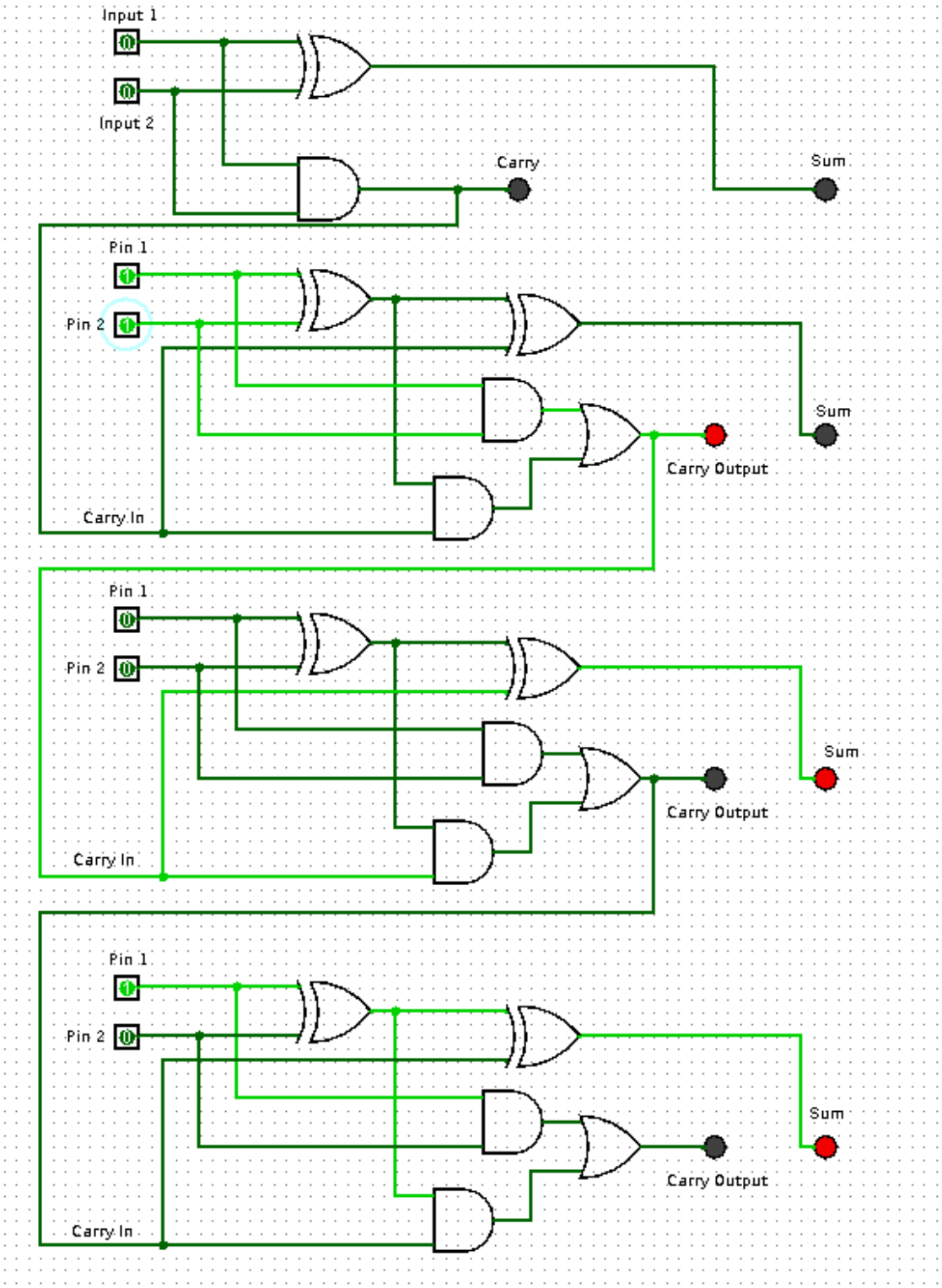
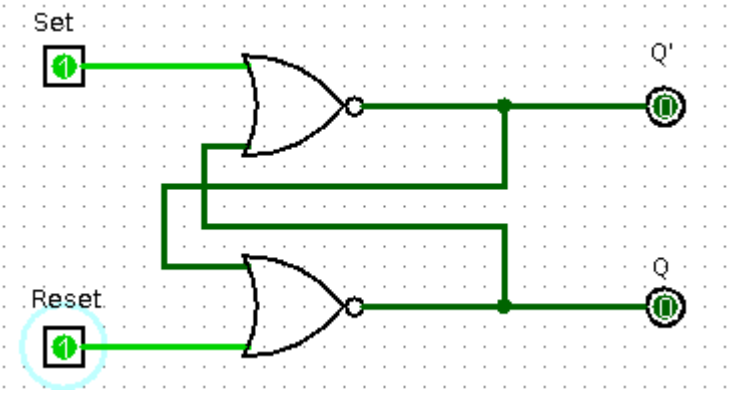
Circuit 1



Input A (1)	Input B (2)	Output
0101	0000	0101
0101	0001	0110
0101	0010	0111
0101	0011	1000
0101	0100	1001
0101	0101	1010
0101	0110	1011
0101	0111	1100
0101	1000	1101
0101	1001	1110
0101	1010	1111
0101	1011	0000
0101	1100	0001
0101	1101	0010
0101	1110	0011
0101	1111	0100

Circuit 2

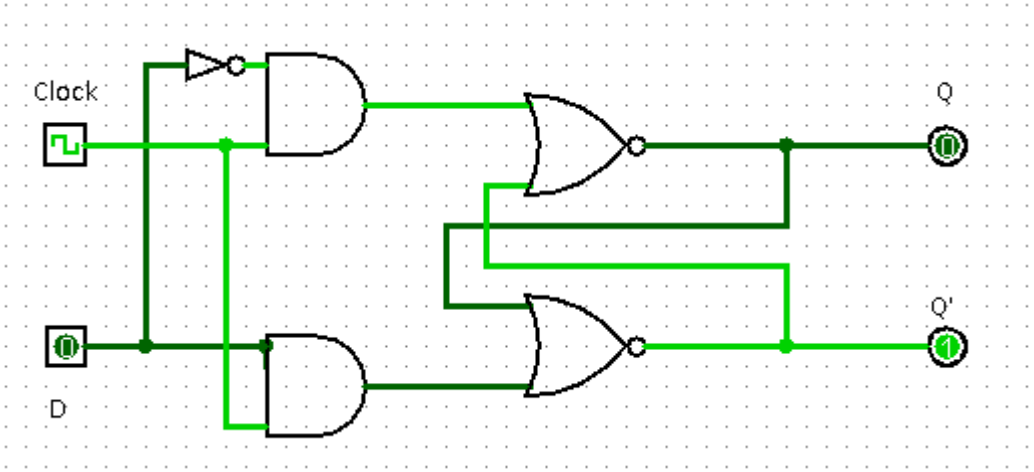


Set	Reset	Q	Q’
1	0	1	0
1	1	0	0
0	1	0	1
1	1	0	0

Q11. When one input is 1, Q or Q’ will change to 1: If Set = 1, Q = 1 and if Reset = 1, Q’ = 1. This is useful for digital circuit design because it helps us to save the value in 1-bit storage which holds the value without requiring a stable input signal.

Q12. Due to the effect of NOR gates, when both two inputs are 1, both two outputs try to reach 0. Because those outputs should complement each other, this circumstance violates the rule.

Circuit 3



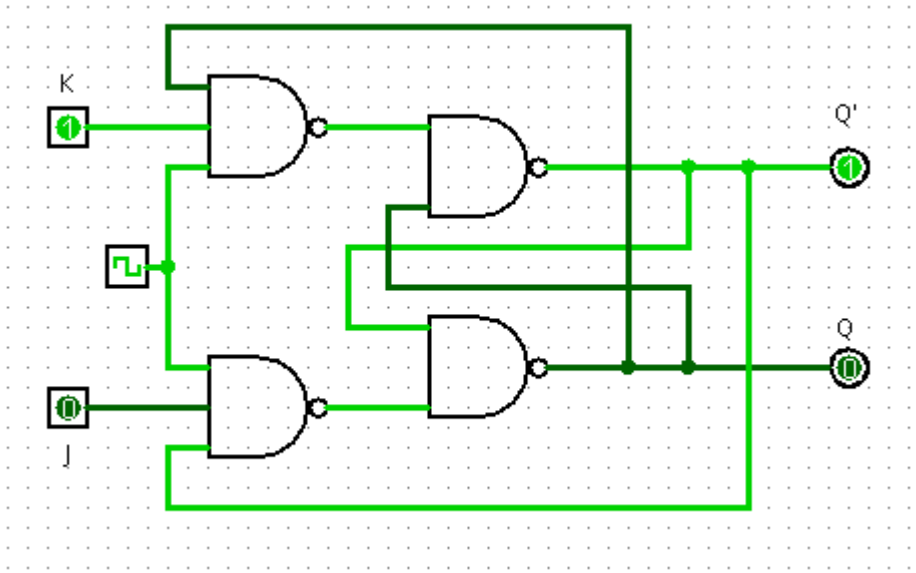
Clock	Input	Q	Q’
0	0	0	0
0	1	0	0
1	1	1	0
1	0	0	1

Q15. The D Flip-flop has a single data input and is split into 2 inputs. Those inputs are always opposite due to the effect of the NOT gate. When the clock is on, the output Q will be the opposite of the input D, and Q' is the same as the input D.

Q16. The clock is used to synchronize the signal of the input D.

Q17. The D Flip-flop is preferred over the RS Flip-flop in case we just want to have one input and stable output thanks to the synchronization effect from the clock.

Circuit 4



J	K	Q (when clocked)	Q'(when clocked)
0	0	Unchanged	Unchanged
1	0	1	0
0	1	0	1
1	1	Toggle	Toggle

Q20. To let the JK Flip-flop behaves like a D Flip-flop, we can drive the input J and K with the D input and its negation.

Q21. When both J input and K input are 1, JK Flip-flop behaves like a T Flip-flop or a toggle.