Ch8 Sequential Logic Design Practices

Main contents:

（1）Timing diagram时序图

（2）Registers寄存器

（3）Counters计数器（重点）

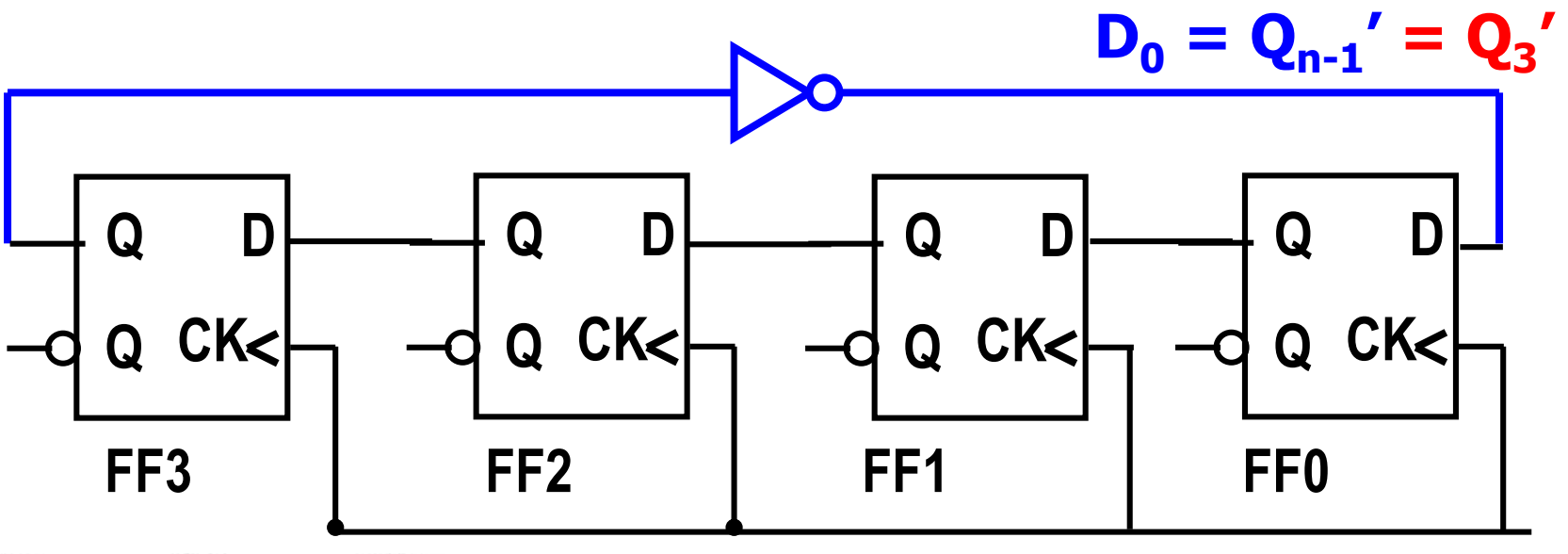
以74x163为代表的电路分析与应用，包含：电路功能分析；任意模m计数器设计；序列发生器；控制各种不同器件

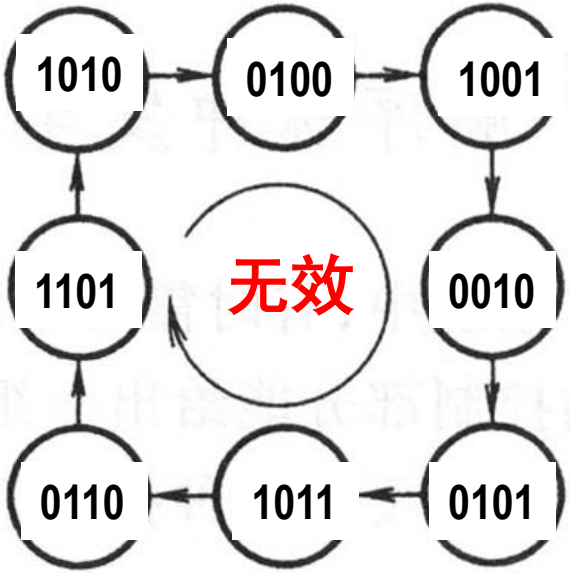
（4）Shift registers移位寄存器（重点）

以74x194为代表的电路分析与应用，包含：

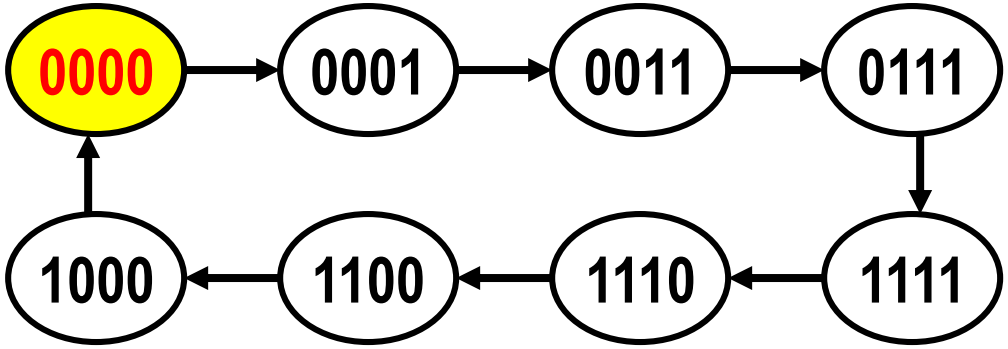
8.5.1 Shift-Register Structure
8.5.2 MSI Shift Registers
8.5.3 Shift-Register Counters
8.5.4 Ring Counters
8.5.5 Johnson Counters
8.5.6 Linear Feedback Shift-Register Counters(LFSR)

8.5.5 Johnson Counter/"Twisted ring" counter

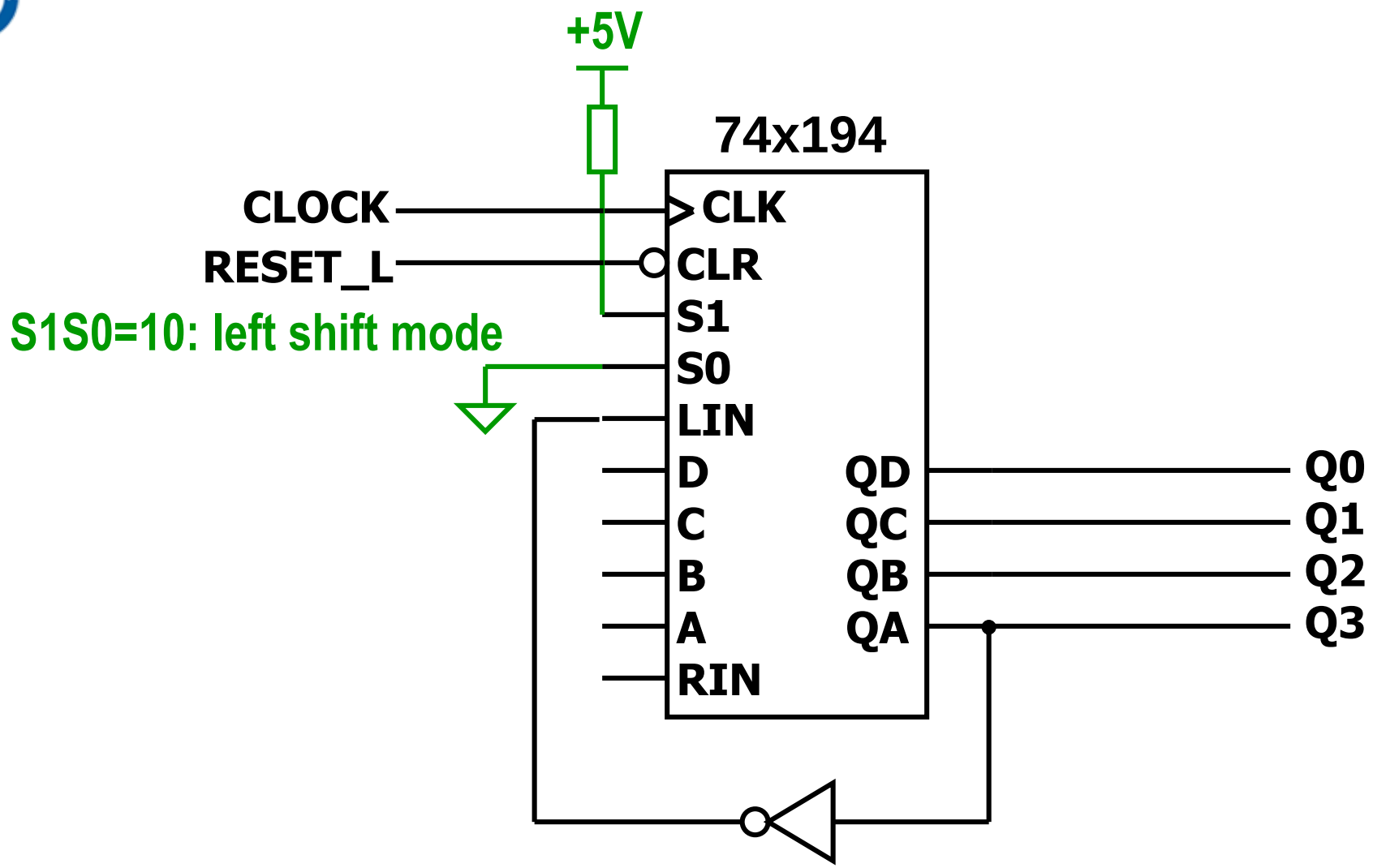




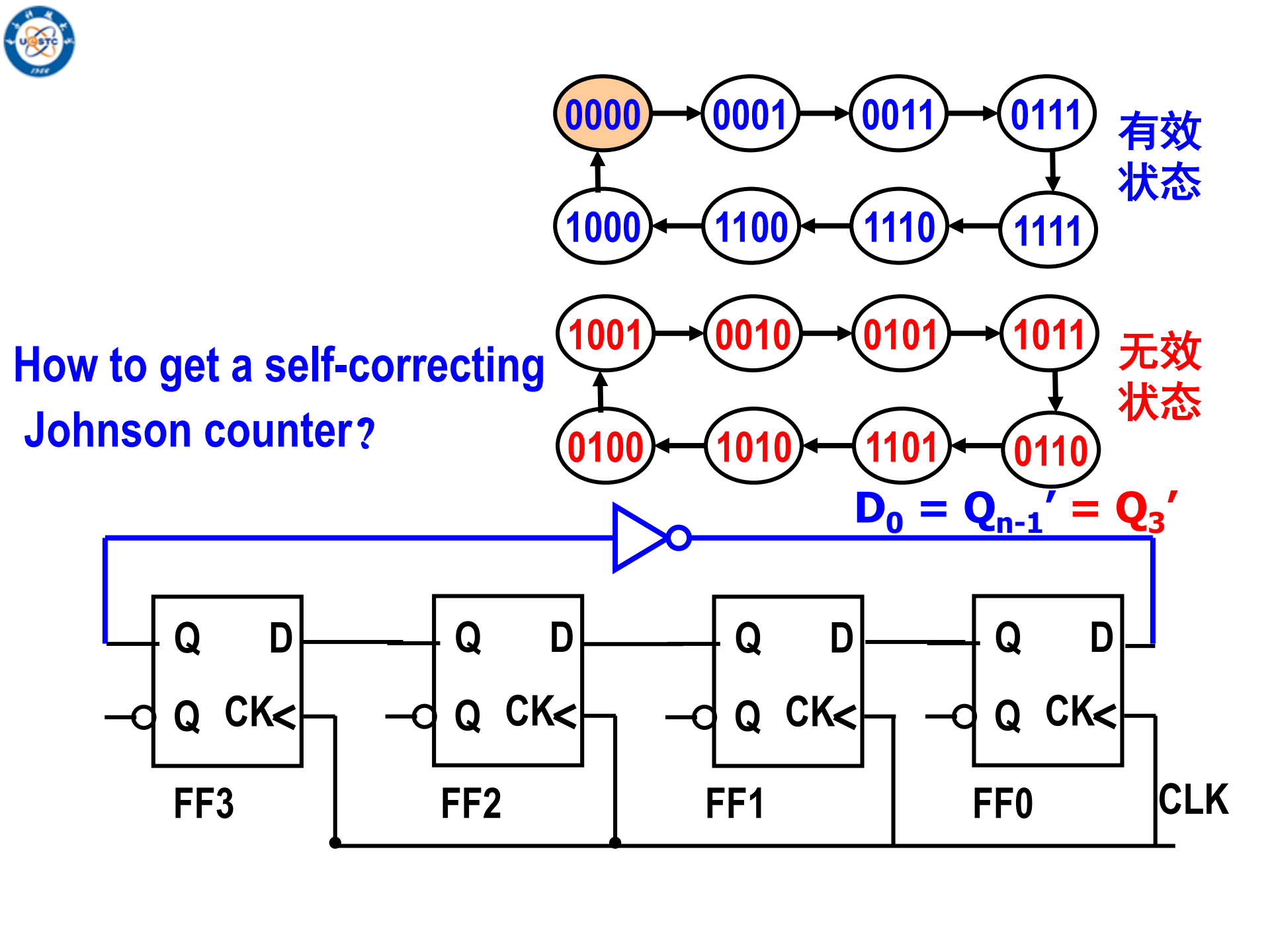
Assume initial state: 0000



有效的状态循环



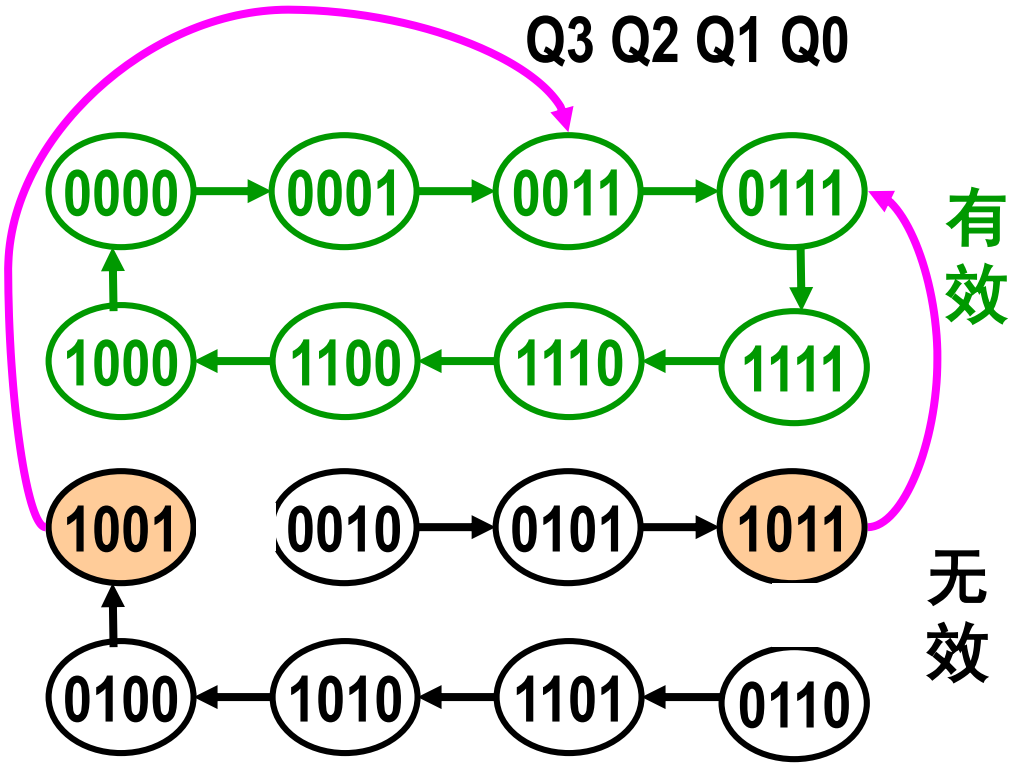
Johnson counter with 74x194

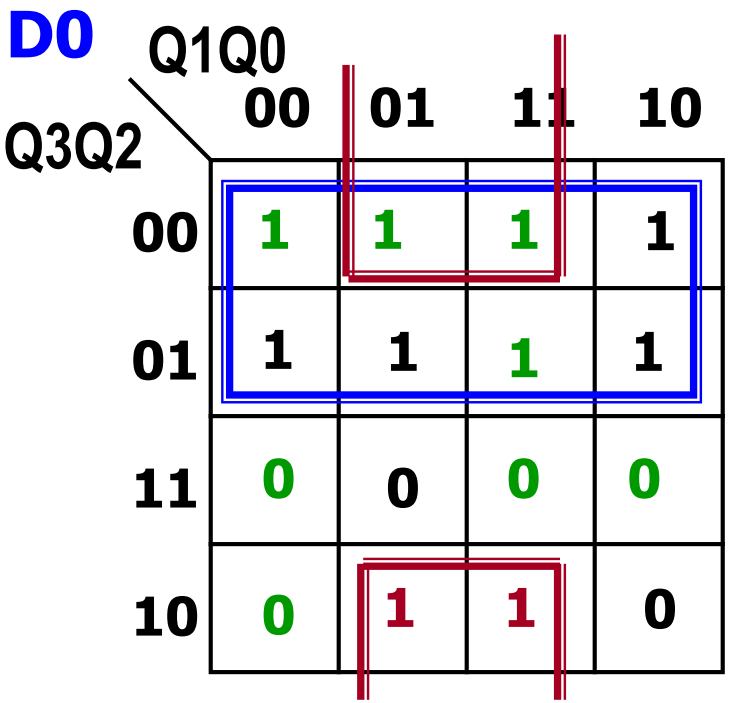

How to get a self-correcting Johnson counter?
0000
0001
0011
0111
1000
1100
1110
1111
有效状态
1001
0010
0101
1011
0100
1010
1101
0110
无效状态
$D_0 = Q_{n-1}' = Q_3'$
Q
D
Q
CK
FF3
FF2
FF1
FF0
CLK

Self-correcting design (1)

1、decide which state circle is normal circle相对性
确定有效的状态循环

2、process the abnormal state circle, let them get into normal circle
对无效状态进行处理，使其进入有效循环



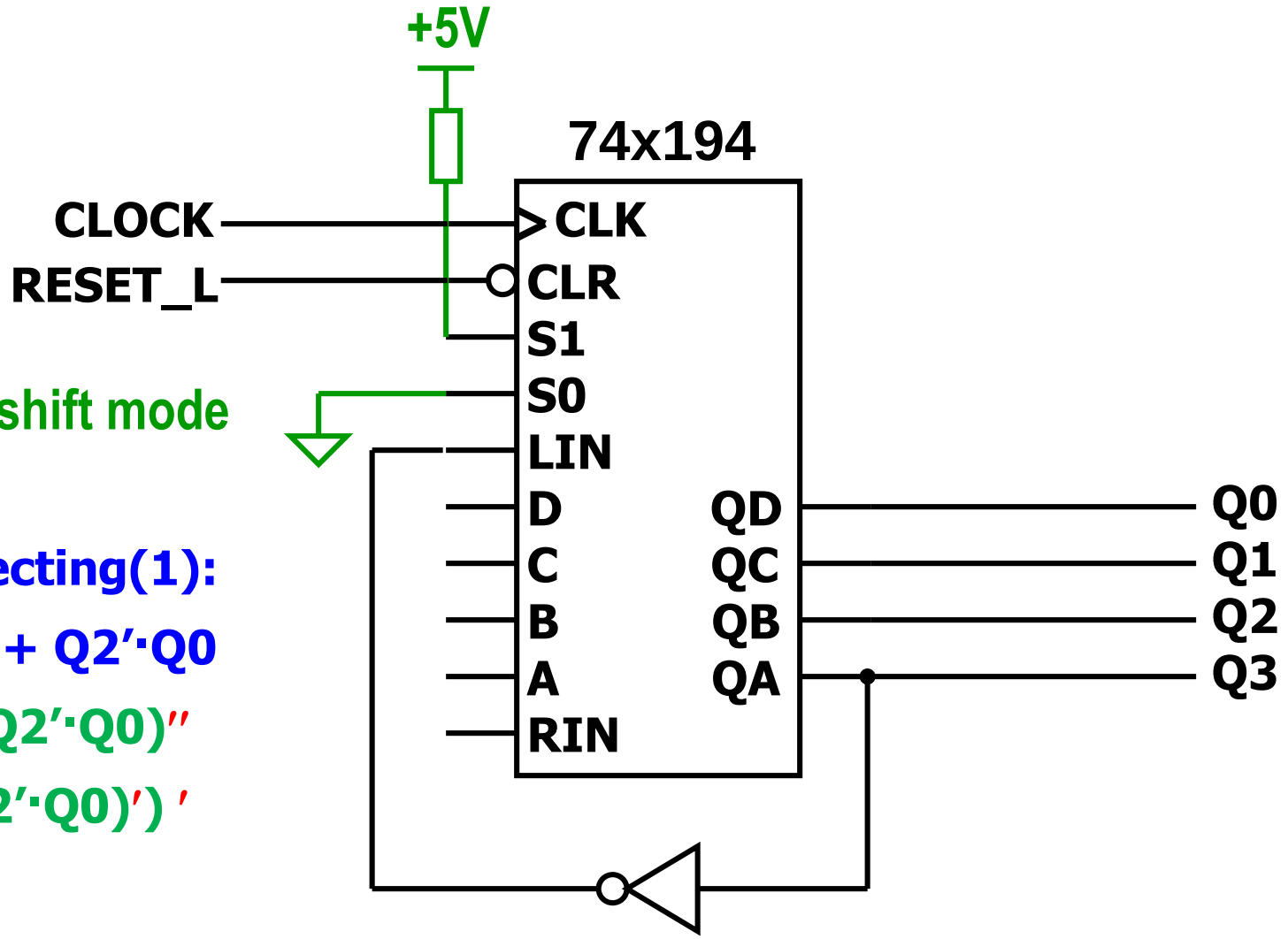


$$D0 = Q3' + Q2'\cdot Q0$$

8.5.5 Johnson Counter/"Twisted ring" counter

Self-correcting design (1)

扭环形计数器



S1S0:left shift mode

Self-correcting(1):

D0 = Q3′ + Q2′·Q0

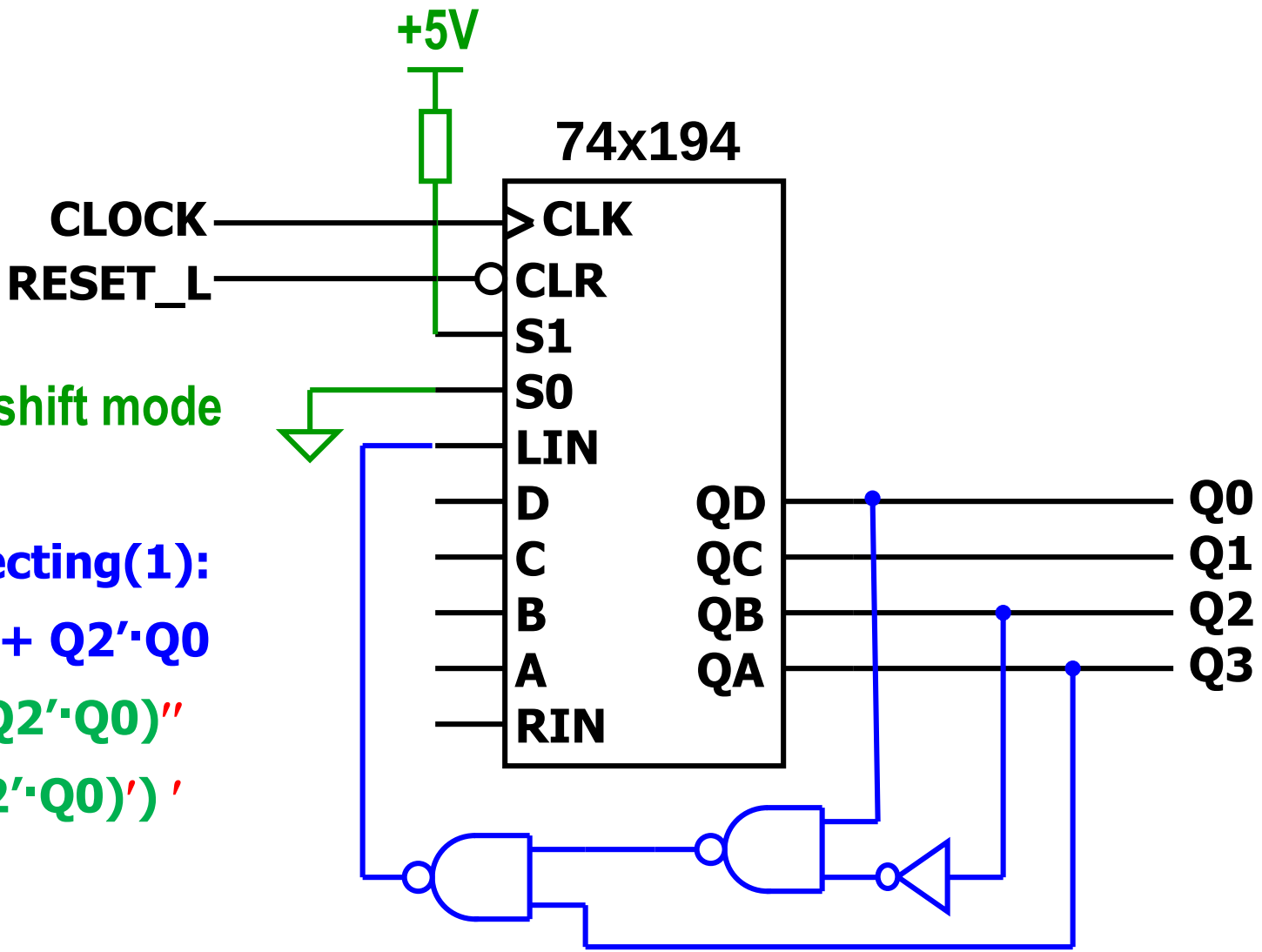
=(Q3′ + Q2′·Q0)″

=(Q3•(Q2′·Q0)′) ′

8.5.5 Johnson Counter/"Twisted ring" counter

Self-correcting design (1)

扭环形计数器



S1S0:left shift mode

Self-correcting(1):

D0 = Q3′ + Q2′·Q0

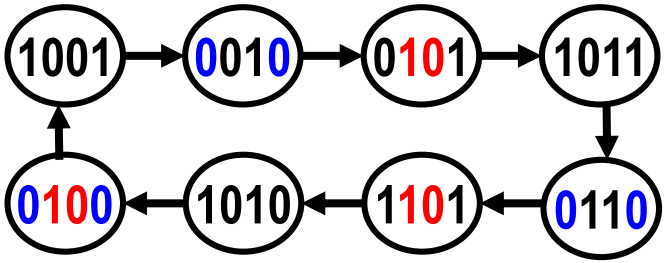
=(Q3′ + Q2′·Q0)″

=(Q3•(Q2′·Q0)′)′

8.5.5 Johnson Counter/"Twisted ring" counter

扭环形计数器

问题的提出：无效状态 X10X After some periods, it has 10XX, and next state is 0XX0, 如何进行校正？

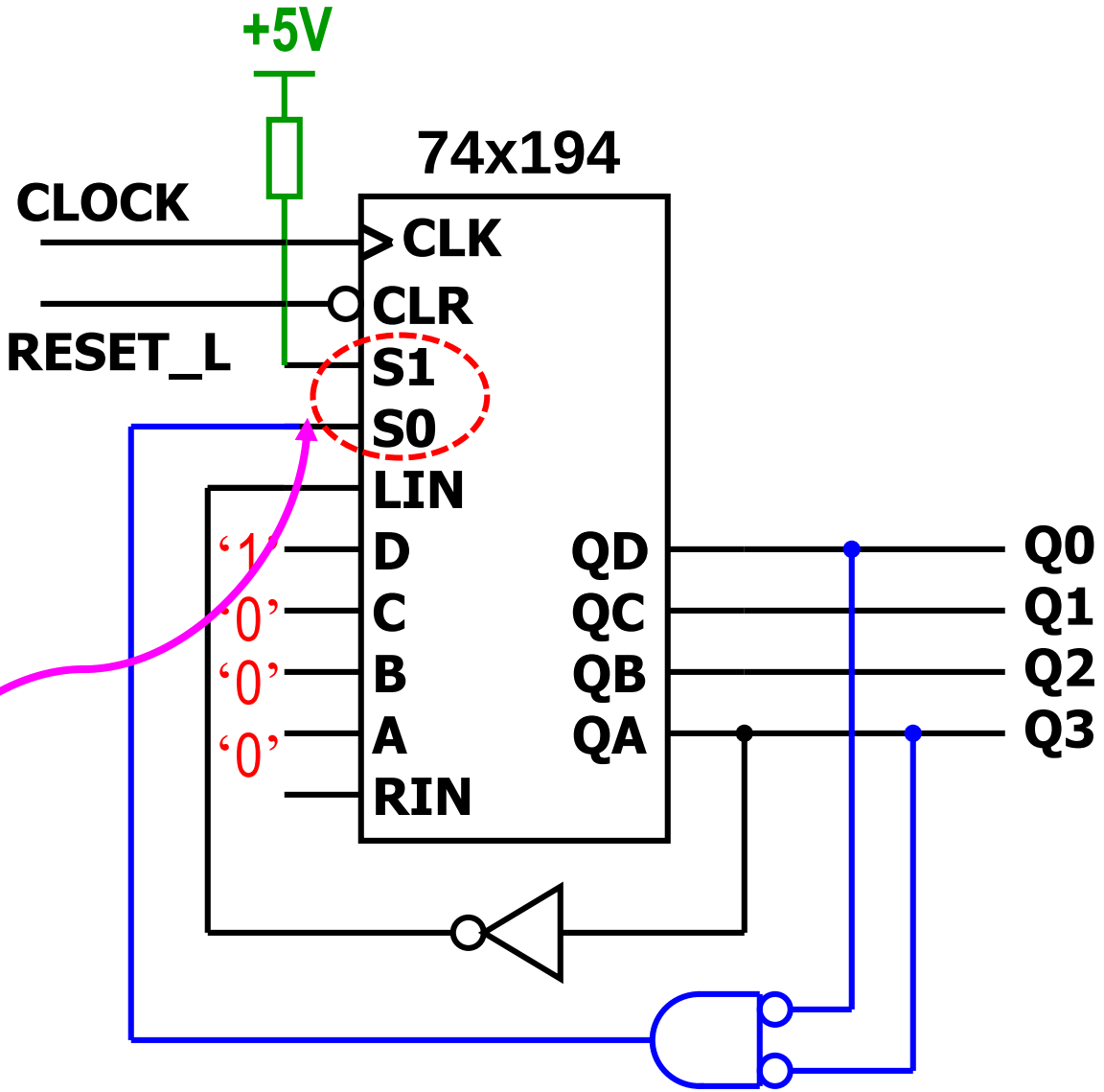


self-correcting (2):

When the outputs are 0XX0, let the next State is 0001

Load: 0001

S1=1,S0 = Q3'.Q0'



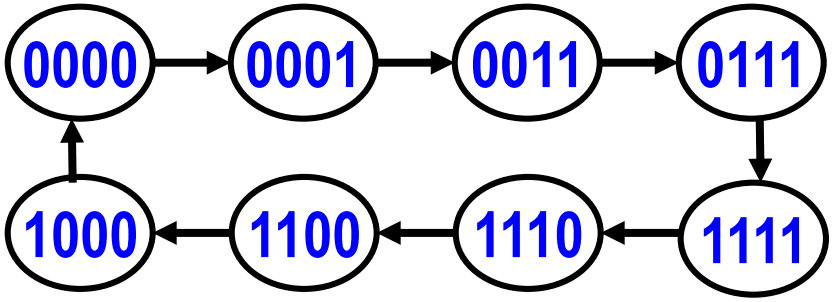
8.5.5 Johnson Counter/"Twisted ring" counter

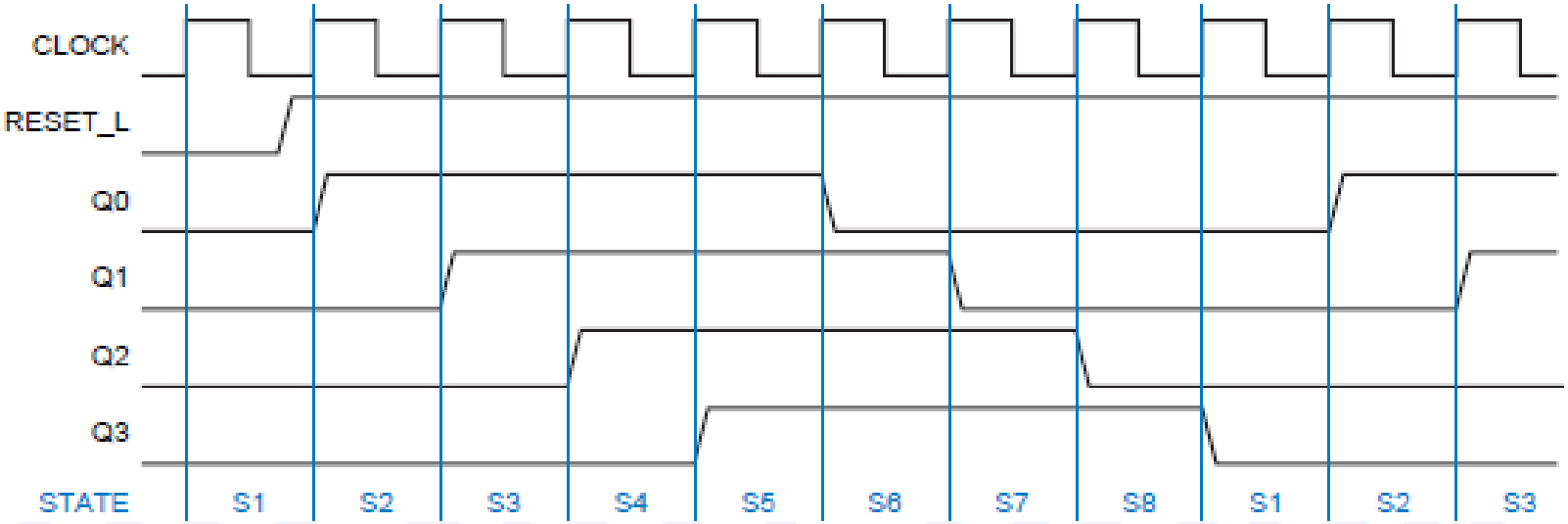
扭环形计数器

Conclusion:

n-bit Johnson counter: 2n normal states, 2^n-2n abnormal states

4-bit Johnson counter

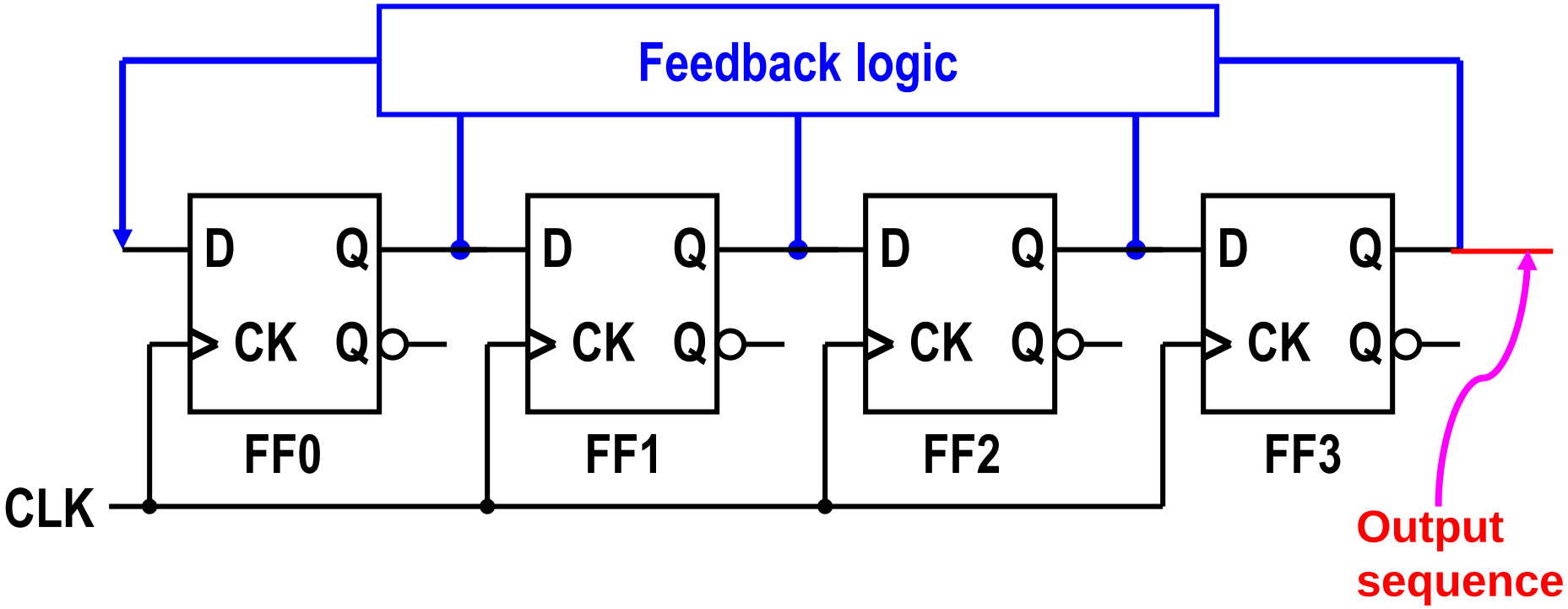




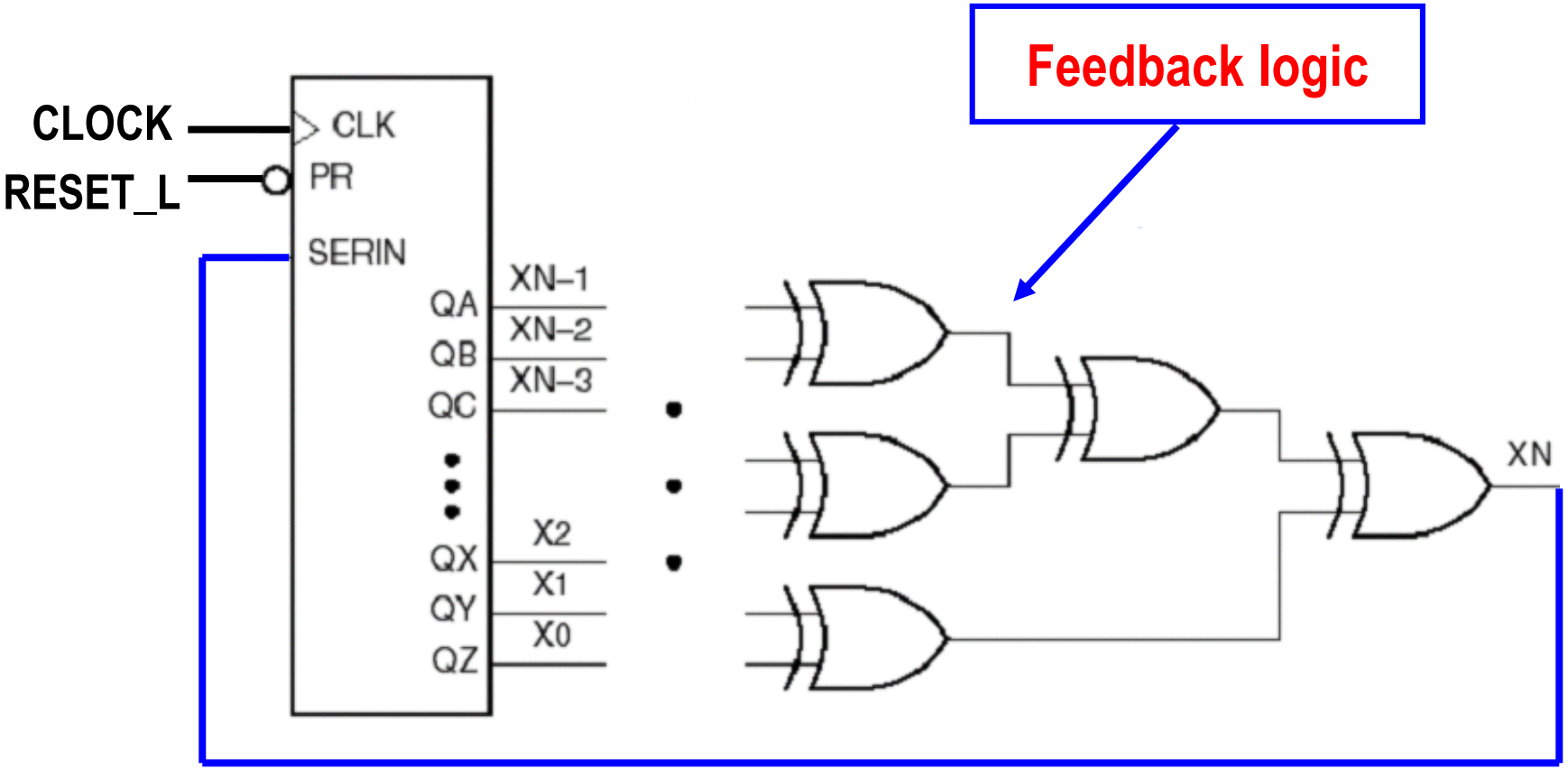
8.5.6 Linear Feedback Shift Register (LFSR) counters

n-bit LFSR: 2^n-1 states(有效)

——maximum- length sequence generator



LFSR counters的一般结构



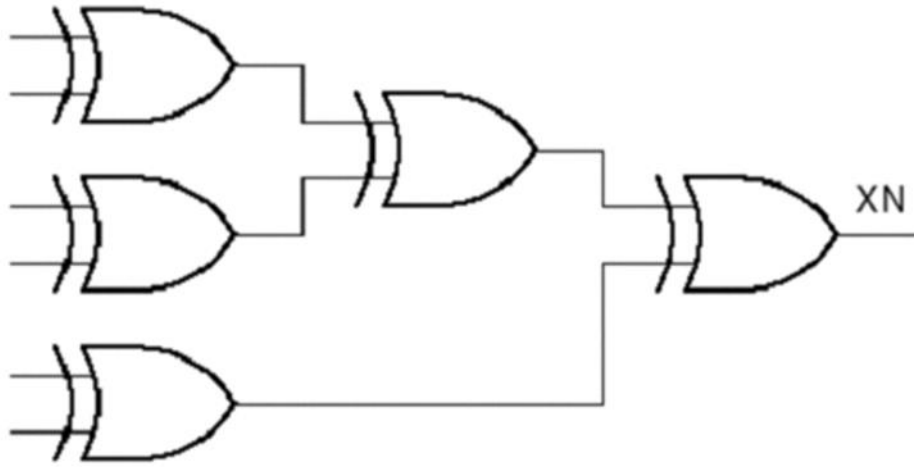
All 0 state, what is next state?

反馈方程

n	Feedback Equation
2	X2 = X1 ⊕ X0
3	X3 = X1 ⊕ X0
4	X4 = X1 ⊕ X0
5	X5 = X2 ⊕ X0
6	X6 = X1 ⊕ X0
7	X7 = X3 ⊕ X0
8	X8 = X4 ⊕ X3 ⊕ X2 ⊕ X0
12	X12 = X6 ⊕ X4 ⊕ X1 ⊕ X0
16	X16 = X5 ⊕ X4 ⊕ X3 ⊕ X0
20	X20 = X3 ⊕ X0
24	X24 = X7 ⊕ X2 ⊕ X1 ⊕ X0
28	X28 = X3 ⊕ X0
32	X32 = X22 ⊕ X2 ⊕ X1 ⊕ X0

The next state is still all 0

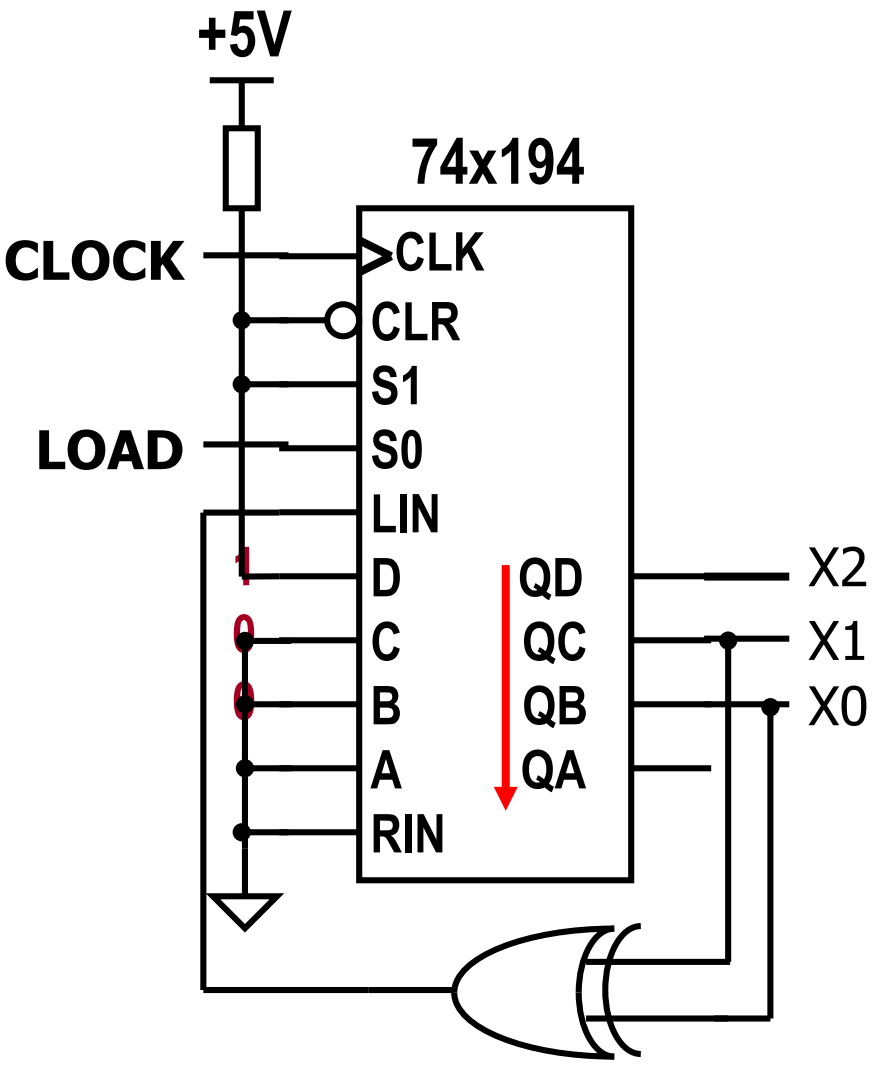
Odd-parity circuits奇校验电路



Thinking: LFSR counters如何自校正？

参见教材：P738-740(英文第4版)

Linear Feedback shift-register（LFSR）counters



Ex:以3位LFSR计数器为例

状态序列 (未校正序列)

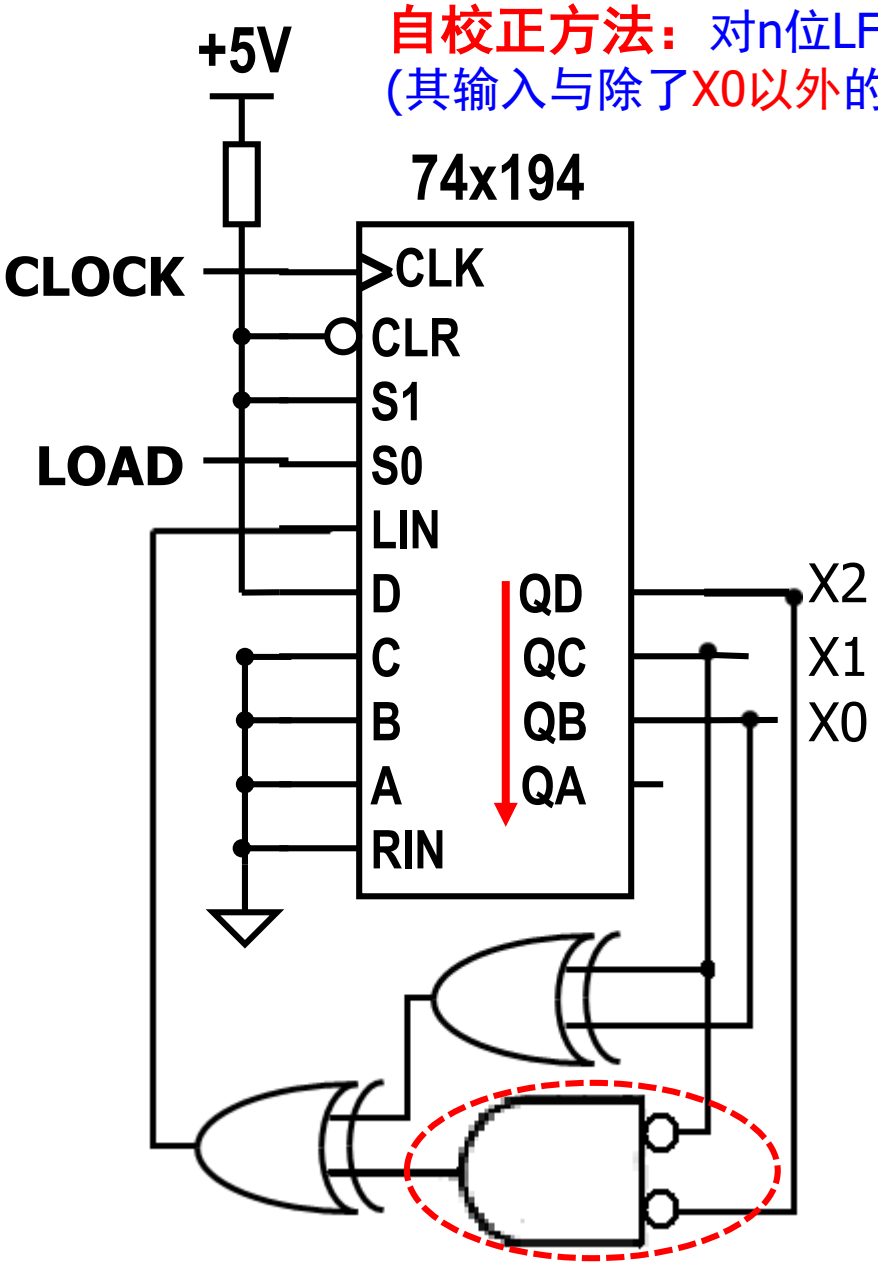
Original Sequence		
X2	*X1*	*X0*
1	0	0
0	1	0
1	0	1
1	1	0
1	1	1
0	1	1
0	0	1
1	0	0
.	.	.
.	.	.

如何加入000状态？

（即如何实现自校正？）

Linear Feedback shift-register（LFSR）counters

自校正方法：对n位LFSR计数器，外加1个XOR、1个n-1输入的NOR(其输入与除了X0以外的其他所有寄存器输出相连)即可



3位LFSR计数器

状态序列(自校正前后对比)

Original Sequence			Modified Sequence		
X2	X1	X0	X2	X1	X0
1	0	0	1	0	0
0	1	0	0	1	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1
0	1	1	0	1	1
0	0	1	0	0	1
1	0	0	0	0	0
.	.	.	1	0	0
.	.	.	.	.	.

Shift registers的其他应用(1)：Sequence generator

Example：generate 8-bit periodic sequence 000 101 11

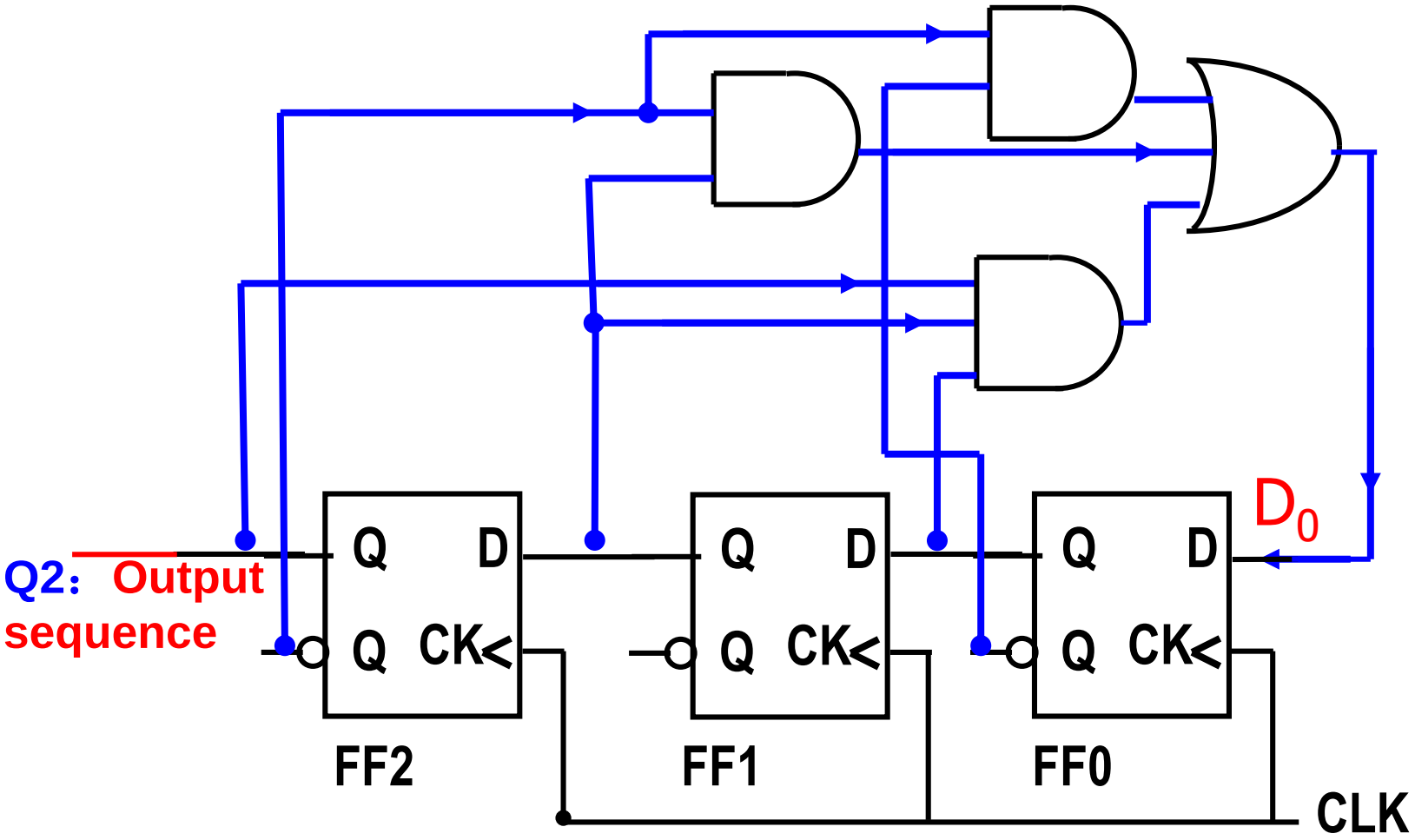
$Q_2Q_1Q_0$	D_0
0 0 0	1
0 0 1	0
0 1 0	1
1 0 1	1
0 1 1	1
1 1 1	0
1 1 0	0
1 0 0	0

刚好完全覆盖8种不同状态：000~111，
且Q2输出就为设计所需序列

反馈方程D_0

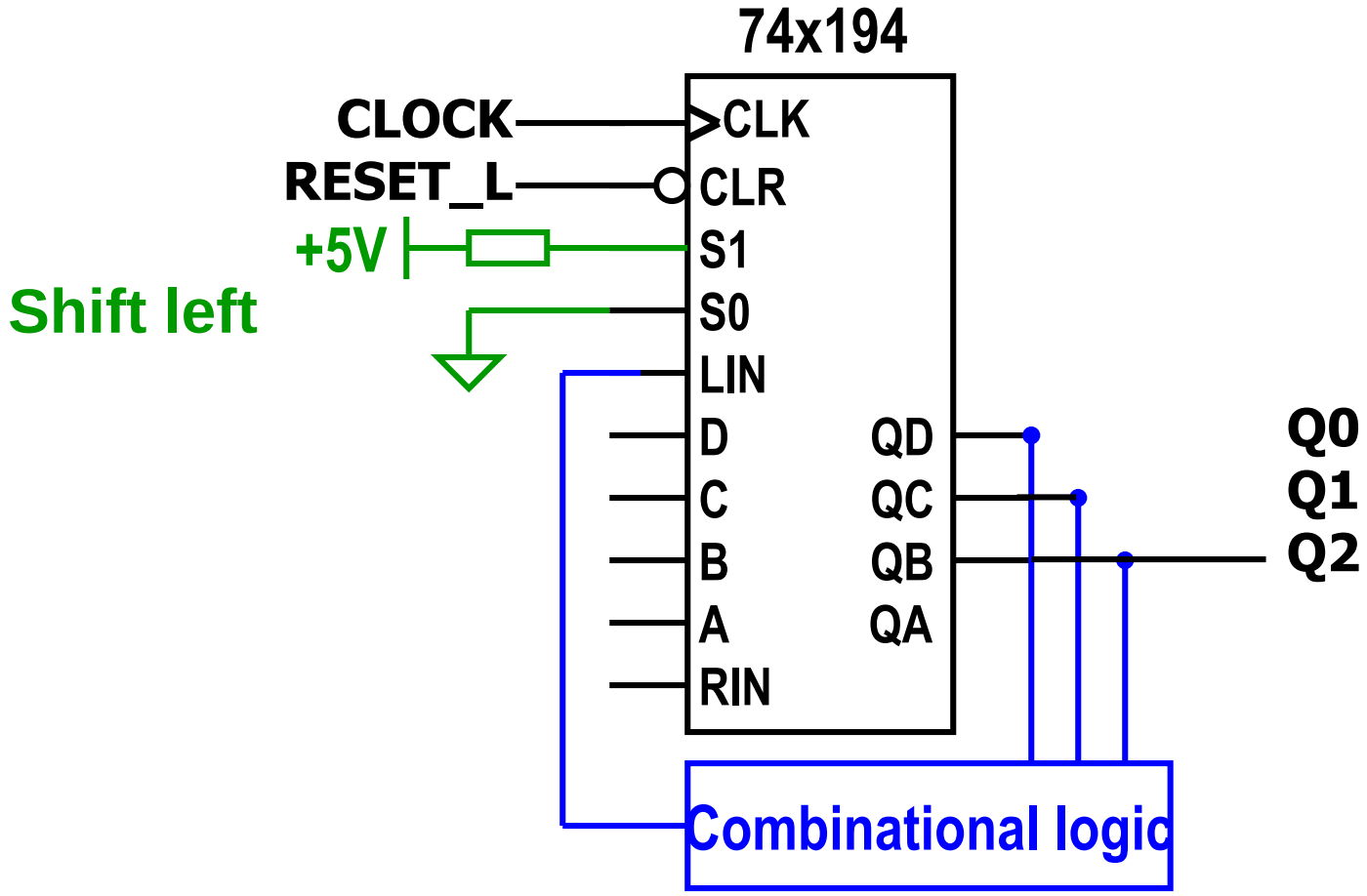
Q_2 \ Q_1Q_0	00	01	11	10
0	1	0	1	1
1	0	1	0	0

$$D_0 = Q_2 \cdot Q_1' \cdot Q_0 + Q_2' \cdot Q_1 + Q_2' \cdot Q_0'$$



Solution 1：分立元件—D触发器

$$D_0 = Q_2 \cdot Q_1' \cdot Q_0 + Q_2' \cdot Q_1 + Q_2' \cdot Q_0'$$



Solution 2：MSI芯片—74x194

$$D_0 = LIN = Q_2 \cdot Q_1' \cdot Q_0 + Q_2' \cdot Q_1 + Q_2' \cdot Q_0'$$

Conclusion: Sequence generator design method （using shift register)

Example ： generating 8-bit sequence 110 110 01

1）number of flip-flops： n

2^n>length(sequence): 8 bits sequence， need at least 3 flip-flops；

If choose 3 flip-flops， 110 states occurs 2 times， so n should be 4.

2）steps：

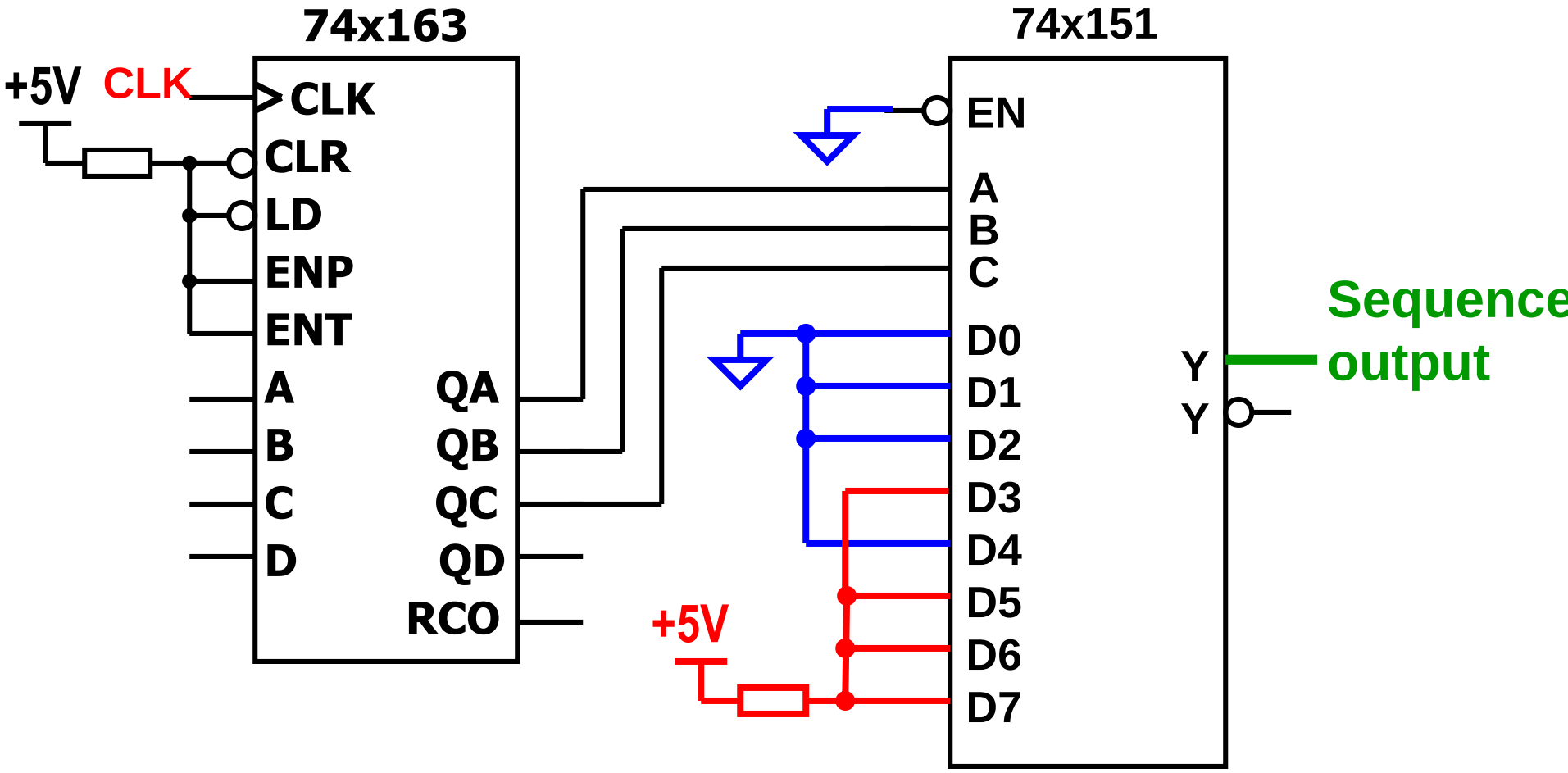
State-machine design procedure.

Need only one excitation equation:$D_0=F(Q_0,Q_1,\ldots Q_{n-1})$

思考：写出反馈方程$D_0=F(Q_0,Q_1,\ldots Q_{n-1})$=？

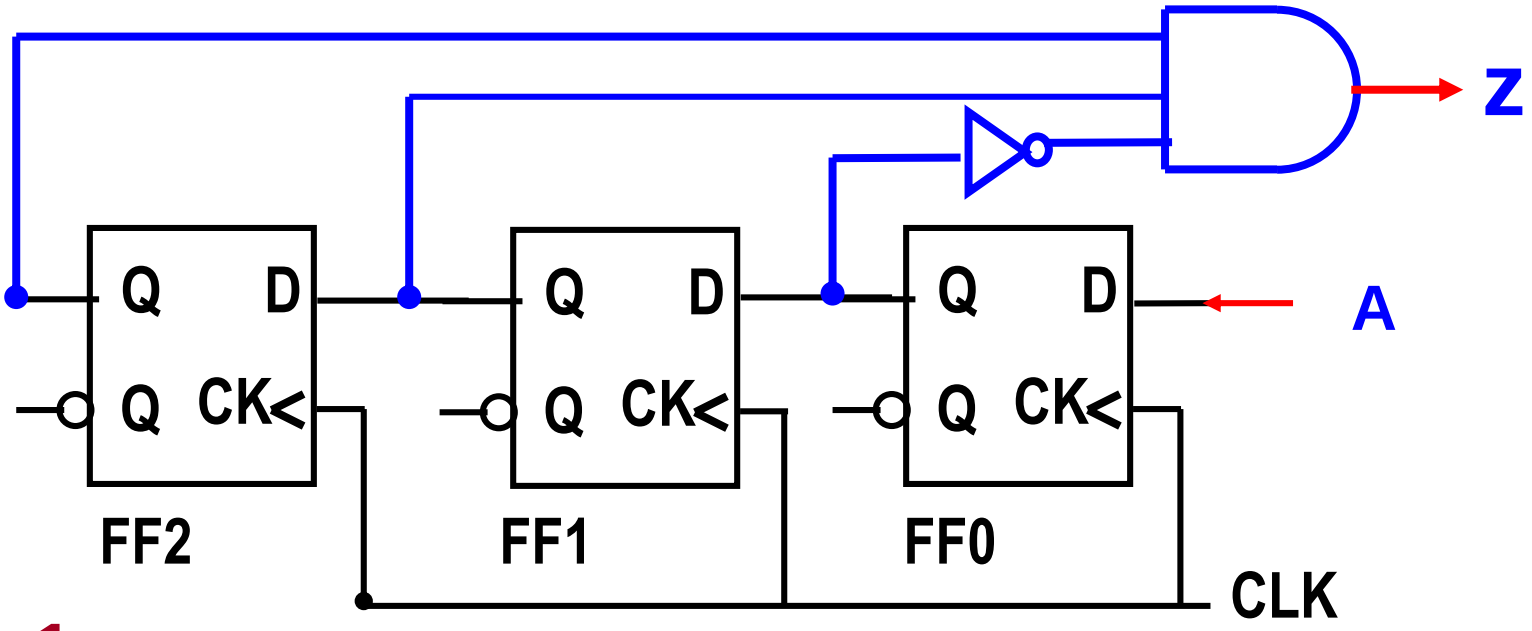
Review: sequence generator using counter and multiplexer

Example： generating 8-bit periodic sequence 00010111

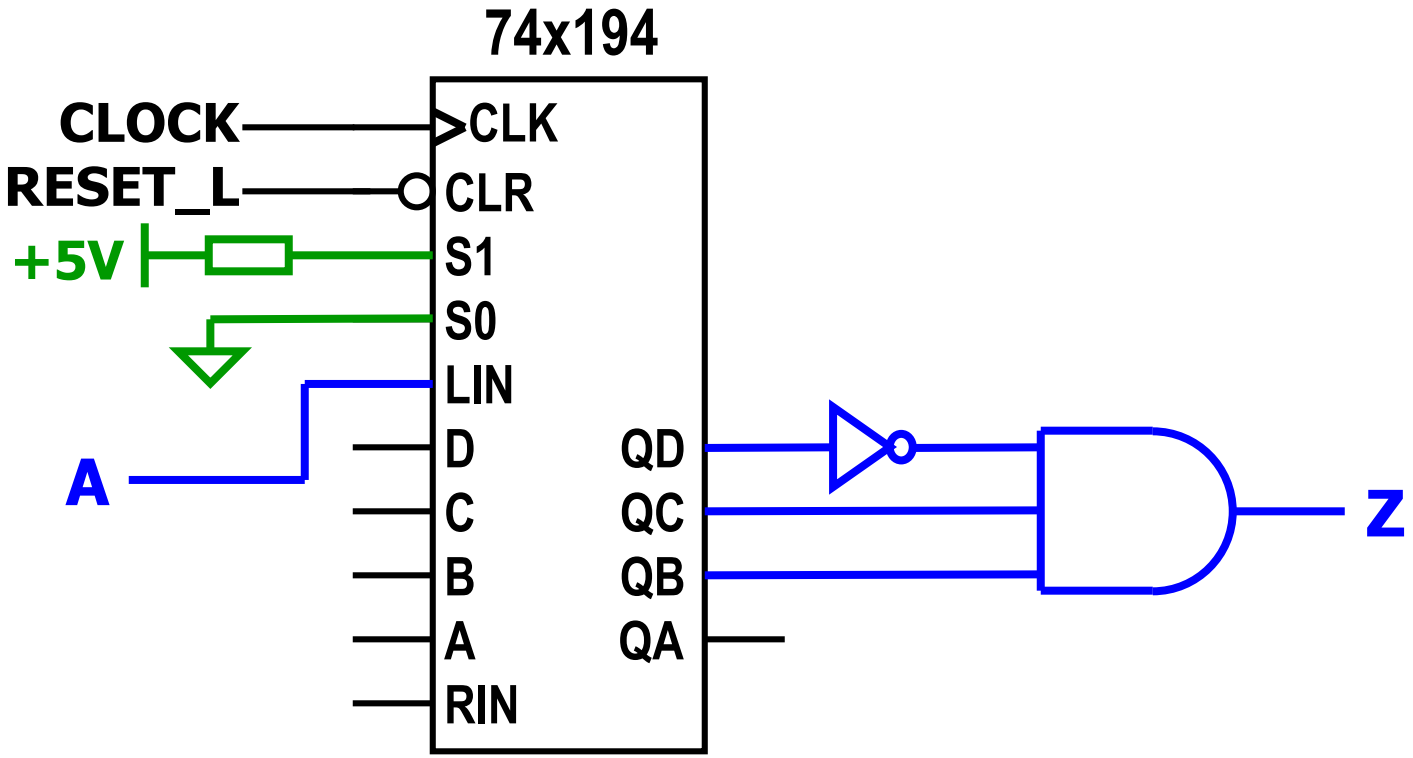


Shift registers的其他应用(2)：
Sequence detector

Example: design 110 sequence detector，When 110 is detected on input A , Output Z is 1. complete the function using shift register.



Solution 1



Solution 2

思考：如果是A是从RIN输入呢？

Review: 110 sequence detector using state machine

See also chapter 7

S	A = 0	A = 1	z
STA	STA	A1	0
A1	STA	A11	0
A11	OK	A11	0
OK	STA	A1	1
	S*		

Moore state machine

$D_0 = A \cdot Q_1' \cdot Q_0' + A' \cdot Q_1 \cdot Q_0' + A \cdot Q_1 \cdot Q_0$

$D_1 = Q_0' \cdot Q_1 + A \cdot Q_0 \cdot Q_1'$

$Z = Q_0 \cdot Q_1$

Summary of Chap.8

- **SSI latches and flip-flops**
- **MSI**
  - **Multi-bit latches and registers**
  - **Counter: 74x163**
  - **Shift register: 74x194**
- **Counters**
  - **Application of Counter**
  - **Ripple counters, Synchronous counters**

  ---Arbitrary modulo-m counter

  ---Sequence generators

  ---Decoding binary counter states

Shift Registers

- Shift Register types
- Application of shift register

---Shift register counters: Ring counters, Johnson counters, LFSR counters

---Sequence generator, sequence detector

第7章 要求

重点学习掌握：

1）锁存器、触发器的区别；

2）D型、J-K型、T型触发器的时序特性，功能表，特征方程表达式，不同触发器之间的相互转换；

3）钟控同步状态机的模型图，状态机类型及基本分析方法和步骤，使用状态图表示状态机状态转换关系；

4）钟控同步状态机的设计：状态转换过程的建立，状态的化简与编码赋值、未用状态的处理——风险最小方案和成本最小方案、使用状态转换表的设计方法、使用状态图的设计方法。

第8章 要求

重点学习掌握：学习利用基本的逻辑门、时序元件作为设计的基本元素完成规定的钟控同步状态机电路的设计任务：计数器、移位寄存器、序列检测电路和序列发生器的设计；学习利用基本的逻辑门和已有的中规模集成电路（MSI）时序功能器件作为设计的基本元素完成更为复杂的时序逻辑电路设计的方法。