**电子科技大学2016-2017学年第一学期期末考试A卷参考解答**

考试科目：数字逻辑设计及应用考试形式：闭卷考试日期： 2017年1月10日

成绩构成比例：平时20/30%， 期中20/30%， 小班研讨20/0%， 期末40%

本试卷由V部分构成，共6页。考试时长：120分钟 注：可以带纸质英文字典,不使用计算器

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 题号 | I | II | III | IV | V | 合计 |
| 得分 |  |  |  |  |  |  |

|  |
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| 得分 |
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**I. Please fill out the correct answers in the bracket “（）”. (For 1-8, 2’ X 12 =24, For 9-12, 4’X 4 =16,total 40’)**

1. For an8-bit DAC, its output voltage is 1.00V when the input is 01100100. If the input is 10001010, the corresponding output voltage will be ( 1.38 )V.

2. If a ROM has 8-bit address inputs and 4-bit data outputs, then it can be used to implement ( 4 ) combinational logic functions. Its capacity is ( 1024 ) bits.

3.A 5-bit Johnson counter without self-correcting has ( 10 ) valid states at most.A 4-bit ring counter without modification has ( 4 ) states in the cycle at most.

4. Parity circuit can be used to detect errors during data transfer. Suppose that a 9-bit parity code with 8-bit information data and 1-bit parity is implemented in one data transfer system and the receiver get a data string 010011001 without error indicated, then the parity circuit realize a ( even ) (odd/even) parity.

5. The 74x85 is a 4-bit magnitude comparator. If input A=B, and the less-than output ALTBOUT=1, then the cascading inputs should be AGTBIN = ( 0 ), AEQBIN =( 0 ) and ALTBIN = ( 1 ).

6. The 74x148 is an 8-input priority encoder with active low inputs and outputs. If its I0,I4 and I7 inputs are activated then the output code is ( 000).

7. To design a modulo-44 counter requires ( 6 ) D flip-flops at least. Also, the counter can be constructed by two 4-bit binary counter of 74x163, witch one cleared to zero when counting to 1010 and another loaded with ( 1100 ) when RCO=1.

8.A sequential circuit whose output depends only on its state is called a ( moore) state machine.

9. A 4-bit LFSR counter with feedback equation D0=Q3⊕Q2 yields a modulo-( 15 ) counter.

10. A sequence pulse generator circuit is shown in Figure 1. Assume the initial state of the circuit is Q3Q2Q1Q0 =1101 , the output sequencein Q3 is (11010 or 10101 ).

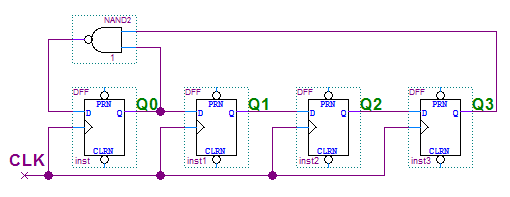


Figure 1

11. A sequential circuit implemented a function F is shown in Figure 2. The function is F=.

Table 1

|  |  |  |
| --- | --- | --- |
| S | S\* | Z |
| A | B | 0 |
| B | C | 0 |
| C | A | 1 |
| D | A | 0 |

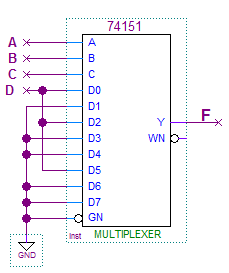


Figure 2.

12. According to the state/output table shown in Table 1, there are ( 3 ) states in the cycle.

|  |
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**II. Please choose the only correct answer and fill the item number in the barackets. (3’X5=15’)**

1. How many states are ambiguous according to the state diagram shown in Figure 3 ? ( B )

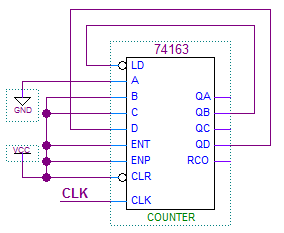
A. 1 B. 2 C. 3 D. 4

2. To design a “10011110” sequence pulse generator by shift registers, we need a ( B )-bit shift register at least.

A. 3 B. 4 C. 5 D.6

3. The modulus of the circuit shown in Figure 4 is ( C ).

A. 4 B. 5 C. 6 D.14



**A**

**B**

**C**

**D**

Y

Y’

XY

X

XY’

X

Figure 3. Figure 4.

Y

X’

Function table for 74X163

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Inputs | | | | Current State | Next state | Output |
| CLR\_L | LD\_L | ENT | ENP | QD QC QB QA | QD\* QC\* QB\* QA\* | RCO |
| 0 | X | X | X | X X X X | 0 0 0 0 | 0 |
| 1 | 0 | X | X | X X X X | D C B A | 0 |
| 1 | 1 | 0 | X | X X X X | QD QC QB QA | 0 |
| 1 | 1 | X | 0 | X X X X | QD QC QB QA | 0 |
| 1 | 1 | 1 | 1 | 0 0 0 0 | 0 0 0 1 | 0 |
| 1 | 1 | 1 | 1 | 0 0 0 1 | 0 0 1 0 | 0 |
| 1 | 1 | 1 | 1 | 0 0 1 0 | 0 0 1 1 | 0 |
| 1 | 1 | 1 | 1 | 0 0 1 1 | 0 1 0 0 | 0 |
| 1 | 1 | 1 | 1 | **………….** | **…………..** | 0 |
| 1 | 1 | 1 | 1 | 1 1 1 1 | 0 0 0 0 | 1 |

4. Which of the following statements is CORRECT? ( D )

A. An edge-triggered D flip-flop never goes into metastable status.

B. A master/slave J-K flip-flop keep the current status when input J=1 and K=1.

C. if S is asserted, an S-R latch is forced to logic stats Q=1.

D. A D latch will follow the input as long as the control input C is active.

5. The state/output table of a clocked synchronous state machine is shown in Table 2. Suppose that the initial state of the state machine is “A”, When input sequence is X=”10101110”, the corresponding output sequence Z will be ( A ).

A. 00010010 B. 00110010 C. 01000110 D. 00100010

Table 2.

|  |  |  |  |
| --- | --- | --- | --- |
|  | X | |  |
| S | 0 | 1 | Z |
| A | B | D | 0 |
| B | C | B | 0 |
| C | B | A | 1 |
| D | B | C | 0 |
|  | S\* | |  |

|  |
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| 得分 |
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III. Analyze the clocked synchronous state machine as shown below. **(15’)**

(1) Write out the excitation equations, transition equations and output equation. [2’]

(2) List out the transition/output table. [4’]

(3) Assume the initial state Q1Q0 is 00, draw the timing diagram for Q0, Q1and Z. [7’]

(4) Indicate the function for the logic circuit. [2’]

D0

CLK

Q0

Q0

D1

CLK

Q1

Q1

X

Z

CLK

**【参考答案】**

(2) 每格0.5分，共4分。

Transition/output table

|  |  |  |
| --- | --- | --- |
| Q1Q0 | X | |
| 0 | 1 |
| 00 | **01/0** | **00/0** |
| 01 | **01/0** | **10/0** |
| 10 | **01/1** | **00/0** |
| 11 | **01/1** | **10/0** |
|  | Q1\*Q0\*/Z | |

(1) 激励方程每个0.5分，转移方程共0.5分，输出方程0.5分，

共2分。

激励方程: D0 = X' D1 = X·Q0

转移方程: Q0 = X' Q1 = X·Q0

输出方程: Z = X'·Q1

CLK

X

Q0

Q1

Z

(3) Q1和Q0每个触发沿0.5分，

Z每个变化沿0.5分，共7分。

(4) 电路功能：可重叠的010序列

检测。(2分)

|  |
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| 得分 |
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**VI.**  Design a 2-bit Gray-code up/down counter with two D Flip-flops and some gates. Q1Q0 represent the counter value in Gray-code. M is the up/down select input. When M=1, the counter counts in ascending Gray-code order and then the output Z will be 1 when counter value reaches 3. When M=0, the counter counts in descending Gray-code order and then the output Z will be 1 when counter value reaches 0. **(15’)** (1) List out the transition/output table. [4’]

(2) Fill out the Karnaugh maps. [3’]

(3) Write out the transition equations, excitation equations and output equation. [4’]

(4) Draw the logic circuit diagram. [4’]

**【参考答案】**

(1) 每行1分，共4分。

Transition/output table

|  |  |  |
| --- | --- | --- |
| Q1Q0 | M | |
| 0 | 1 |
| **00** | **10/1** | **01/0** |
| **01** | **00/0** | **11/0** |
| **11** | **01/0** | **10/0** |
| **10** | **11/0** | **00/1** |
|  | Q1\*Q0\*/Z | |

(2) 每个卡诺图1分，共3分。

|  |  |  |  |
| --- | --- | --- | --- |
| **1** | **0** | **0** | **1** |
| **0** | **1** | **1** | **0** |

Q1Q0

M

0

00

01

11

10

1

Q1\*

|  |  |  |  |
| --- | --- | --- | --- |
| **0** | **0** | **1** | **1** |
| **1** | **1** | **0** | **0** |

Q1Q0

M

0

00

01

11

10

1

Q0\*

|  |  |  |  |
| --- | --- | --- | --- |
| **1** | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** |

Q1Q0

M

0

00

01

11

10

1

Z

(3) 转移方程每个1分，激励方程每个0.5分，输出方程1分，共4分。

转移方程：Q0\* = M'·Q1+M·Q1' 或M⊕Q1 Q1\* = M'·Q0'+M·Q0 或M⊙Q0

激励方程：D0 = M'·Q1+M·Q1' 或M⊕Q1 D1 = M'·Q0'+M·Q0 或M⊙Q0

输出方程：Z = M'·Q1'·Q0'+M·Q1·Q0' 或 Q0'·(M⊙Q1)

(4) 略。（共4分）

|  |
| --- |
| 得分 |
|  |

**V.**  Design an “101110” sequence generator with the shortest path self-correction only using one 74x194 and one 74x151. 74x194 will work in shift left mode. QA of 74x194 will be the sequence output. **(18’)**

(1) Fill out **LIN** in the simple transition table for 74x194. [7’]

(2) Write out the maxterm list of the feedback function for LIN. [1’]

(3) Fill out the K-maps. [3’]

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| The function table for 74x151 | | | | | |
| Iutputs | | | | Outputs | |
| EN\_L | C | B | A | Y | Y\_L |
| 1 | x | x | x | 0 | 1 |
| 0 | 0 | 0 | 0 | D0 | D0’ |
| 0 | 0 | 0 | 1 | D1 | D1’ |
| 0 | 0 | 1 | 0 | D2 | D2’ |
| 0 | 0 | 1 | 1 | D3 | D3’ |
| 0 | 1 | 0 | 0 | D4 | D4’ |
| 0 | 1 | 0 | 1 | D5 | D5’ |
| 0 | 1 | 1 | 0 | D6 | D6’ |
| 0 | 1 | 1 | 1 | D7 | D7’ |

(4) Draw the logic circuit diagram. [7’]

**【参考答案】**

(1) 上面六行2分，下面六行每行0.5分，共7分。

Simple transition table for 74x194

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| QA | QB | QC | QD | LIN |
| 1 | 0 | 1 | 1 | **1** |
| 0 | 1 | 1 | 1 | **0** |
| 1 | 1 | 1 | 0 | **1** |
| 1 | 1 | 0 | 1 | **0** |
| 1 | 0 | 1 | 0 | **1** |
| 0 | 1 | 0 | 1 | **1** |
| 0 | 0 | 0 | 0 | **1** |
| 0 | 0 | 0 | 1 | **1/0** |
| 0 | 0 | 1 | 0 | **1** |
| 0 | 0 | 1 | 1 | **1** |
| 0 | 1 | 0 | 0 | **1** |
| 0 | 1 | 1 | 0 | **1** |
| 1 | 0 | 0 | 0 | **1** |
| 1 | 0 | 0 | 1 | **1/0** |
| 1 | 1 | 0 | 0 | **1** |
| 1 | 1 | 1 | 1 | **0** |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| The function table for 74x194 | | | | | | |
| Iutputs | | Next state | | | | Function |
| S1 | S0 | QA\* | QB\* | QC\* | QD\* |
| 0 | 0 | QA | QB | QC | QD | Hold |
| 0 | 1 | RIN | QA | QB | QC | Shift right |
| 1 | 0 | QB | QC | QD | LIN | Shift left |
| 1 | 1 | A | B | C | D | Load |

(2) LIN **=** ∏QA,QB,QC,QD (*m*7, *m*9, *m*13, *m*15) (1分)

(3) 第一个卡诺图1分，第二个卡诺图2分，共3分。

|  |  |  |  |
| --- | --- | --- | --- |
| **1** | **1** | **1** | **1** |
| **1/0** | **1** | **0** | **1/0** |
| **1** | **0** | **0** | **1** |
| **1** | **1** | **1** | **1** |

QAQB

QCQD

00

00

01

11

10

01

11

10

LIN

|  |  |
| --- | --- |
| **1** | **1** |
| QA’/1/0 | QA’ |
| **1** | **0** |
| **1** | **1** |

QB

QCQD

00

0

1

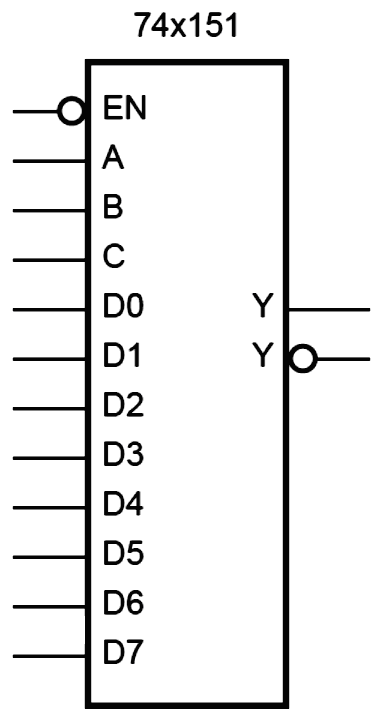
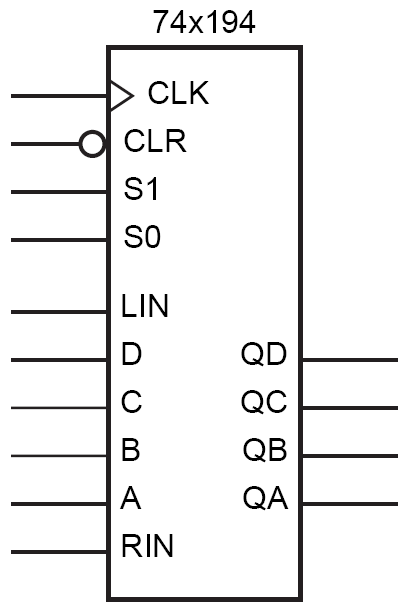
01

11

10

LIN

(4) 74x194输入端1分，74x151输入端每个0.5分，共7分。



Vcc

Clock

Vcc

Sequence output

QA/1/0