**电子科技大学2019-2020学年第 2 学期期 末 考试 A卷**

考试科目： 数字逻辑设计及应用 考试形式： 闭卷 考试日期： 2020年8月25日

本试卷由 VI部分构成，共 9页。考试时长：120分钟

成绩构成比例：平时成绩 40 %，期末成绩 60 % 注： 不准带计算器和词典

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| 题号 | I | II | III | IV | V | VI | 合计 |
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(Please refer to the appendix for the function description of 74 chips)

**I. Please fill out the correct answers in the brackets.(2’×15 = 30’)**

1. (99.75)10 = ( 1100011.11 )2 = ( 63.C )16
2. For an 8-bit digit system, given[A]= (11011101) two’s complement, [B] = (-73)10,   
   then A+B = ( 10010100 ) two’s complement, and is it overflow?(Yes/No) ( No ).
3. Table1 gives the specifications for 74HCT and 74ALS. When a 74ALS device drives a 74HCT device, the LOW-state DC noise margin is ( 0.3V ).

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| Table 1 | | | | | | | | | |
| Symbol | | VOLmax (V) | VOHmin (V) | IOLmax | IOHmax | VILmax (V) | VIHmin (V) | IIHmax | IILmax |
| Logic Family | 74HCT | 0.33 | 3.84 | 4.0 mA | -4.0 mA | 0.8 | 2.0 | -1 uA | 1 uA |
| 74ALS | 0.5 | 2.7 | 8.0 mA | -400 uA | 0.8 | 2.0 | 20 uA | -200 uA |

1. Given the function , the minimal sum expression of the function *F* is ( CD+BD+AC’D’ ).
2. If a read-only memory has 12 address input pins and 8 data output pins, then it contains ( 32 ) Kbits of memory.
3. When the input is the max value of a 6-bit DAC with single polarity, the corresponding output voltage is 4.90V. The output voltage is ( 2.80 ) V when the input is 100100.
4. An even-parity circuit is employed to generate parity bit for the information 010010001, then the parity bit is ( 0 改为1 ).
5. A modulo-24 counter circuit needs ( 5 ) D flip-flops at least. A modulo-356 counter circuit needs ( 3 ) 74x1634-bit counter(s) at least.
6. If a seial sequence 101011 generator is constructed by MSI 74x194shift register, then ( 1 ) MSI 74x194(s) is/are required at least.
7. A sequential logic circuit whose output depends not only on its states but also on its inputs is called a ( Mealy ) state machine.
8. If a T flip-flop is constructed by a D flip-flop, then the input D = ( T⊕Q或者 TQ’+T’Q ).
9. If we want to design a modulo-12 counter with twisted-ring count method, how many D flip-flops are required at least? The answer is ( 6 ) D flip-flops.

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**II. Choose the correct answer and fill in the brackets. ( 2’×10=20’ )**

1. Which of the followings is Excess-3 code for the decimal number 2476 ? ( C )

A.0010010001110110 B. 10100111110

C.0101011110101001 D. 1010011011100

1. A digital circuit is analyzed by two engineers based on the positive logic and the negative logic respectively, and the corresponding function expressions are gotten. The relationship between the two expressions is（ D）
2. equality B. don’t-care C. complement D. duality
3. Which one of the following statements is **not** correct? ( A )

A. Outputs of any two CMOS devices can be linked together.

B. Outputs of several open-drain gates can be tied together with a pull-up resistor to perform “wired logic”.

C. Three-state devices can output three states: High, Low and High-Impedance;

D. Unused CMOS inputs should never be floating.

1. The following expressions are equivalent to the logical function F=A’B+AC. Which is **not** correct ( B )
2. A’B+AC+BC B. (A+B’)(A+C)

C. A’BC’+A’BC+AB’C+ABC D. (A+B)(A’+C)

1. The static hazard of the combination logic circuit is caused by the reason that ( D ).

A. the circuit has many outputs.

B. the circuit is not the simplest one.

C. logic level interface of the gate devices are different in the circuit.

D. there is propagation delays at different signal paths in the circuit.

1. Multiple output signals may be active at the same time for the following digital circuit. Which is correct ? ( A ).

A. 74x148 Encoder B. 74x138 Decoder

C. 74x151 multiplexer D. Ring counter with 74x194 shift register

1. If a 74x85 magnitude comparator has ALTBIN=0, AGTBIN=1, AEQBIN=0, A3A2A1A0=0011, B3B2B1B0=1000 on its inputs, the outputs are ( B ).

A. ALTBOUT=0, AEQBOUT=0, AGTBOUT=0

B. ALTBOUT=1, AEQBOUT=0, AGTBOUT=0

C. ALTBOUT=1, AEQBOUT=0, AGTBOUT=1

D. ALTBOUT=0, AEQBOUT=0, AGTBOUT=1

1. Given the current state Q3Q2Q1 = 101 of the circuit shown in Figure 1, the next state is ( B )

A. 011 B. 111 C. 010 D. 110

Q

Q

CLK

D

Q

Q

CLK

D

Q

Q

CLK

D

CLK

Q3

Q2

Q1

Figure 1．

9. A Verilog HDL statement is shown below:

assign f = ^x;

If 'f' is a 1-bit wire variable and 'x' is a 4-bit input port. The value of input port x is 1011, then the value of wire f should be ( A ).

A. 1 B. 0 C. Hi-Z D. X

10. A Verilog HDL code block is shown below:

always @ (posedge clk)

begin

if (load)

a1 = in1;

else

a1 = a1+1;

end

'clk' is the clock signal input. 'in1' is a 4-bit input port. 'load' is a 1-bit input port. 'a1' is a 4-bit register variable. If the value of a1 is 4’b1111, in1 is 4’b0110, and load is 0 at the rising edge of clk, then the new value of a1 should be ( C )after the rising edge of clk.

A. 0110 B. 1110 C. 0000 D.0111

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**III.** A full subtractor handles 1-bit binary subtraction algorithm, having input bits X (minuend), Y (subtrahend), and BIN (borrow in), and output bits D (difference) and BOUT (borrow out).

Design such a full subtractor using a 74x153 and **just one** NOT gate. [12’]

(1) Fill out the truth table for the full subtractor. (4’)

(2) Write out the **minterm lists** of output bits D (X, Y, BIN) and BOUT(X, Y, BIN). (4’)

(3) Complete the logic diagram with 74x153 **as shown on the next page**. (4’)

参考答案及评分标准：

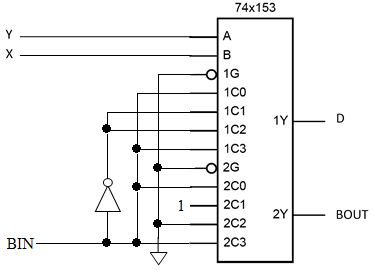
(1) 填真值表，每空0.25分，共4分。

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| X | Y | BIN | D | BOUT |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

Truth table for the full subtractor

(2) （正确得2分）

（正确得2分）

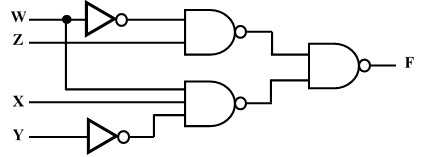
****(3) 74x153的8个数据输入端，每个连接正确得0.5分，共4分。

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**IV.** A combinational circuit is shown below. [6’]

(1) Write out the **sum-of-products** expression of output F. (2’)

(2) Analyze all conditions that the static hazard may exit for the logic circuit, and indicate the type(s) of static hazard. (4’)

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参考答案及评分标准：

（1）（正确得2分）

（2）可利用卡诺图或者代数法

当XYZ=101时（1分），W变化（1分），可能导致静态1型险象（2分）

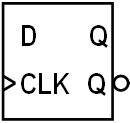
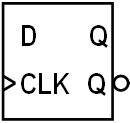
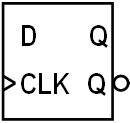
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**V.** Analyze the synchronous state machine circuit as shown below. [16’]

(1) Write the excitation equations, the state transition equations and the output equation. (7’)

(2) Fill out the transition/output table. (8’)

(3) Describe the logic circuit’s function. (1’)



**Q0**

**Q1**

**Q2**

**Z**

**CLK**

参考答案及评分标准：

(1) 每个表达式正确得1分，共7分。

Excitation equations:, ,

Transition equations:, ,

Output equation:

(2) 填表。（每空0.5分，共8分）

Transition / output table

|  |  |  |
| --- | --- | --- |
| Q2Q1Q0 | Q2\*Q1\*Q0\* | Z |
| 000 | 001 | 0 |
| 001 | 011 | 0 |
| 010 | 001 | 0 |
| 011 | 111 | 0 |
| 100 | 000 | 1 |
| 101 | 110 | 0 |
| 110 | 000 | 1 |
| 111 | 110 | 0 |

(3) 模5计数器。  （正确得2分）

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**VI.** Design a sequence signal generator with **self-correcting** to generate a serial output sequence of 100101 at output Z, using a **shift left** 74x194 , a 74x138, and **just one** NAND gate. [16’]

(1) Fill out the transition table. (8’)

(2) Write the **minterm list** of LIN. (2’)

(3) Complete the schematic diagram. (6’)

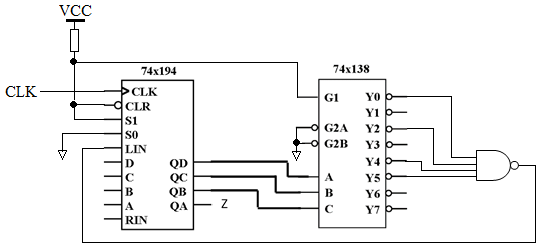
参考答案及评分标准：

(1) 填表。（每0.5分，共8分）

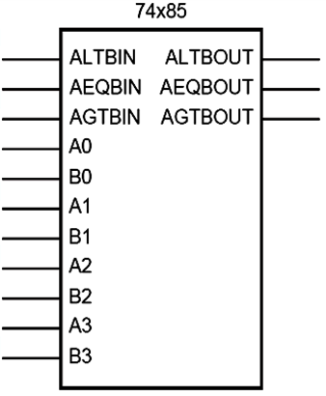
The transition table

|  |  |  |
| --- | --- | --- |
| QBQCQD | QB\*QC\*QD\* | LIN |
| 000 | 001 | 1 |
| 001 | 010 | 0 |
| 010 | 101 | 1 |
| 011 | 110 | 0 |
| 100 | 001 | 1 |
| 101 | 011 | 1 |
| 110 | 100 | 0 |
| 111 | 110 | 0 |

(2) （正确得2分）

(3) 算上与非门的四个输入，明确需要连接的有12个输入端，每个连接正确得0.5分，共6分。

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**Appendix**

Function description: Comparator

A(A3 A2 A1 A0), B(B3 B2 B1 B0) are two 4-bit binary numbers input.

AGTBOUT=1 only when (A>B) or (A=B and AGTBIN=1).

ALTBOUT=1 only when (A<B) or (A=B and ALTBIN=1).

AEQBOUT=1 only when A=B and AEQBIN=1.

Signal name abbrev:

LT means Less Than. GT means Greater Than.

EQ means Equal. IN means Input. OUT means Output.

