**电子科技大学2019-2020学年第一学期期 末 考试 A卷**

考试科目： 数字逻辑设计及应用 考试形式： 闭卷 考试日期： 2020年1月9日

本试卷由VI部分构成，共8页。考试时长：120 分钟

成绩构成比例：平时成绩60 %，期末成绩40 % 注：不准带计算器

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 题号 | I | II | III | IV | V | VI | 合计 |
| 得分 |  |  |  |  |  |  |  |

|  |
| --- |
| 得 分 |
|  |

**I. Please fill out the correct answers in the brackets “( )”.**

(Please refer to the appendix for the function description of 74 chips)**(2’×12 = 24’)**

1. A ROM has 4 address inputs and 4 data outputs, its capacity is ( 64 ) bits. To design a 2421BCD to Seven-Segment decoder constructed by this kind of ROM, ( 2 ) chips are required.

2. If the output voltage of an 8-bit unipolar DAC is 2.048V when the input code is 10000000, then the output voltage is (1.024) V for the DAC when the input code is 01000000.

3. A transceiver system employs an odd-parity circuit to generate parity bit from all information bits, then the parity code of the system is ( EVEN )(EVEN/ODD)-parity code.

4. A counter circuit is shown in Figure. 1. Is it a ring counter? (YES/NO) ( NO ). This counter has ( 6 ) valid states at most. Is it self-correcting? (YES/NO) ( NO ).

Figure 1

Q

Q

CLK

D

Q

Q

CLK

D

Q

Q

CLK

D

CLK

5.To design a serial sequence 11010110 generator, there are ( 3 ) flip-flops required at least. If the generator is constructed by shift register, ( 7 ) bits shift registers are required at least. If the generator is implemented by MSI 74x194, ( 2 ) chip(s) should be used at least.

6.74x85 is a 4-bit magnitude comparator with cascading inputs. If input A>B, and cascading inputs AGTBIN=0, AEQBIN=0, ALTBIN=1, then outputs AGTBOUT= ( 1 ), ALTBOUT= ( 0 ).

|  |
| --- |
| 得 分 |
|  |

**II. Choose the correct answer and fill in the brackets.(3’×5=15’)**

1. The state/output table of an FSM circuit is shown in Table 1. X is input and Y is output. According to the table, the correct statement is ( C ).

Table 1 State/output table

|  |  |  |  |
| --- | --- | --- | --- |
| S | X | |  |
| 0 | 1 | Y |
| A | A | C | 0 |
| B | B | A | 0 |
| C | C | B | 1 |
| D | A | A | 0 |
|  | S\* | |  |

A. Mealy machine, 3 valid states B. Mealy machine, 4 valid states

C. Moore machine, 3 valid states D. Moore machine, 4 valid states

2. The modulus of the LFSR counter circuit shown in Figure 2 is ( D )

A. 4 B. 5 C. 6 D. 7

Q

Q

CLK

D

Q

Q

CLK

D

Q

Q

CLK

D

CLK

Figure 2 LFSR counter circuit

CLK

EN

A

B

C

D0

D1

D2

D3

D4

D5

D6

D7

Y

Y

CLK

CLR

S1

S0

LIN

RIN

D

C

B

A

QD

QC

QB

QA

VCC

74x194

74x151

Figure 3 Serial sequence generator

3. The serial sequence generator constructed by MSI 74x194 and 74x151 is shown in Figure 3. The output sequence of QA is ( B ).

A. 10001100 B. 11100101 C. 01010000 D.11011011

4. The 74x283 is a 4-bit binary adder. Suppose that the input C0=0, A0A1A2A3=1001, and B0B1B2B3=0101, then the outputs will be ( A ).

A. C4=1, S0S1S2S3=1100 B. C4=0, S0S1S2S3=1110

C. C4=0, S0S1S2S3=1100 D. C4=1, S0S1S2S3=1110

5. Which of the following statements about latches and flip-flops is NOT CORRECT? ( C ).

A. For an S-R latch, if both S and R are 1, then both outputs Q and QN are forced to 0.

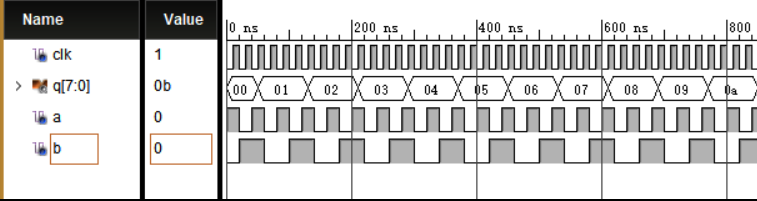
B. If J and K are asserted simultaneously, the next state of J-K flip-flop is the opposite of its current state.

C. Edge-triggered D flip-flop will never goes to metastable state.

D. For a D latch, the Q output will retain its last value without change when C input retains 0.

|  |
| --- |
| 得 分 |
|  |

**III.** We need to design a verilog hdl program to realize a special counter. The **correct** simulation result is shown below. But there are several errors in the main module shown below. Please find the errors and correct them. (10’)

****

`timescale 1ns / 1ps //1

module p1(clk,a, b, q) //2

input clk; //3

input a; //4

input b; //5

output q[7:0]; //6

reg [7:0] q =0; //7

always @ ( clk ) //8

begin //9

if (a &b) //10

q++; //11

else //12

q= 0; //13

end //14

endmodule //15

Please write the number of error line and correct it.

参考答案及评分标准：每空正确得1分，共10分。

Line ( 2 ) is error. Modified to: ( module p1(clk,a,b,q); )

Line ( 6 ) is error. Modified to: ( output [7:0] q; )

Line ( 7 ) is error. Modified to: ( always @ (posedge clk) )

Line ( 11 ) is error. Modified to: ( q <= q+1; )

Line ( 13 ) is error. Modified to: ( q <= q; 或q = q )

|  |
| --- |
| 得 分 |
|  |

**IV.** Analyze the clocked synchronous state machine in Figure 4. (21’)

(1) Write the excitation equations, the transition equations and the output equation. [7’]

(2) Fill out the transition/output table. [6’]

(3) Draw the state diagram. [4’]

(4) Assume the initial state Q0Q1Q2=000, draw the timing diagram for Q0, Q1, Q2 and Out. [4’]

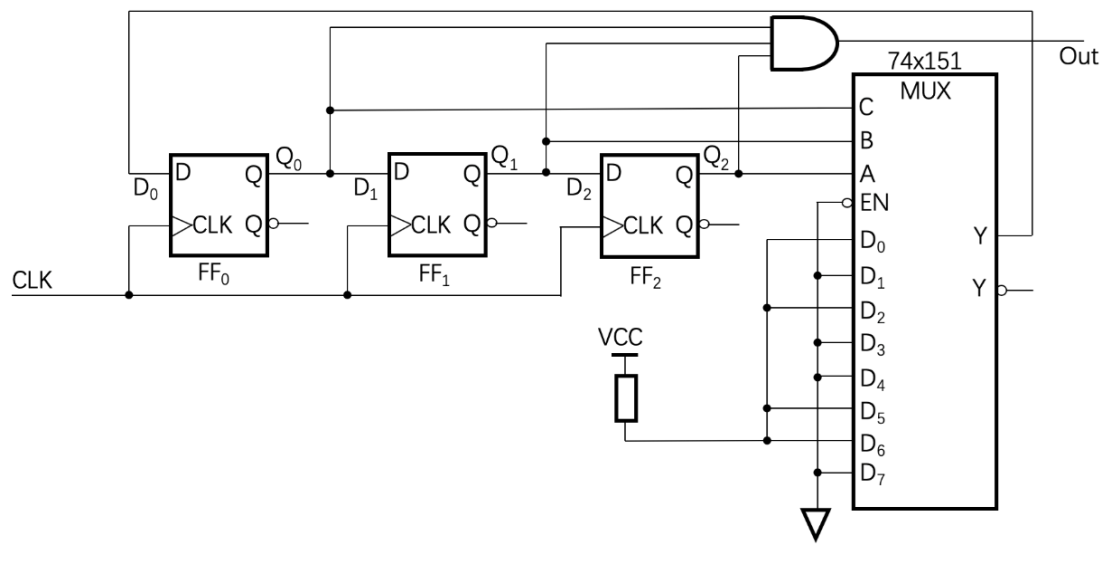


Figure 4

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Transition/output table | | | | | | |
| Q0 | Q1 | Q2 | Q0\* | Q1\* | Q2\* | Out |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 |

参考答案及评分标准：

(1) 每个方程正确得1分，共7分。

激励方程：D0 = ΣQ0,Q1,Q2(0,2,5,6)或Q0’Q1’Q2’ + Q0’Q1Q2’+ Q0Q1’Q2+ Q0Q1Q2’

D1 = Q0D2 = Q1

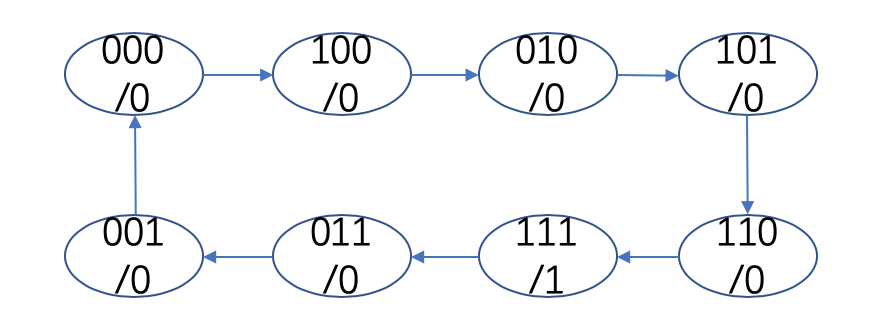
转移方程：Q0\* =ΣQ0,Q1,Q2 (0, 2, 5, 6) 或Q0’Q1’Q2’ + Q0’Q1Q2’+ Q0Q1’Q2+ Q0Q1Q2’

Q1\* = Q0Q2\* = Q1

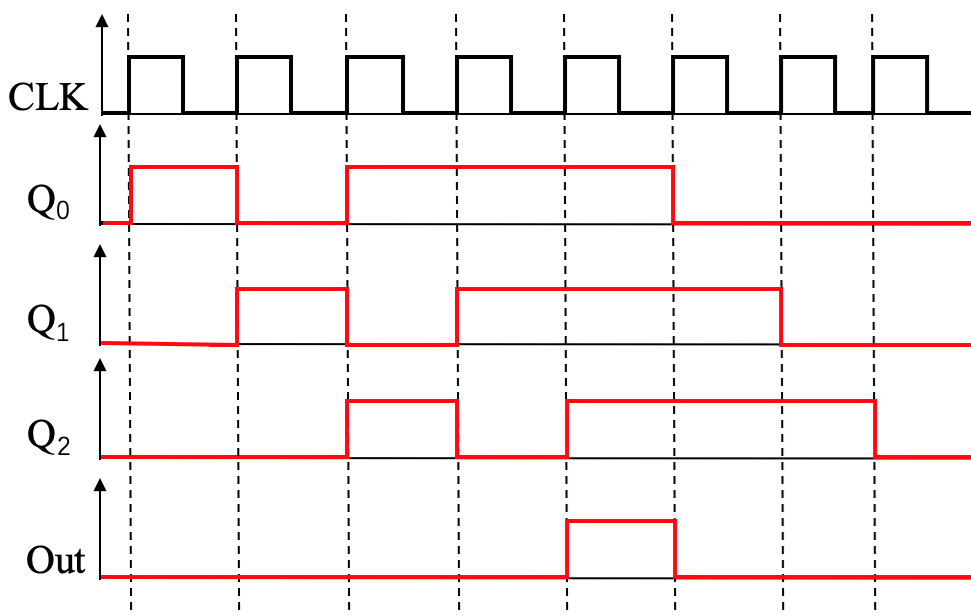
输出方程：Out = Q0·Q1·Q2

(2)填转移/输出表。转移表每个新状态正确得0.5分，输出表正确得2分，共6分。

(3) 画状态图，每个状态全对得0.5分，共4分。



(4) 画时序波形。每个触发边沿波形正确得0.5分，共4分。



|  |
| --- |
| 得 分 |
|  |

**V.** Design a clocked synchronous **Mealy** state machine with an input X and an output Z using D flip-flops to detect “11010” sequence. When the sequence of input X continuously appears 11010, the output Z is 1, otherwise 0. (11’)

(1) Fill out the **minimal** state/output table. [5’]

(2) Assume the state machine will never enter an unused state. The states value is assigned in binary ascending counting order. Please fill out the transition/output table with minimal-cost solution. [6’]

参考答案及评分标准：

(1) 填写状态/输出表。每格全对得0.5分，共5分。

|  |  |  |
| --- | --- | --- |
| State/output table | | |
| State | X | |
| 0 | 1 |
| Init | Init, 0 | Got 1, 0 |
| Got 1 | Init, 0 | Got 11, 0 |
| Got 11 | Got110, 0 | Got11, 0 |
| Got 110 | Init, 0 | Got1101, 0 |
| Got 1101 | Init, 1 | Got11, 0 |
|  | Next state, Z | |

(2) 填写转移/输出表。前5行每行全对得1分，后三行正确得1分，共6分。

|  |  |  |  |
| --- | --- | --- | --- |
| Transition/output table | | | |
| State | Q0Q1Q2 | X | |
| 0 | 1 |
| Init | 000 | 000, 0 | 001，0 |
| Got 1 | 001 | 000, 0 | 010, 0 |
| Got 11 | 010 | 011, 0 | 010, 0 |
| Got 110 | 011 | 000, 0 | 100, 0 |
| Got 1101 | 100 | 000, 1 | 010, 0 |
| Unused | 101 | ddd, d | ddd, d |
| Unused | 110 | ddd, d | ddd, d |
| Unused | 111 | ddd, d | ddd, d |
|  |  | Q0\*Q1\*Q2\*,Z | |

|  |
| --- |
| 得 分 |
|  |

**VI.** Connect the logic circuit in Figure 5 to design a modulo-12 counter with a counting sequence 0, 2, 3, 4, 5, 8, 9, 10, 11, 13, 14, 15.(19’)

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | | | | | | | | | |
| CLK | QD | QC | QB | QA | LD\_L | D | C | B | A |
| Positive Edge | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | X | X | X | X |
| 0 | 0 | 1 | 0 | 1 | X | X | X | X |
| 0 | 0 | 1 | 1 | 1 | X | X | X | X |
| 0 | 1 | 0 | 0 | 1 | X | X | X | X |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | X | X | X | X |
| 0 | 1 | 1 | 1 | 1 | X | X | X | X |
| 1 | 0 | 0 | 0 | 1 | X | X | X | X |
| 1 | 0 | 0 | 1 | 1 | X | X | X | X |
| 1 | 0 | 1 | 0 | 1 | X | X | X | X |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | X | X | X | X |
| 1 | 1 | 0 | 1 | 1 | X | X | X | X |
| 1 | 1 | 1 | 0 | 1 | X | X | X | X |
| 1 | 1 | 1 | 1 | 1 | X | X | X | X |

1. Fill the Table shown below to determin what values the intputs D, C, B, A and LD\_L should be in each output state QDQCQBQA for the mininal-cost reason.[8’]
2. Write the logic function expression of inputs LD\_L, D, C, B, A in the form of **minimal product-of-sums.** [5’]
3. Connect the logic circuit in Figure 5 without adding other component. [6’]

参考答案及评分标准：

(1) 填表。每行正确得0.5分，共8分。

(2) 每个表达式正确得1分，共5分。

LD\_L = (QA+QB+QC+QD)·(QA’+QB+QC’+QD)·(QA’+QB’+QC’+QD)

A=QB B= QA’ C= QB D= QA

(3) 电路连线。74x163的使能输入连接正确得0.5分，LD\_L反馈输入连接正确得0.5分，A, B, C, D输入连接正确各0.5分，每个或非门输入连接正确得1分，共6分。

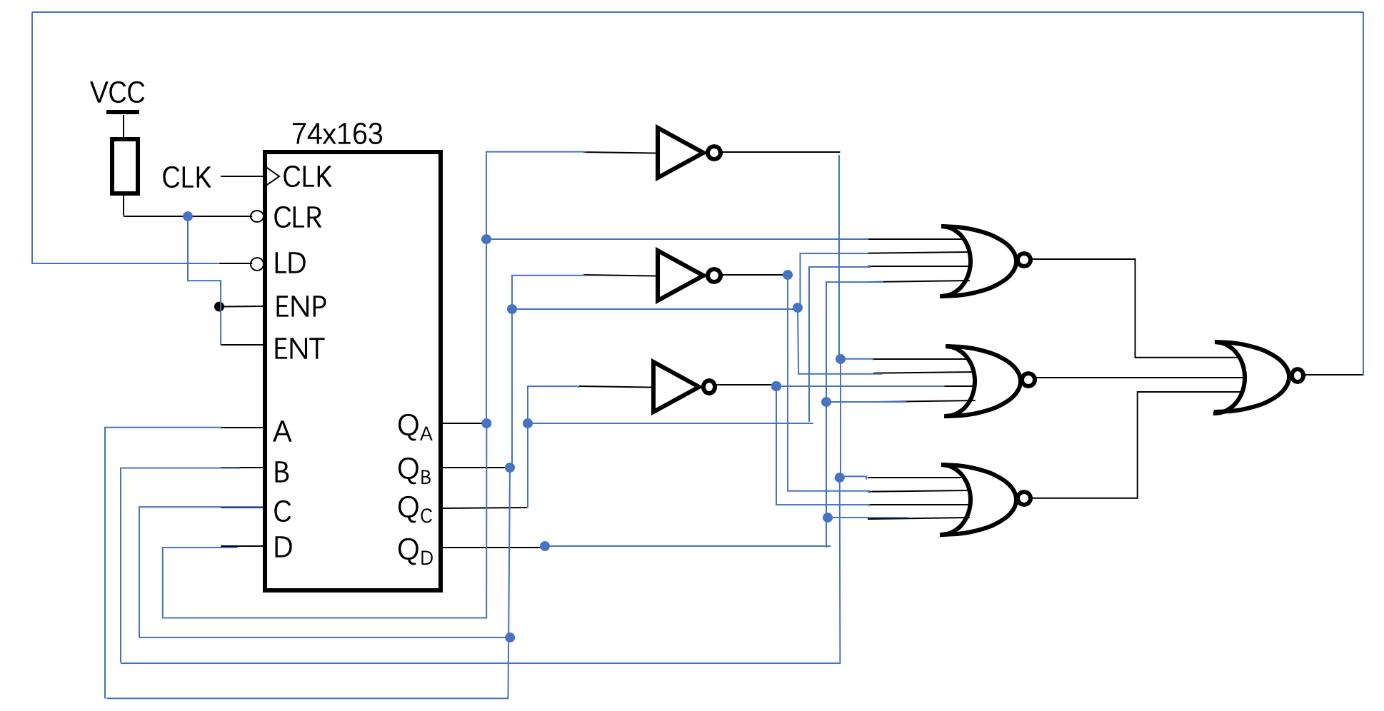
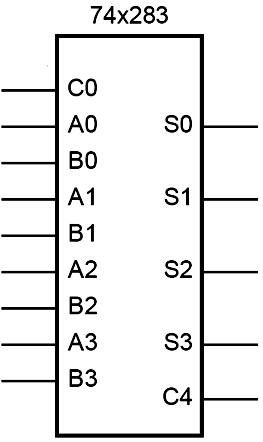


Figure 5

**=====================================================**

**Appendix**



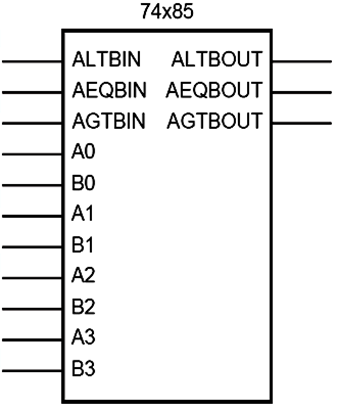
Function description: Adder

A(A3 A2 A1 A0), B(B3 B2 B1 B0) are two 4-bit binary number inputs.

C0 is the carry input.

S(S3 S2 S1 S0) is the sum output of C0 + A + B.

C4 is the carry output.



Function description: Comparator

A(A3 A2 A1 A0), B(B3 B2 B1 B0) are two 4-bit binary numbers input.

AGTBOUT=1 only when (A>B) or (A=B and AGTBIN=1).

ALTBOUT=1 only when (A<B) or (A=B and ALTBIN=1).

AEQBOUT=1 only when A=B and AEQBIN=1.

Signal name abbrev:

LT means Less Than. GT means Greater Than.

EQ means Equal. IN means Input. OUT means Output.

