**电子科技大学2020-2021学年第 1 学期期 末 考试 A卷**

考试科目： 数字逻辑设计及应用 考试形式： 闭卷 考试日期： 2021年 1 月 14 日

本试卷由 VI 部分构成，共 8页。考试时长：120分钟

成绩构成比例：平时成绩 60 %，期末成绩 40 % 注： 不准带计算器和词典

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| 题号 | I | II | III | IV | V | VI | 合计 |
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(Please refer to the appendix for the function description of 74 chips)

**I. Please fill out the correct answers in the brackets. (2’×14 = 28’)**

1. ( 215.625 )10 = ( 11010111.101 )2
2. ( 1101 )2421BCD + ( 1000 )Excess-3 = ( 0001 0010 )8421BCD
3. For an 8-bit digital system, Atwo’s complement = 0011 0010, Bone’s complement = 1000 0010,  
    A - B = ( 1010 1111 )two’s complement. Is it overflow ? (Yes/No) ( Yes ).
4. The parameters of a logic gate are listed as follow: VOLmax = 0.5V, VILmax = 0.8V, VOHmin = 2.7V, VIHmin = 2.1V, then the High-state DC noise margin is ( 0.6 )V.
5. If the dual logic function of F is FD = (A+B)·(A’+C), then the complement logic function of F is   
    F’ = ∑ABC ( 0, 2, 4, 5 ).
6. ((A⊙B)·( C⊙D))’ = ∏ABCD ( 0, 3, 12, 15 ).
7. The minimal sum of ∏ABCD (5, 7, 12, 13, 15) is ( A’∙D’+C∙D’+B’ )
8. If A = B⊕C, then C = ( A⊕B 或 A’∙B+A∙B’ )
9. If the information data is 10110010 for an odd parity system, then the parity bit should be ( 1 ).
10. The 74x148 is an MSI of 8-input priority encoder, its inputs and outputs are active low. If the inputs I7-L I6-L I5-L I4-L I3-L I2-L I1-L I0-L = 10101101 and the enable input is asserted, then the outputs A2-L A1-L A0-L is ( 001 ).
11. How many flip-flops are needed at least to design a LFSR counter with modulus 63? ( 6 )
12. Transition/output table for a sequential circuit is shown in Table 1, X is input and Z is output, the sequential circuit is a modulus ( 3 ) up/down counter.

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| Table 1 State/output table | | |
| *X*  *S*n | 0 | 1 |
| *S*0  *S*1  *S*2  *S*3 | *S*2/1  *S*0/0  *S*1/0  *S*0/0 | *S*1/0  *S*2/0  *S*0/1  *S*2/0 |
| *S*n+1/*Z* | | |

1. Assume the minimal output voltage of an 8 bit DAC is 0V, and the corresponding output voltage is 3.32V when the input is 01010101. Then the output voltage range for the DAC is ( 0 ~ 9.96 )V

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**II. Choose the correct answer and fill in the brackets. ( 2’×10=20’ )**

1. Which of the following logical function is equivalent to F = (AB)’+(BC)’+AC ? ( )

A. F = C+A∙B B. F = B+A∙C C. F = A+B∙C D. F = A+B+C

1. Which of the following statement is **ERROR**? ( D )

A. Any logical function can be represented by a Karnaugh map.

B. The Karnaugh map of a logical function is unique.

C. The minimization of a Karnaugh map may not be unique

D. There must be essential prime implicant in a Karnaugh map.

1. Which of the following representations of logical functions is **not** unique? ( A )

A. logic expression B. true table C. canonical sum D. canonical product

1. The demultiplexer can be implemented by ( B ).

A. encoder B. decoder C. adder D. multiplexer

1. To generate a serial sequence **0100101** by using 74x194, what is the least number of 74x194(s) needed? ( B )

A. 1 B. 2 C. 3 D. 4

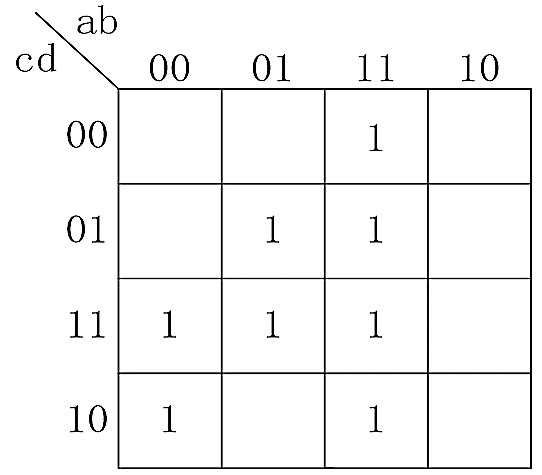
1. The CMOS circuit is shown in Figure 1. The expression of output F is ( A ).

A. ((A+B)·C)’ B. (A+B)·C C. (A·B+C)’ D. A·B+C

Figure 1

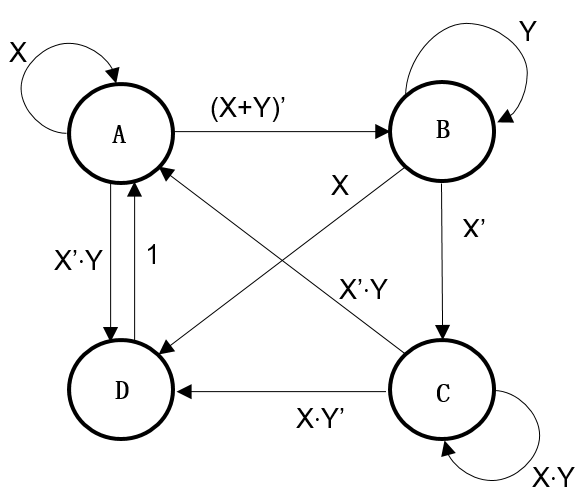
1. The Karnaugh map is shown in Figure 2. How many distinguished 1-cells are there in it? ( D )

A. 1 B. 2 C. 3 D. 4

 Figure 2

1. How many states are ambiguous in the state diagram shown in Figure 3? ( B )

A. 1 B. 2 C. 3 D. 4

 Figure 3

1. The memory with capacity of 64K×8 bits has ( B ).

A. 64K-bit address and 8-bit data B. 16-bit address and 8-bit data

C. 64K-bit data and 8-bit address D. 16-bit data and 8-bit address

1. A Verilog HDL statement is shown below:

assign d = ^(a & b);

**d** is a 1-bit wire variable. **a** and **b** are 4-bit input ports. If the value of input port **a** is 1011, **b** is 1010, then the value of **d** should be ( B ).

A. 1 B. 0 C. Z D. X

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**III.** Analyze the following Verilog HDL code block. **clk** is the clock signal input. **load** is a 1-bit input port. **data** is 4-bit output port. If the value of **load** is 1’b1 in the first clock period, and then keeps 1’b0. **(8’)**

(1) Write out all the values of the ouput port **data** in a cycle? [7’]

(2) Describe the function of the code block. [1’]

    reg [3:0] shift\_reg;

wire shift\_in;

    always @(posedge clk) begin

        if (load) shift\_reg <= 4’b1001;

        else shift\_reg <= {shift\_reg[2:0], shift\_in};

end

    assign shift\_in = shift\_reg[2] ^ shift\_reg[0];

    assign data = shift\_reg;

【参考答案及评分标准】

(1) 1001, 0011, 0111, 1110, 1101, 1010, 0100, (每个输出值正确得1分，共7分)

(2) 模7的LFSR计数器 (正确得1分)

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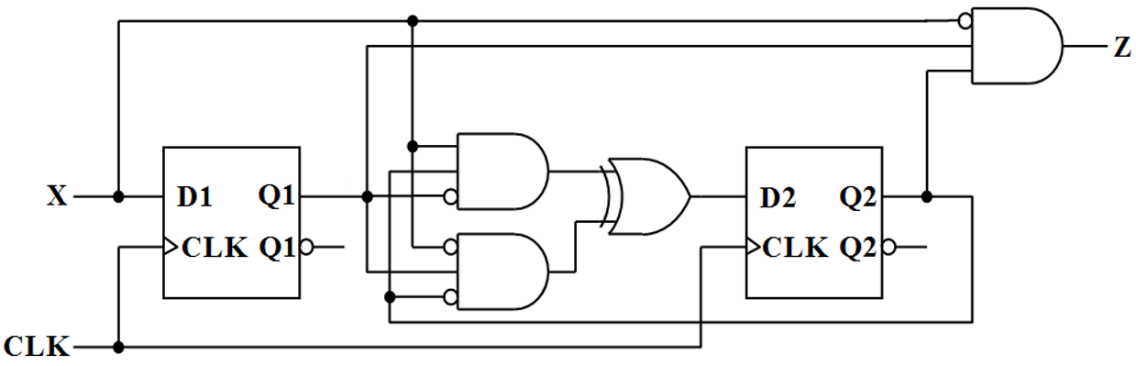
**IV.** Analyze the sequential logic circuit as shown below. **(20’)**

1. Write out the excitation equations and output equation. [3’]

2. List out transition/output table and draw a full state diagram. [8’]

3. Assume the initial state Q2Q1=00, draw the timing diagram for Q2 ,Q1 and Z. [8’]

4. Indicate the logic function of the circuit. [1’]

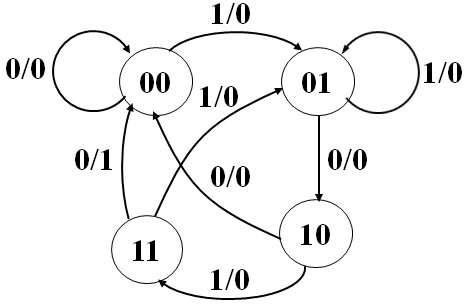
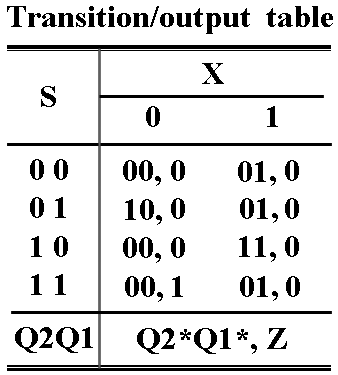


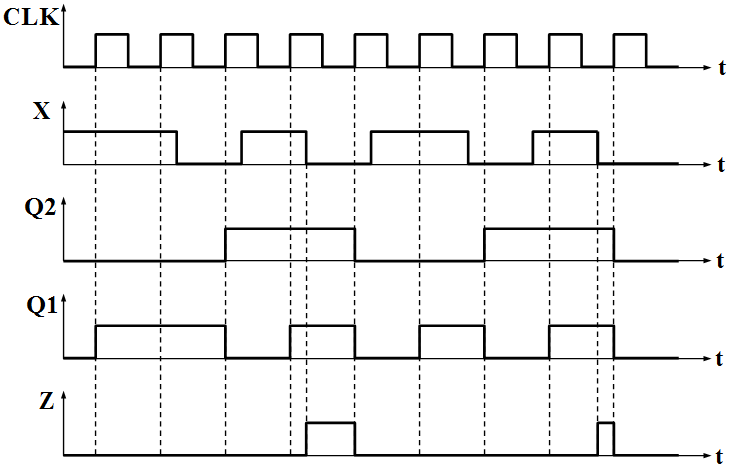
【参考答案及评分标准】

1. 激励方程: D1 = X（正确得1分），D2 = X·Q2·Q1’⊕X’·Q2’·Q1（正确得1分）

输出方程Z = X’·Q2·Q1（正确得1分）

2. 转移/输出表(每行正确得1分，共4分)，状态图(每个状态转移正确得0.5分，共4分)





3. 定时图(每个波形变化边沿0.5分，共8分)

4. 功能描述（1分）：

Mealy机，不可重叠的1010序列检测。

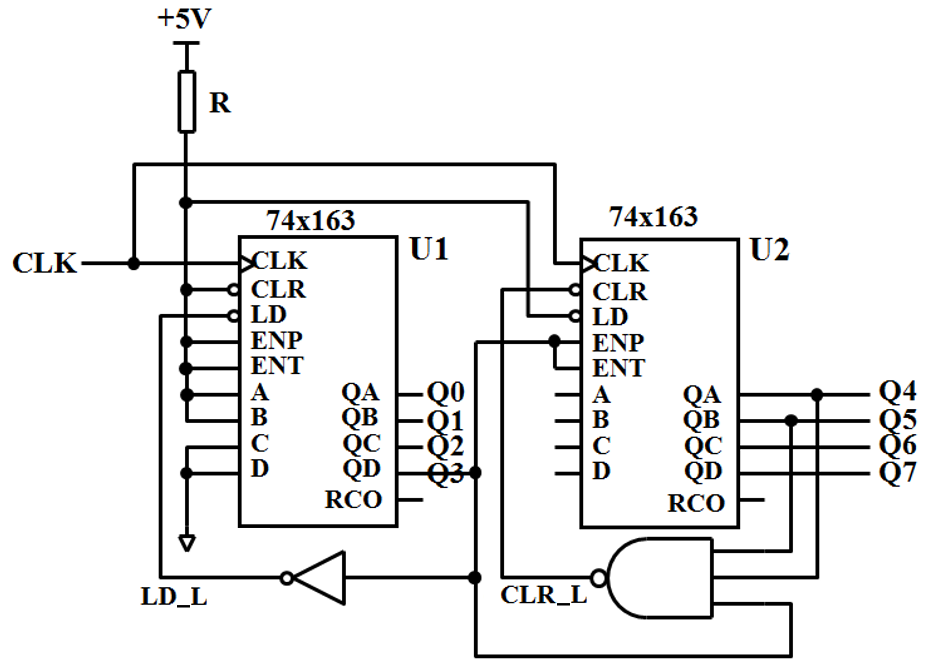
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**V.** Analyze the sequential-circuit as shown below, which contains two 74x163 4-bit binary counters and two gates. **(9’)**

1. Write out the logic expression of LD\_L for U1 and CLR\_L for U2. [2’]

2. Assume the initial value of the state output (Q7Q6Q5Q4Q3Q2Q1Q0) is 3, write out the state sequence in a cycle for the logic circuit. [6’]

3. Indicate the modulus for the logic circuit. [1’]

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【参考答案及评分标准】

1. LD\_L = Q3’（1分） CLR\_L = (Q5∙Q4∙Q3)’ （1分）

2. 状态序列：（6分）   
3, 4, 5, 6, 7, 8, 19, 20, 21, 22, 23, 24, 35, 36, 37, 38, 39, 40, 51, 52,53, 54, 55, 56, 3, …

3. modulus = 24（1分）

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**VI.** Design a sequence signal generator with **the shortest path self-correcting** to generate a serial output sequence Z=1011 using **only** a 74x194 and a 74x151 **without** other devices. Please select **shift left** mode for the 74x194. **(15’)**

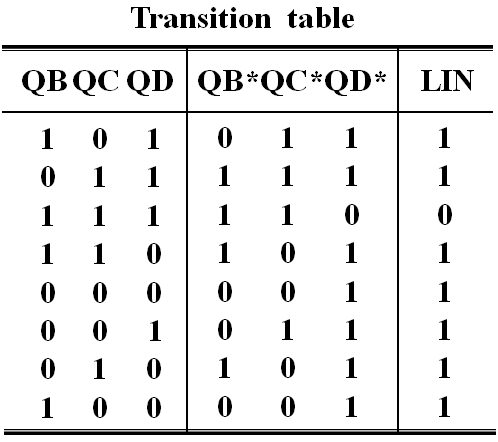
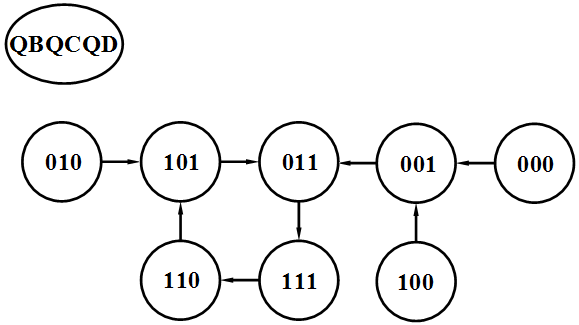
1. List out the transition table and draw a full state diagram. [8’]

2. Write out the **maxterm list** of the feedback function LIN(QB,QC,QD). [2’]

3. Draw a schematic diagram for the circuit. [5’]

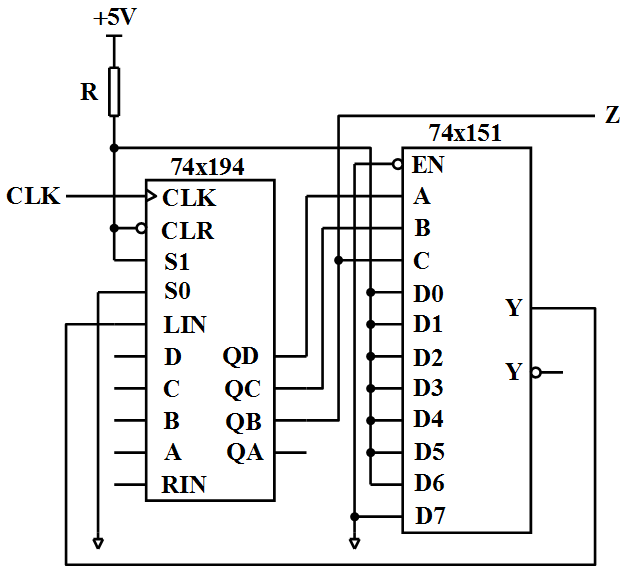
【参考答案及评分标准】

1. 转移表每行正确得0.5分，全状态图每个状态转移正确得0.5分，共8分。



2. 反馈函数正确得2分

LIN(QB,QC,QD) = ∏QB,QC,QD ( 7 )



3. 电路图

74x194的CLK, CLR, S1,S0连接正确得0.5分，LIN连接正确得0.5分，Z输出连接正确得0.5分，74x151的D输入端连接正确得2分，选择端连接正确得1分，使能端连接正确得0.5分，共5分。