**电子科技大学2022-2023学年第2学期期末考试A卷**

考试科目： 数字逻辑设计及应用 考试形式： 闭卷 考试日期： 2023 年 6 月 27 日

本试卷由 六 部分构成，共 8 页。考试时长： 120 分钟

成绩构成比例：平时成绩 60 %，期末成绩 40 % 注：禁止使用计算器及英文辞典

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 题号 | 一 | 二 | 三 | 四 | 五 | 六 | 七 | 八 | 合计 |
| 得分 |  |  |  |  |  |  |  |  |  |

|  |
| --- |
| 得 分 |
|  |

(Please refer to the appendix for the function description of 74 chips)

**I. Please fill out the correct answers in the brackets “( )”.**

**( 2’×15 = 30’ )**

1. (0001 1001 0101)8421BCD = ( 1100 0011 )2

2. For an odd-parity transceiver system, if the information bits sent are 10101010，then the parity bit should be ( 1 ).

3. The function of DAC is to convert ( digital ) inputs proportionally into analog outputs.

4. There are ( 2N-N ) invalid states for a N-bit Ring counter.

\*5. The three output states of the tristate gate are: logic "1", logic "0", and ( Hiz ).

\*6. To design a 3-input majority judger using AND-OR structure (output is “1” when the input is majority), ( 3 ) AND gates are required at least.

7. The FSM which its output depends not only on its states but also on the input is called ( Mealy ) machine.

\*8. A NAND gate in positive logic is called ( NOR ) gate in negative logic.

9. If a RAM’s capacity is 16K words × 8 bits, the address inputs should be ( 14 ) bits. We need ( 8 ) chips of 16K × 8 bits RAM to form a 32K × 32 bits RAM.

10. If the minimum incremental output voltage of an 8-bit unipolar DAC is 0.02V, then the output voltage is ( 2.72 ) V for the DAC when the input is 10001000.

11. A FSM with 130 states requires ( 8 ) flip-flops at least.

\*12. The implementation of 3-input CMOS NOR gate requires ( ) MOS transistors.

\*13. The input waveforms A, B, C, and output waveforms F of a combination logic circuit are shown in Fig. 1. The minterm list for this circuit are F( ).

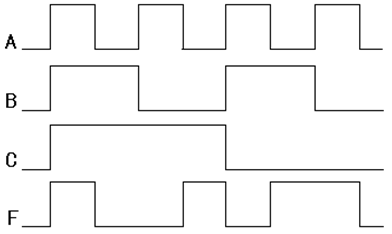


Fig. 1

14. The output of the circuit shown in Fig. 2 is F( 0,1,2,4 ).



Fig. 2

|  |
| --- |
| 得 分 |
|  |

**II. Choose the correct answer and fill in the brackets. ( 2’×10 = 20’ )**

1. A sequential circuit is shown in Fig. 3 with initial states Q2Q1 = 00. Which of the following is NOT the output serial sequence from Q1? ( C )

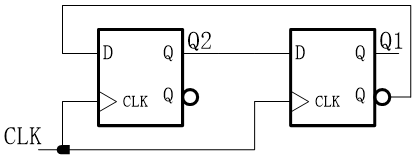


Fig. 3

A. 0011 B. 1001

C. 1101 D. 0110

2. If a Johnson counter with 12 valid states is constructed by shift register, ( B ) 74x194 shift register(s) should be used.

A. 1 B. 2

C. 3 D. 4

3. Let [A]two’s complement=10010011. Which of the following is true? ( C )

A. [-A]one’s complement = 01101100 B. [A]one’s complement= 10010100

C. [-A]sign-magnitude= 01101101 D. [A]sign-magnitude= 00010011

4. How many invalid states are there in the circuit shown in Fig. 4? ( D ).

A. 10 B. 11

C. 12 D. 13

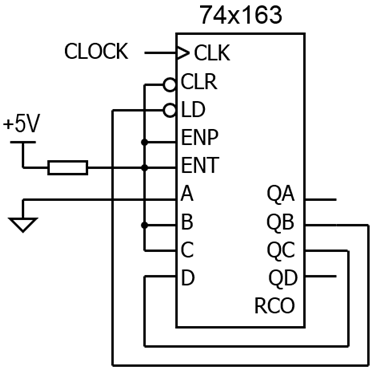


Fig. 4

5. There is no static hazard in expression ( B ).

A. F = B’C’+AC+A’B B. F = B’C’+AC+A’B+BC+AB’+A’C’

C. F = A’C’+BC+AB’+A’B D. F = A’C’+BC+AB’

\*6. A gate that can implement wired AND function is called ( ) gate.

A. open-drain B. OR

C. XOR D. AND

7. The minimum sum-of-products of  is ( A ).

A．W’X + Y’Z + WX’Y’ B. W’X + Y’Z + WX’Z’ + XZ

C．W’XY + Y’Z + WX’Z’ D. W’XZ’ + Y’X’Z + WX’Z’ + XZ

\*8. If we want to use an XNOR gate as an Inverter (NOT gate), then the inputs of A and B should be connected as ( ) .

A. one of the A and B connect to ‘1’ B. one of the A and B connect to ‘0’

C. A and B connect together D. can’t realize

9. The output of the following circuit shown in Fig. 5 is F = (A+B)’, when C1 and C2 are equal to ( D ).

A．0，0 B．0，1

C．1，0 D．1，1

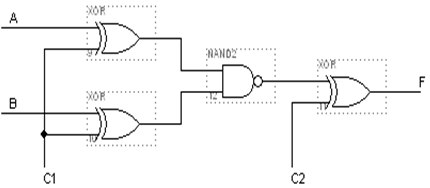


Fig. 5

10. The output signal of ( A ) circuit is 1-out-of-N code.

A. binary decoder B. binary encoder

C. seven-segment decoder D. decade counter

|  |
| --- |
| 得 分 |
|  |

**III.** A Verilog module for a 74x163 4-bit binary counter as shown below. Please fill in the missing code on the underlines to complete the module. [5’]

评分标准：每空正确得1分

module M74x163(CLK, CLR\_L, LD\_L, ENP, ENT, D, Q, RCO);

input CLK, CLR\_L, LD\_L, ENP, ENT;

input [3:0] D;

output [3:0] Q;

output RCO;

reg [3:0] Q;

reg RCO;

always @ (posedge CLK)

if (CLR\_L == 0) Q <= 4’b0;

else if (LD\_L == 0) Q <= D ;

else if ((ENT == 1) && ( ENP == 1 )) Q <= Q + 1;

else Q <= Q ;

always @ (Q or ENT)

if (( ENT == 1 ) && ( Q == 4’d15 )) RCO = 1;

else RCO = 0;

endmodule

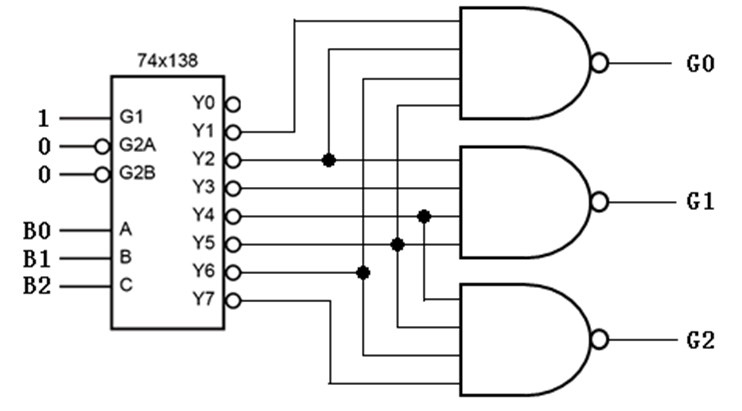
|  |
| --- |
| 得 分 |
|  |

**IV.** Analyze the combinational logic circuit as shown below. [10’]

1. Write out the **minterm list** of outputs G2B2,B1,B0, G1B2,B1,B0, G0B2,B1,B0. (3’)

2. Write out the **minimal sum-of-products** expression of each output. (6’)

3. Indicate the function of the circuit. (1’)



[Solution]

1. Minterm list （每个表达式正确得1分，共3分）

2. Minimal sum（每个表达式正确得2分，共6分）

3. 电路功能为将输入三位的二进制编码转换为格雷码。（正确得1分）

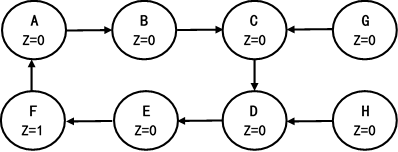
|  |
| --- |
| 得 分 |
|  |

**V.** Design a clocked synchronous state machine with the state diagram shown as below by using three D flip-flops. The state values Q2Q1Q0 of A~H are 000, 001, 010, 011, 100, 101, 110, 111 respectively. [17’]

1. Fill in the Karnaugh maps, write out the **minimal sum-of-products** expressions for the excitation equations. (12’)

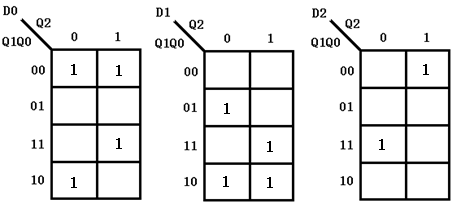
2. Write out the output equation. (3’)

3. Indicate the logic function of the state machine. (2’)



[Solution]

1. （卡诺图每个正确得2分，表达式每个正确得2分，共12分）



2. （正确得3分）

3. 带自启动功能的模6二进制加法计数器。 （正确得2分）

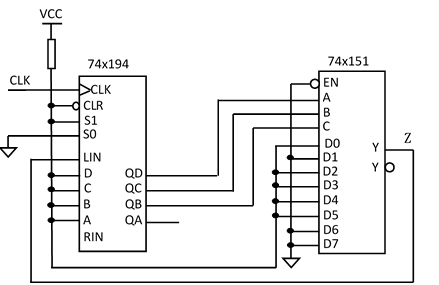
|  |
| --- |
| 得分 |
|  |

**VI.** Analyze the sequential logic circuit as shown below. [18’]

1. Write out the **minterm list** of the output Z QB,QC,QD . (3’)

2. Complete the transition/output table. (12’)

3. Assume the initial state QBQCQD is 001, write out the output sequence of Z in a cycle. (3’)



[Solution]

1. （正确得3分）

2. （转移输出表的新状态每空正确得1分，输出每空正确得0.5分，共12分）

Transition / output table

|  |  |  |
| --- | --- | --- |
| QBQCQD | QB\*QC\*QD\* | Z |
| 000 | 001 | 1 |
| 001 | 010 | 0 |
| 010 | 101 | 1 |
| 011 | 111 | 1 |
| 100 | 001 | 1 |
| 101 | 011 | 1 |
| 110 | 100 | 0 |
| 111 | 110 | 0 |

3. Output sequence is 0111001. （正确得3分）

**Appendix**

