RISC_PROCESSOR Project Status			
Project File:	processor_design.xise	**Parser Errors:**	No Errors
Module Name:	RISC_PROCESSOR	**Implementation State:**	Synthesized
Target Device:	xc4vfx12-12sf363	• **Errors:**	X 2 Errors (2 new)
Product Version:	ISE 14.7	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Di. Sep 8 03:49:34 2015	X 2 Errors (2 new)	0	0
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports [-]		
Report Name	**Status**	**Generated**
ISIM Simulator Log	Out of Date	Mo. Sep 7 18:33:54 2015

Date Generated: 09/08/2015 - 03:59:32