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EE446 Experiment 4 Preliminary Work

1. Datapath

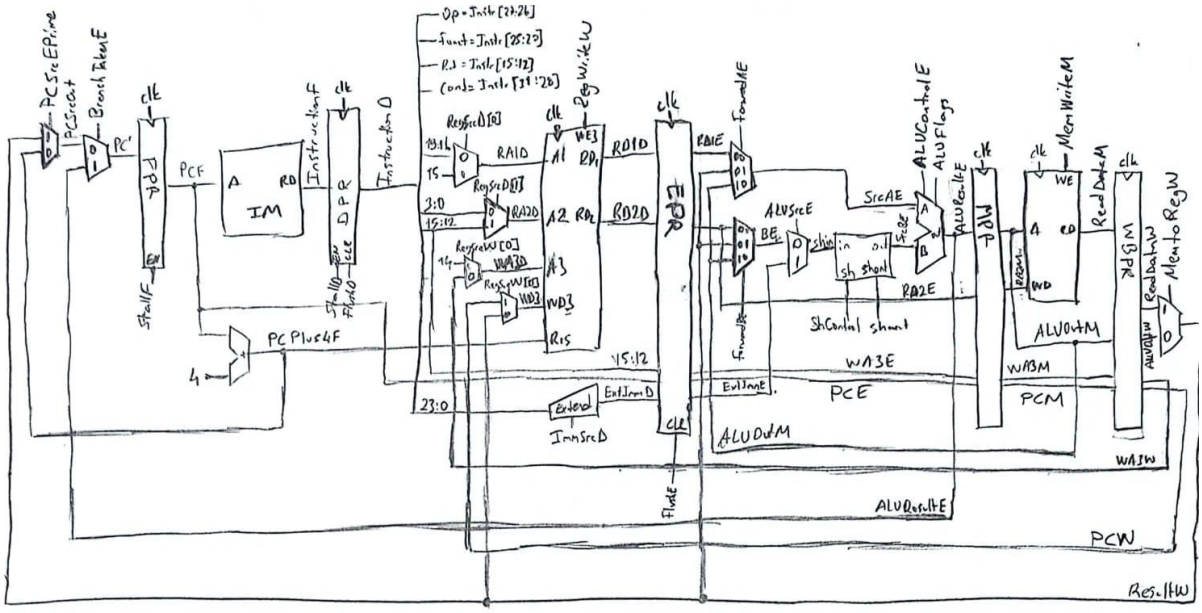

Figure 1. Updated datapath, control signals and connections.

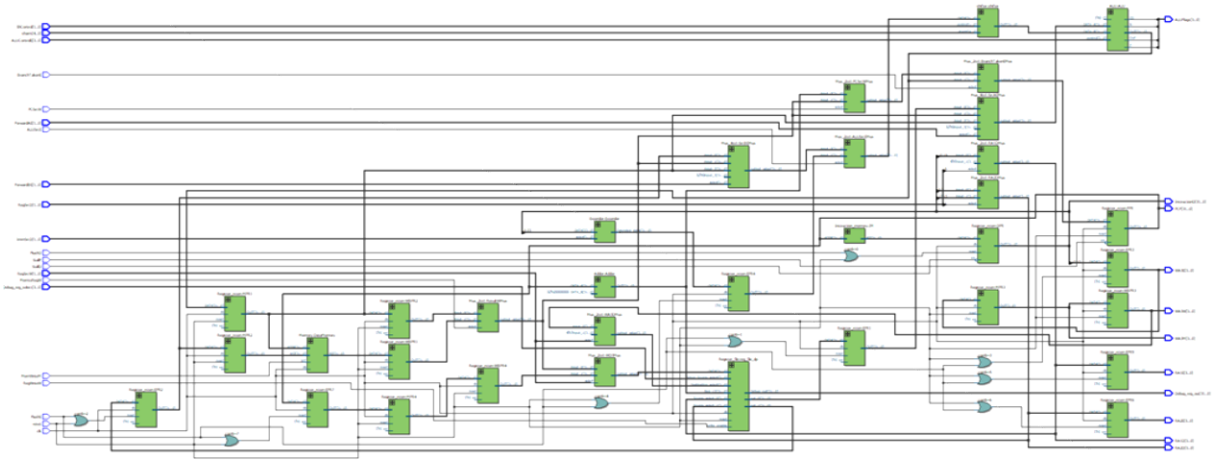

Figure 2. Datapath RTL view.

I put the shifter right before the ALU source B so that it can shift both register content and extended immediate. For BL operation I added two more muxes to the A3 and WD3 inputs of the register file. These muxes choose 14 for A3 and PC+4 value for WD3 when BL operation is in the writeback cycle.

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2. Controller

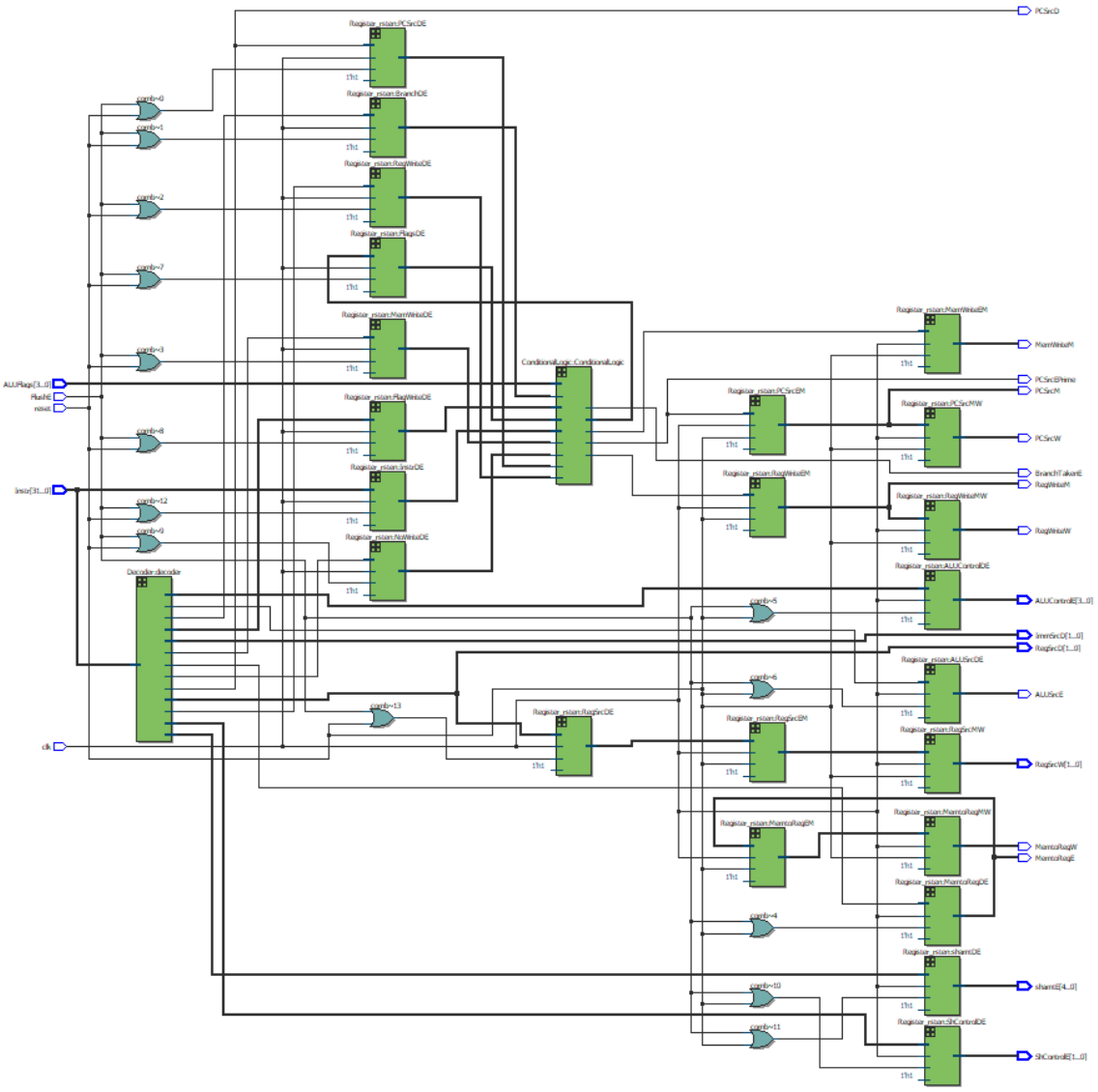

Figure 3. Controller RTL view.

In controller, I added shifter control and shamt signals which take its value from the instruction when there is a data processing operation for the shifter. For MOV operation ALU control signal is extended to 4 bits to encode MOV operation as well. For BL operation RegSrc signal is passed through the pipeline registers to give the correct signal when there is the BL operation is in the writeback stage. Also, PC+4 wire in the datapath is passed through the pipeline registers to give the correct value of PC in writeback stage of the BL operation. For BX no more adjustment is needed as MOV operation for Source B of the ALU is already implemented.

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3. Hazard Unit

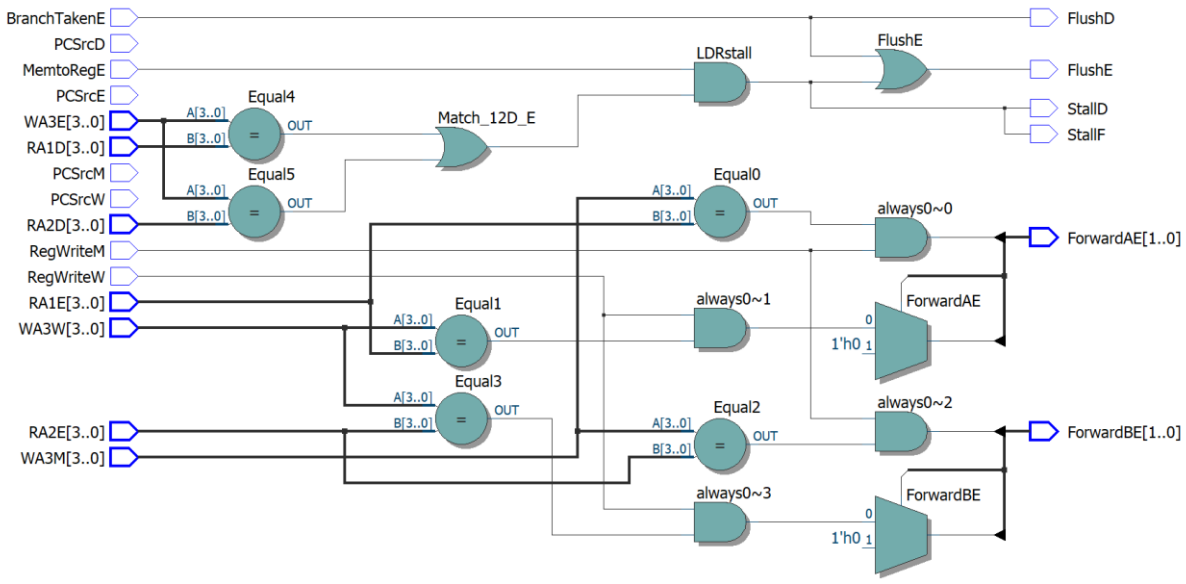

Figure 4. Hazard unit RTL view.

I designed the hazard unit as described in the lecture notes. This unit takes care of data hazards with Forward AE and Forward BE control signals for the muxes in the datapath. Stall and Flush signals for pipeline registers for LDR operation. Also, for Branch operations flush and stall signals are used.

4. Testbench

```
************ Performance Model / DUT Data  **************
PC:0x-1          PC:0x54
Register:0: 0x330        0x330
Register:1: 0x13         0x13
Register:2: 0x26         0x26
Register:3: 0x2          0x2
Register:4: 0x4c         0x4c
Register:5: 0xa          0xa
Register:6: 0x80000002   0x80000002
Register:7: 0xfffffff8   0xfffffff8
Register:8: 0x26         0x26
Register:9: 0x0          0x0
Register:10: 0x0         0x0
Register:11: 0x0         0x0
Register:12: 0x0         0x0
Register:13: 0x0         0x0
Register:14: 0x40        0x40
Register:15: Not checked         0x58
Pipeline_test passed
*******************************************************************************
** TEST                          STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
*******************************************************************************
** Pipeline_Test.Pipeline_test     PASS      297000.00          2.43     122172.39  **
*******************************************************************************
** TESTS=1 PASS=1 FAIL=0 SKIP=0             297000.00          2.72     109298.71  **
*******************************************************************************
```

Figure 5. Testbench results.