

EE446 Experiment 2 Preliminary Work

1. Datapath

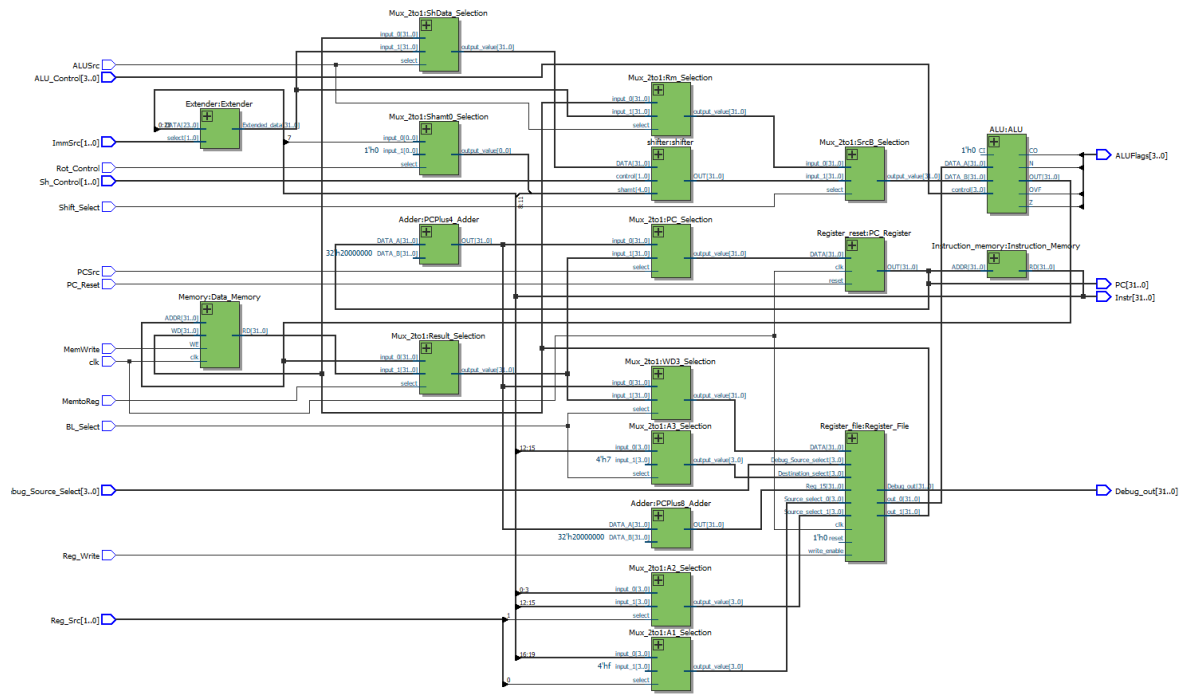


Figure 1. Datapath RTL View.

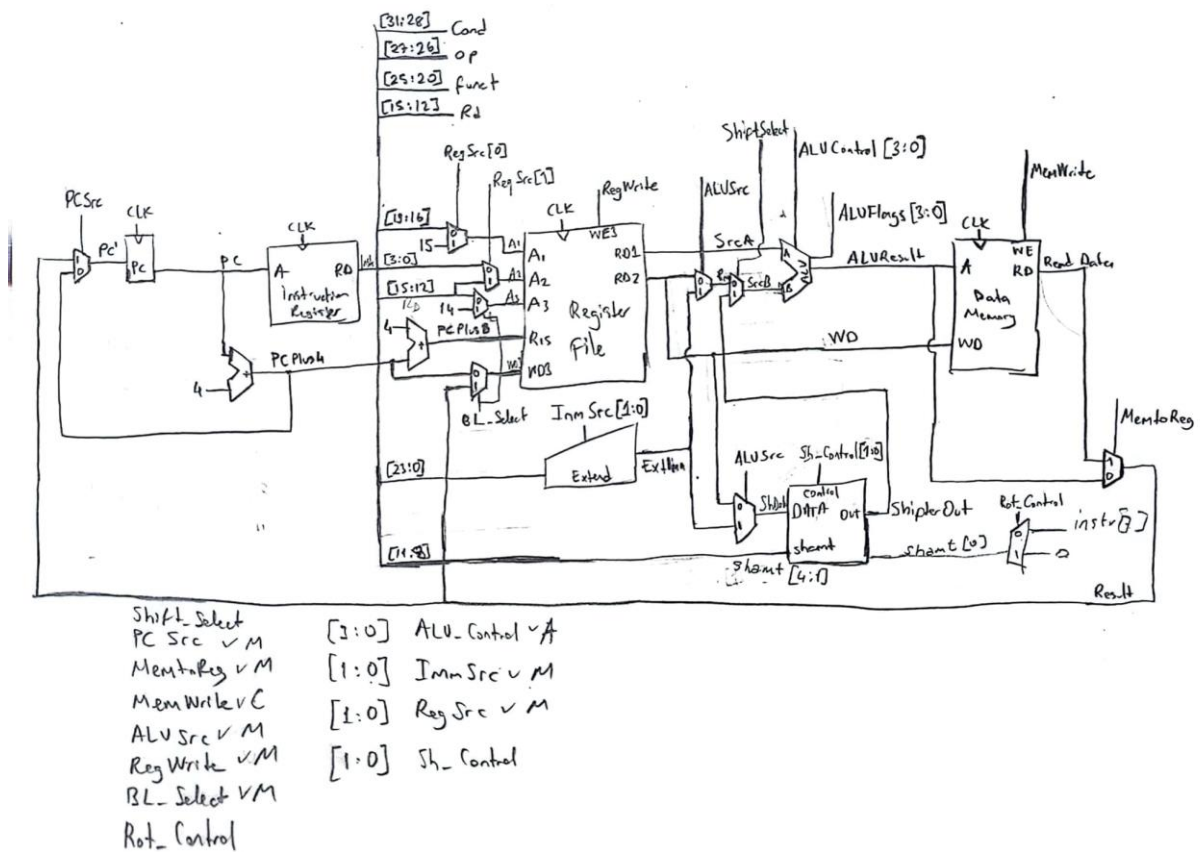


Figure 2. Extended datapath.

This is my expanded datapath to cover shifted register operations and BL and BX operations.

2. Controller

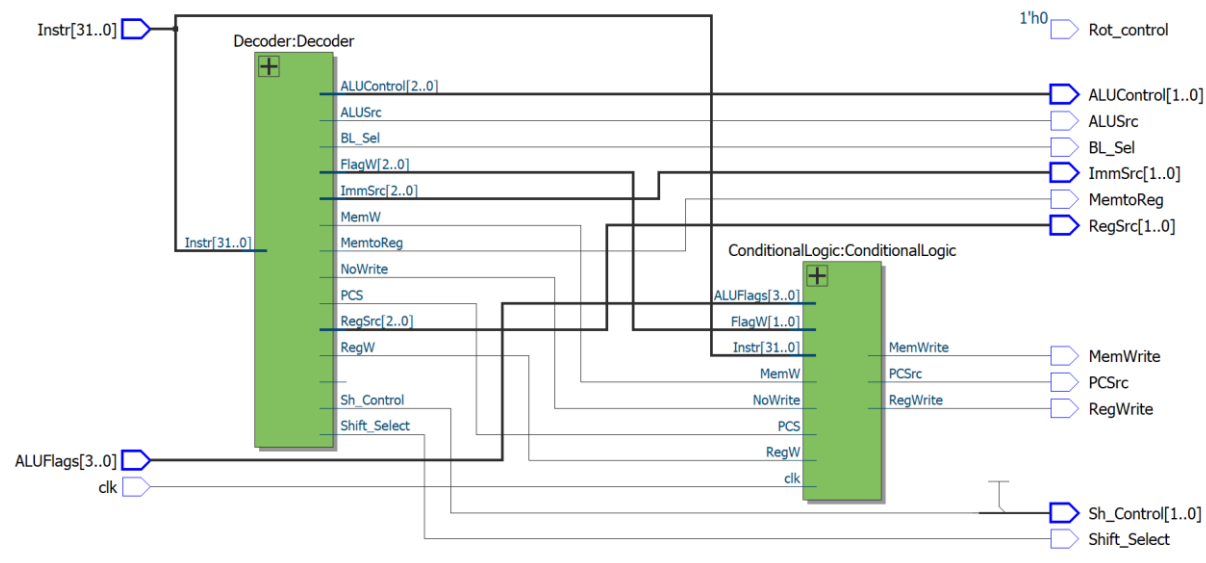


Figure 3. RTL View of controller.

I added Muxes and a combinational shifter to my datapath and their corresponding control signals are created in the controller.

3. Testbench

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Single_cycle_test failed
Traceback (most recent call last):
  File "C:\Users\Msi\OneDrive\Masaüstü\EE446_Exp2\Single_Cycle_Test\Test\Single_Cycle_Test.py", line 185, in Single_cycle_test
    tb = TB(instruction_lines,dut, dut.FetchPC, dut.datapath.Register_File)
          ^^^^^^^^^^^^^^^
  File "C:\Users\Msi\anaconda3\Lib\site-packages\cocotb\handle.py", line 363, in __getattr__
    handle = self.__get_sub_handle_by_name(name)
             ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^
  File "C:\Users\Msi\anaconda3\Lib\site-packages\cocotb\handle.py", line 321, in __get_sub_handle_by_name
    sub_handle = SimHandle(new_handle, self._child_path(name))
             ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^
  File "C:\Users\Msi\anaconda3\Lib\site-packages\cocotb\handle.py", line 1173, in SimHandle
    obj = _type2cls[t](handle, path)
          ^^^^^^^^^^^^^^^^^^^^^^^
  File "C:\Users\Msi\anaconda3\Lib\site-packages\cocotb\handle.py", line 226, in __init__
    SimHandleBase.__init__(self, handle, path)
  File "C:\Users\Msi\anaconda3\Lib\site-packages\cocotb\handle.py", line 130, in __init__
    self._def_file: str = self._handle.get_definition_file()
                          ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^
UnicodeDecodeError: 'utf-8' codec can't decode byte 0xfc in position 26: invalid start byte

** TEST                                STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
** Single_Cycle_Test.Single_cycle_test  FAIL      11000.00      0.00          inf **
** TESTS=1 PASS=0 FAIL=1 SKIP=0         11000.00      0.17        64013.94 **

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Figure 4. Testbench screenshot.

I tried to run my design in the testbench and I couldn't manage to run the test for a reason I couldn't solve. I don't have enough time to correct it therefore I will try to show it in the laboratory session if I get eligible to attend.