## 18 FIT Address Man

		<b>3.</b> □	اج	ξ			T	A																	Ī		٥	9	e				Т	Γ		ì				
lŀ	1		LED Stby	swR									AR OR				HR measur. period							Drec			PunMode	RunMode	RunMode						1 0					
lŀ	2	P2			sion	sion							H				R measu								Page#	-	2 orrF	-	errF	rage#		4	g g	te	2					
lŀ	4	V UP	TPE	rstTp	CFPGA-Revision	FPGA8-Kevision					inter		I				Ì			02047	200			12:5]	ľ	-	4 3	hPg	hPg			ADC: A hyte	C B by	ADC_C byte	4 3	Ī	5	or t error	BoardID error unlock phase 10MHz	aring
lŀ	2	ABFW		rs	CFP	FP					write pointe	pattern	GAP Length	D						PostTriggerTime 02047	Set Value 0 +0 Gain Channel 1		ľ	Seconds[12 : 5]		1 }	2 2	hCir	i		el i)	١	1	ΑΓ	ADCsample(i)	power error	statistics erro PLLs error	QDR DLL error QDR self-test error	BoardID error unlock phase	HistPage clearing
	9	ABHW					1.321	-		pled		- test	GAP Leng							stTrigg	Gain Ch	Measured Hit Rate Channel 1	(	နှ			9 074	hcD	hcD		Histgrm: FirstEntry (channel i				ADCsa 6	bowe	PLLs	98	Board	HistP
lŀ	8 2	Bsy A	•	re E	1	-	Board ID [47:32]			1' - ena		01	-	_						<u>ح</u> ا	5	Rate Ch			ŀ	1	8 D1	7	P1	(i laune	rstEntry	(i leur	$\frac{1}{1}$		8 7	# 12 to	P1/2 .	8 # ;	SNE UP	hClr .
ŀ	6	<u>ш</u>					Boar			abled,				Histogram: E_min			و					red Hit			ŀ	┨ ┞	6 6	+	P2	Energy (channel i)	grm: Fi	actual threshold (channel I)			6	<u> </u>	ōÀ	a a i	ຫ⊃	Ĕ
L	9				ion .	uoi		ask	rces	.0' - dis			Filter Length	stogran			zero						0			4 H	2 9	$\perp$	g	Ene	Hist	inresno			10	1		cess) ters	nked	
H	12 11	4			CFPGA-Version	FPGA8-Version		Interrupt Mask	Interrupt Sources	ement:	_		Filter	Ξ	tions	Je			Si	_	+		Test Pattern		F	4 6	12 0F	a	ØE			actual			2 11	routine	nable n	busy flag (for long access) reset Test Pulse pointers	load gains now wrong AB interface linked	de
<b> </b> -	13				CFPC	PPG.		Inter	Interru	Measur	FF AF	- 0			munica	tualTin	(5)	sec)	change				Test	.24.01	+			lags	lags						res res 13 12	start self-test routine	test pattern enable set interrupt on	lag (for est Pul	load gains now wrong AB interf	histogram mode
	14						0			Hit Rate Measurement : '0' - disabled, '1' - enabled	4	"00" - normal	- alway		of Com	To / Ac	as (in se	ime (in	of page					SubSeconds[24:0]			14 mntv' f	mpty'	empty'						14 r	start s	set inte	busy f reset T	load g wrong	histog
==	3 15			†		15.4	Board ID [31:0]			Ī		00	_		32bit access Register for Test of Communications	Second Counter: SetTimeTo / ActualTime	set HistormMeasTime (in sec)	get HistgrmRecordTime (in sec)	Histogram: number of page changes					Shirks			15	Histogram: 'page not empty' flags	Histogram: 'page not empty' flags						PT 3 15		٠،	 	, , m	٠
	17 16	-	mode of operation	rstPg rPoint			Doard						18		gister f	nter: S	stormM	stgrmR	ram: nı			٥			F			am: pa	am: ˈbai						17 16	TS :	swR	Bsy rstTP	ABE	Σ
H	18	es	le of op	rst								<u>.</u>	5		ess Re	nd Cou		get His	Histog			H			F		Histogram	Histogra	Histogra	p					18					ite
	19	S									ır	LSBits[21:0]	7 (5) (7)		2bit acc	Seco	g perio							Q.	L		19			zero					19	1	Ē	control		overwr
ŀ	20	interrupt			uo.	uoi					read pointer	TS	Ě	Bin	37		HR sampling period							Channel Map	L		70								(i+1)	ADC run	QUR RAIN overflow	max. increment/decrement value for hitrate control	ticks	FIFObehaviour: '1'- stop when overflow, '0'- overwrite
- 1-	22 21	-			Doc Revision	Doc Revision				H	read			Histogram: E_Bin			£ E						i	Cha	ŀ		22 21				annel i	prev. A			ADCsample(i+1)	4.		lue for	n 50ns	overflo
- 1	23				۱۵	ရိ				H			١_												F		-	, ved	,ved		ntry (ch				ADC 23	AR S	ŠŠ	nent va	ength i	p when
- 1-	24	EF	StFF										reserved			l							rep		L	+	24 23	reserved	reserved		grm: LastEntry (channel i)	<del>sign</del>			24			/decren	trigger	1'- sto
ŀ	26 25	. AE					SlofiD		SlotID	_															F	$\perp$	26 25			zero	Histgrm				26 25			rement	d max.	aviour
H	27 2	FF AF					Į,	5	SIC	_													-	-	t	-	27 2				-				27   2			nax. inc	xpecte	FIFObehaviour: '1'-
H	28	hPg F		ŀ							EF			ΣH										4 · 01			28	T	1						28	n n	trigger run statistic run		,	
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ŀ	31 30	irq	4	4	<u>.</u>	2	creok	5	0	-			-	_									4	ď	}	-	31   30								эт тс 31 30	1		DaltaMAX	HR sampl. time	peh
	(7)	=		swTr	1					ė			$\dagger$				τ.	9 0			1	H	1				(2)	H		1		+	$\dagger$		PT 3	E:	s S	۵	生	peh
Description		tatus	ettings	إ	ersion	ersion	iower 32011S 01 40	50: 15		enables HR meas.	entFIFO	of the	Hinds	ttings			HR MeasParam. Histor MeasPeriod	Histgr: MeasPeriod	mber	tooff.	) I Sell	ate	ģ		<u>a</u>	<u>e</u>	afric	atus	atus	adister	ast&First Entries	IS Ped	Red	l Reg	k data					
Desc		Module Status	Module Settings	Command	CFPGA Version	FPGA8 Version	lower Szbits of 46			ables F	status EventFIFO	Behavior of the	lobal Se	Global Settings	R/W 32bit		HR MeasParam Histor: MeasPeri	stgr:Me	Histgr:Number	tooffo a ommoo	indiv. gain	indiv. hit rate	pattern seq		per channel	per channel	periph Status	periph. Status	periph. Status	Fage Count Energy Register	ast&Firs	Inresholds	ADC - SPI Red	ADC - SPI Reg	ADC track data			ting 1		
iAdd		0×00×0		_	_		600x0		0×008		0x00B sta	0x00C Be	OXOOE G	0x00F		_	0x012 HF		0x015 Hi	0x016		П		0x200	т		0000			0x003		0x020			0x000 A[			Status bits cleared by writting 1		
		0			0								35			0					0	П			Τ		څ	0	0		rst		Т				~	cleare		
Name		tus	Control	Command	Version	pversion	Boardin MSB	IntMask	IntRequest	hrMeasEnable	eventFIFOstat	PixelSettings1	RunControl	HistgrSettings	AccessTest	SecTimer	hrControl HistMeasTime	HistRecTime	HistNofMeas	PostTrigTime	ın in	HitRate	TestPattern	eventFIFO1	eventFIF03	eventFIF04	nStatus A	pStatusB	pStatusC	Fagen	HistLastFirst	Inreshold	ADCsettingsB	<b>ADCsettingsC</b>	RAMdata	Read only	Read Write	tus bits	Write only	
Address		000 Status				0x000010 pve					0x00002C eve	0x000030 Pix	_				0x000048 hrc		0x000054 His	0x000058 Pos		П		0x001800 eve			0000000			0x00200C Fac		0x002080 Inc			0x003000 RA	Re	Re	Sta	W	
	PC	0x000000	ŏ	0x000008	ğ	ğ	ğlä		lğ	18	18		SIS	Iğ	lg	ĕ	ĕlē	S	ĕ	힑	315	اجًا	13	3 2	:[2	31	15	20	ž		22	žIŠ	ļĮŽ	504	iğl					

expected max. trigger length in 50ns ticks
FIFObehaviour: '1'. stop when overflow, '0'. overwrite
AB hardware code
code of compiled AB-interface

bits cleared after read-out KATRIN specific fields