Majorana Digitizer Specification and Implementation

A Modification of the LBNL GRETINA Digitizer

Version 0.1

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I. Introduction

The purpose of this document is to specify the firmware modifications of the LBNL GRETINA – 10 Channel Digitizer to meet the requirements of the MAJORANA Neutrinoless Double-beta Decay Experiment.

II. Digitizer Overview

The MAJORANA Digitizer will be a modification of the GRETINA – 10 Channel Digitizer. The base specifications are listed in Table 1: GRETINA 10 Ch. Digitizer base specification. The modifications specified in this document are limited to firmware changes.

Table 1: GRETINA 10 Ch. Digitizer base specification.

Property	Value	Unit
Input Range (CH 9)	9.2	Vpp
Input Range (CH 0-8)	2.9	Vpp
Bandwidth	50	MHz
Sample Rate	100	MHz
Input Impedance	95	Ohms
Resolution	14	bit
VME Bandwidth	40	MB/s
FIFO Depth	1	MB
FPGA Block RAM	240	kB

An overview of the MAJORANA Digitizer is shown in Figure 1: MAJORANA Digitizer Overview. The channels of the digitizer board will be divided into low-gain high-energy and high-energy low-gain channels. There will be five of each channel. All channel requirements will be implemented with identical firmware architecture and differentiated through software configuration.

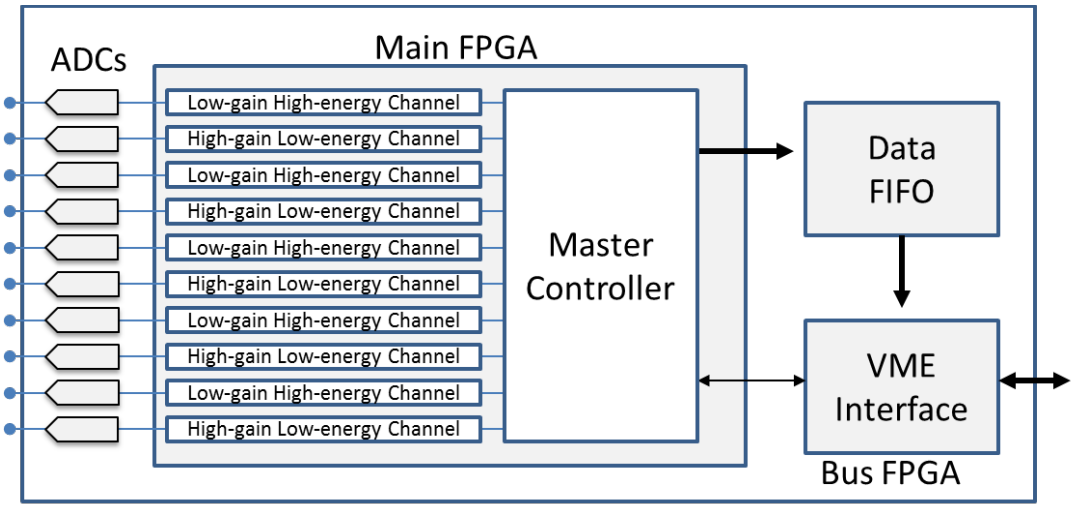

Figure 1: MAJORANA Digitizer Overview

III. MAJORANA Signals

An illustration of the MAJORANA signal with an overlay of the Raw Data Window regions is shown in Figure 2: MAJORANA Channel Signal. The first and last regions are the Base Line and Flat Top respectively, these regions are low bandwidth. The middle region is the Rising Edge which is used for triggering and is high bandwidth. To maximize the capacity of the Raw Data Window the two low bandwidth regions will be pre-summed (down sampled).

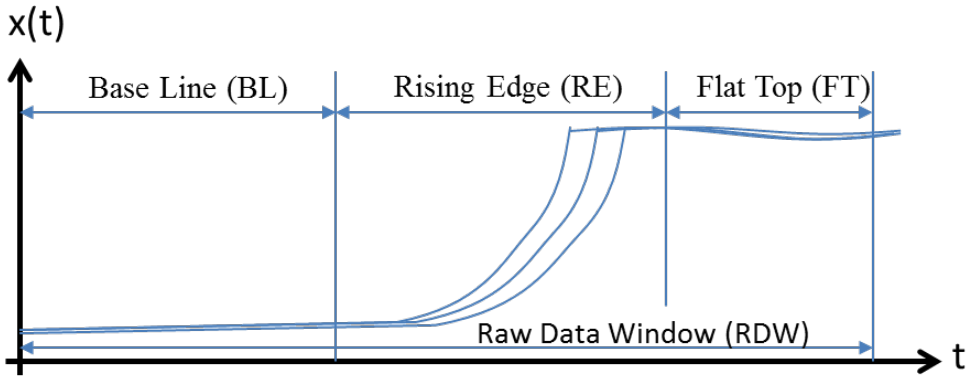

Figure 2: MAJORANA Channel Signal

IV. Digitizer Channel Architecture

The MAJORANA digitizer firmware architecture common to all channels is shown in Figure 3: Channel Architecture. Data sampled from the external 14 bit analog-to-digital converter enters the channel and passes through a series of four filter tap delays. The first tap delay is used for the leading edge detector. The next three tap delays are used for the trapezoidal filter. After the tap delay chain the data passes through the Pre-Sum Select block and is stored in a circular buffer.

The two new blocks that have been added to the base GRETINA channel are Trigger Controller and Pre-sum Select.

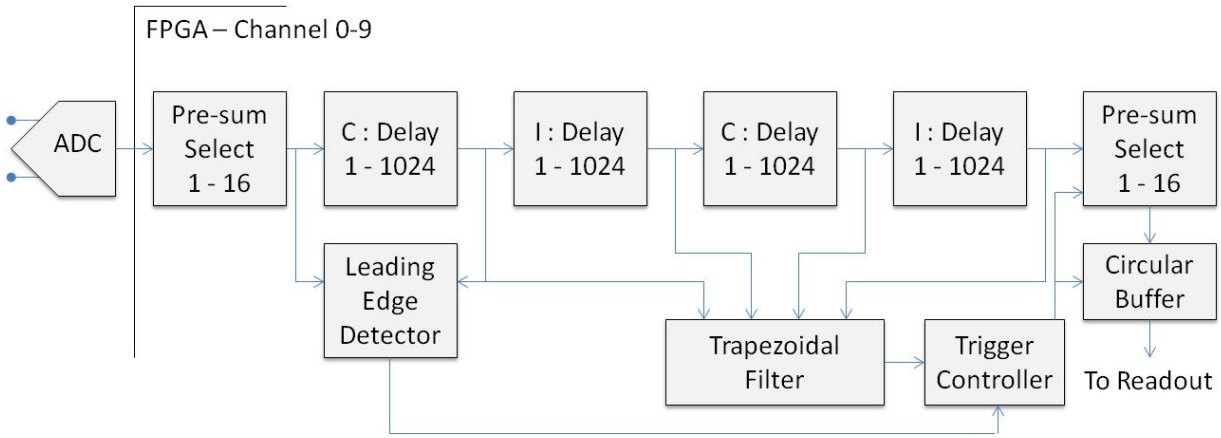

Figure 3: Channel Architecture

The Pre-sum Select block allows the captured raw data window to be increased through region selectable down sampling with a rectangular window anti-aliasing filter. The down sample rate will range from 1 to 16 by powers of two. The anti-aliasing filter will be implemented with software selectable down shift after accumulation.

The Trigger Controller block synchronizes the Pre-sum Select block with the rest of the channel and triggers readout of the circular buffer. A timing diagram for the Trigger Controller block is shown in Figure 4: Channel Timing. The channel may be triggered off a Leading Edge Detector or Trapezoidal Filter threshold. The selection of trigger mode will be software selectable. Prior to a trigger event data is continually pre-summed and written to the circular buffer. When a trigger event occurs the pre-sum is disabled after a delay of TRG samples and data is written to the circular buffer at the full sample rate. After RE samples the pre-sum is re-enabled and FT samples are written to the circular buffer. Once written the last RDW samples of the buffer are readout over the VME bus. After readout of the channel is complete the pre-sum is re-enabled and the trigger re-armed after the circular buffer is refilled with a minimum of BL samples. Definitions of the timing constants are given in Table 2: Definition of Timing Constants.

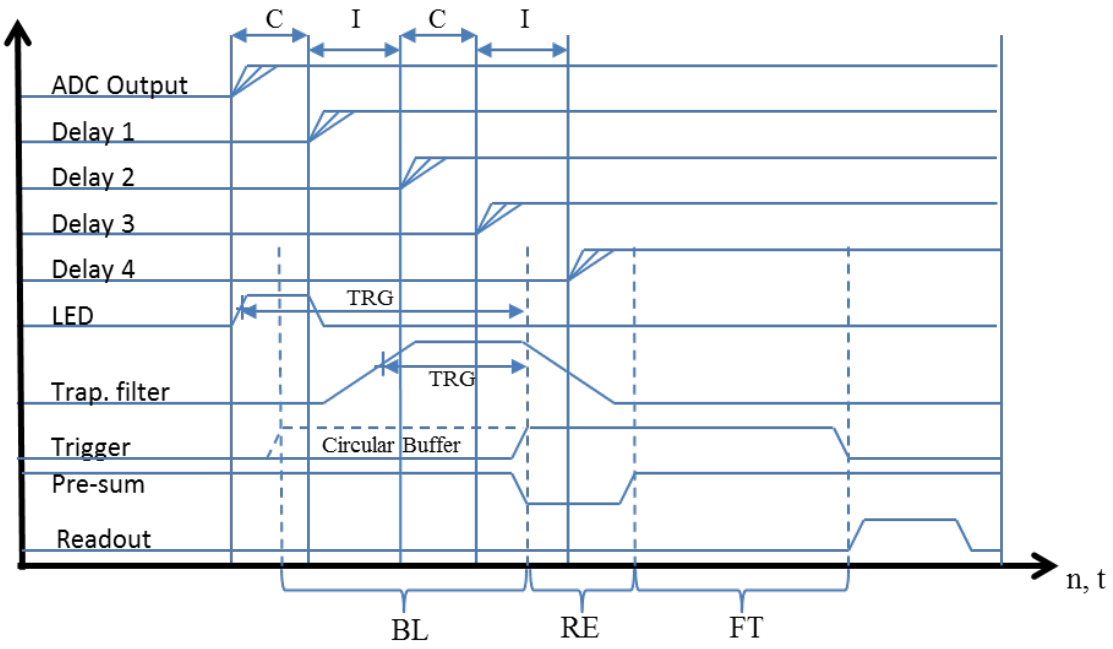

Figure 4: Channel Timing

Table 2: Definition of Timing Constants

Constant	Min	Max	Constraints	Description
I	1	1024		Tap delay for trapezoidal filter.
C	1	1024		Tap delay for Trapezoidal Filter and Leading Edge Detector.
BL	1	1024		Base Line region length of Raw Data Window.
RE	1	1024		Rising Edge region length of Raw Data Window.
FT	1	1024	FT < RDW - BL - RE	Flat Top region length of Raw Data Window.
RDW	TBD	2048	RDW = BL + RE + FT	Raw Data Window length captured in Circular Buffer.
TRG	1	1024		Delay between a trigger event and the start of Rising Edge.

V. Implementation

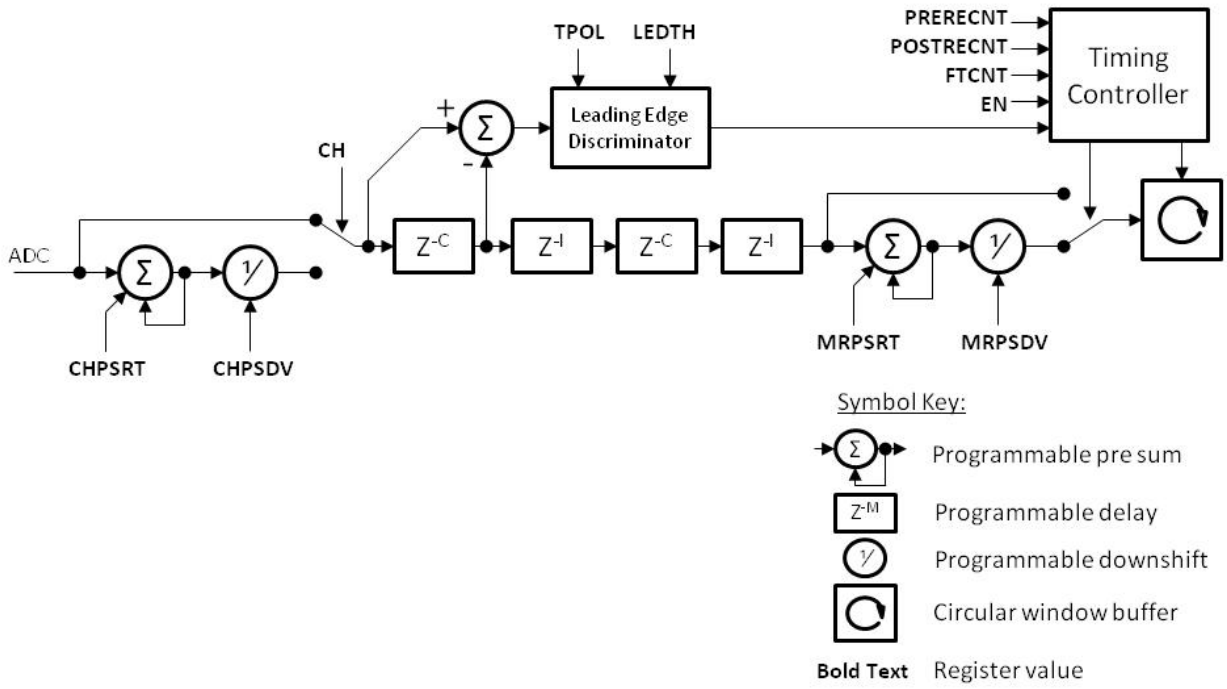

Figure 5: FPGA Channel Architecture.

A. Register Map

Channel Register Map

Window Timing Register

Address: 0x100 + Channel Number x 4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					FTCNT											MRPSRT				MRPSDV				CHPSRT				CHPSDV			

✓

Rising Edge Window Register

Address: 0x140 + Channel Number x 4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									PRERECNT												POSTRECNT										

Status Register

Address: 0x40 + Channel Number x 4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																				TPOL									CH		EN

LED Threshold

Address: 0x80 + Channel Number x 4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															LEDTH																

VME FPGA Register Map

Clock MUX Register

Address: 0x10

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																															CMUX

FTCNT: Flat Top Window Counter Value
Size: 11 bits
Default Value: 256
Description: Internal counter value used to calculate the size of the Flat Top Window.

MRPSRT: Multi-rate Pre-sum Rate Value
Size: 4 bits
Default Value: 0
Description: Selects the number of samples to pre-sum in the Baseline and Flat Top Windows for a channel. This divides the sample rate accordingly.

0: Sum 2 samples.
1: Sum 4 samples.
2: Sum 8 samples.
3: Sum 10 samples.

MRPSDV: Multi-rate Pre-sum Divider Value
Size: 4 bits
Default Value: 0
Description: Selects the divider used after the multi-rate pre-sum.
0: Divide by 1.
1: Divide by 2.
2: Divide by 4.
3: Divide by 8.

CHPSRT: Channel Pre-sum Rate Value
Size: 4 bits
Default Value: 0
Description: Selects the number of samples to pre-sum at the front of a channel. This divides the sample rate accordingly.
0: Sum 2 samples.
1: Sum 4 samples.
2: Sum 8 samples.
3: Sum 10 samples.

CHPSDV: Channel Pre-sum Divider Value
Size: 4 bits
Default Value: 0
Description: Selects the divider used after the pre-sum at the front of a channel.
0: Divide by 1.
1: Divide by 2.
2: Divide by 4.
3: Divide by 8.

PRERECNT: Pre Rising Edge Window Counter Value
Size: 11 bits
Default Value: 512
Description: Internal counter value used to calculate the size of the Pre Rising Edge Window.

POSTRECNT: Post Rising Edge Window Counter Value
Size: 11 bits
Default Value: 512
Description: Internal counter value used to calculate the size of the Post Rising Edge Window.

TPOL: Leading Edge Discriminator Threshold Polarity

Size: 2 bits
Default Value: 0
Description: Selects the polarity of s channels discriminator. 0 : None, 1: Positive, 2: Negative, 3: Both.

CH: Channel Pre-sum Enable
Size: 1 bit
Default Value: 0
Description: Enables the pre-sum block at the front of an individual channel.

EN: Channel Enable
Size: 1 bit
Default Value: 0
Description: Channel enable bit. 1 : Enable, 2: Disable.

LEDTH: Leading Edge Discriminator Threshold Value
Size: 17 bits
Default Value: Maximum
Description: This is the discriminator threshold used by an individual channel.

CMUX: Clock Multiplexer
Size: 2 bits
Default Value: 0
Description: This register selects the clock source used in the Main FPGA.
0 : Front panel clock.
1: Onboard crystal oscillator.

B. Data Format

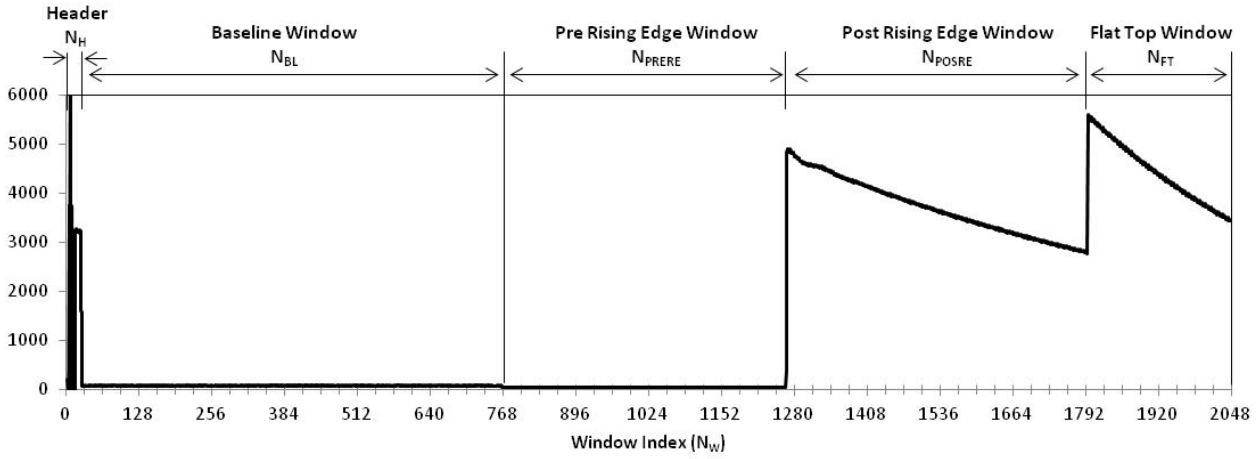

Figure 6: Data Window Format Description.

Table 3: Data Window Format Description

Parameter	Name	Size (16 Bit words)	Start Index (16 Bit words)
N_W	Window Size	2048	0
N_H	Header Size	29	0
N_{BL}	Baseline Size	2018 - (**PRERECNT** + **POSTRECNT** + **FTCNT**)	29
N_{PRERE}	Pre Rising Edge Window	**PRERECNT** - 13	29 + N_{BL}
N_{POSRE}	Post Rising Edge Window	**POSTRECNT** + 18	29 + N_{BL} + N_{PRERE}
N_{FT}	Flat Top Window	**FTCNT** - 4	29 + N_{BL} + N_{PRERE} + N_{POSRE}

Table 4: Header Description

Index	Value
0-1	0xAAAA_AAAA
2	Board ID
3	0x0000
4-6	LED Timestamp
7-8	Energy
9-11	CFD Timestamp
12	CFD 1 L
13	CFD 1 H
14	CFD 2 L
15	CFD 2 H
16-28	Reserved

C. Example Configuration

Below is the register configuration sequence used to capture the data shown in Figure 6.

VME FPGA Register: x10:

CMUX = 1 : Select the on-board crystal oscillator in the clock multiplexer.

Main FPGA Registers: x100, x104, x108, and x10C (Channels 0, 1, 2, and 3)
FTCNT = 256 : Capture 252 samples in the Flat Top Window.
MRPSRT = 0 : Pre-sum every two samples during Baseline and Flat Top Windows.
MRPSDV = 0 : Divide the pre-sum output by 1 during Baseline and Flat Top Windows.
CHPSRT = NA : Channel pre-sum disabled with CH = 0.
CHPSDV = NA : Channel pre-sum disabled with CH = 0.

Main FPGA Registers: x140, x144, x148, and x14C (Channels 0, 1, 2, and 3)
PRERECNT = 512 : Capture 499 samples in the Pre Rising Edge Window.
POSTRECNT = 512 : Capture 530 samples in the Post Rising Edge Window.
Note: The size of the Baseline window is then calculated to be 738 Samples (2048 – 29 – 499 – 530 – 252).

Main FPGA Registers: x80, x84, x88, and x8C (Channels 0, 1, 2, and 3)
LEDTH = x800 : This threshold value was selected for compatibility with the pulser used in testing.

Main FPGA Registers: x40, x44, x48, and x4C (Channels 0, 1, 2, and 3)
CH = 0 : Disable channel pre-sum.
EN = 1 : Enable the channel.
TPOL = 1 : Trigger only on positive polarity pulses.