18. FLT Address Map

Address PCI	Name	iAdd	Description	Bit fields (31 … 0)
0x000000	Status	0x000	Module Status	irq[31]; interrupt sources; Bsy[8]; ABHW[7:6]; ABFW[5:4]; UP[3]; P2[2]; P1[1]; PF[0]
0x000004	Control	0x001	Module Settings	mode of operation; TPE[4]; LED[1]; Stby[0]
0x000008	Command	0x002	Command	swTr[31]; rstPg, iPoint [17:16]; rstTp[4]; swR[0]
0x00000C	Version	0x003	CFPGA Version	Project; Doc Revision; CFPGA-Revision
0x000010	pVersion	0x004	FPGA8 Version	Project; Doc Revision; FPGA8-Revision
0x000014	BoardID_LSB	0x005	lower 32bits of 48	Board ID [31:0]
0x000018	BoardID_MSB	0x006	upper bits [47:32]	Board ID [47:32]
0x00001C	IntMask	0x007	Interrupt Mask	Interrupt Mask
0x000020	IntRequest	0x008	Interrupt Request	Interrupt Sources
0x000024	hrMeasEnable	0x009	enables HR meas.	Hit Rate Measurement : '0' - disabled, '1' - enabled
0x00002C	eventFIFOstat	0x00B	status EventFIFO	EF[24]; FF[27]; AF[26]; AE[25]; hPg[28]; hClr[29]; read pointer; write pointer
0x000030	PixelSettings1	0x00C	Behavior of the	AE; EF; LSBits[21:0]; FF; AF; "00" - normal; "01" - test pattern
0x000034	PixelSettings2	0x00D	Pixel Trigger	MSBits[21:0]; "10" - always 0; "11" - always 1
0x000038	RunControl	0x00E	Global Settings	reserved; SF; Filter Length; GAP Length; TR; FR; QR
0x00003C	HistgrSettings	0x00F	Global Settings	Histogram: E_Bin; Histogram: E_min; AR
0x000040	AccessTest	0x010	R/W 32bit	CM; HM; 32bit access Register for Test of Communications
0x000044	SecTimer	0x011		Second Counter: SetTimeTo / ActualTime
0x000048	hrControl	0x012	HR MeasParam.	HR sampling period; HR measur. period
0x00004C	HistMeasTime	0x013	Histgr.MeasPeriod	set HistgrmMeasTime (in sec); zero
0x000050	HistRecTime	0x014	Histgr.MeasPeriod	get HistgrmRecordTime (in sec)
0x000054	HistNofMeas	0x015	Histgr.Number	Histogram: number of page changes
0x000058	PostTrigTime	0x016		PostTriggerTime 0…2047
0x001000	Offset	0x000	common offset	Offset value 0 …4095
0x001004	Gain	0x001	indiv. gain	Gain Channel 1
0x001100	HitRate	0x040	indiv. hit rate	Measured Hit Rate Channel 1
0x001400	TestPattern	0x100	pattern seq.	Ov; rep; Test Pattern 0
0x001800	eventFIFO1	0x200		Seconds[4 : 0]; Seconds[12 : 5]
0x001804	eventFIFO2	0x201		SubSeconds[24:0]; prec.
0x001808	eventFIFO3	0x202	per channel	Channel Map; Page#
0x00180C	eventFIFO4	0x203	per channel	Energy; Page#
0x002000	pStatusA	0x000	periph. Status	0x0; reserved; Histogram: 'page not empty' flags; QE QD P2 P1; hcD hClr hPg; errF; RunMode
0x012000	pStatusB	0x000	periph. Status	0x1; reserved; Histogram: 'page not empty' flags; QE QD P2 P1; hcD hClr hPg; errF; RunMode
0x052000	pStatusC	0x000	periph. Status	0x2; reserved; Histogram: 'page not empty' flags; QE QD P2 P1; hcD hClr hPg; errF; RunMode
0x00200C	PageN	0x003	Page Count	zero; Page#
0x002040	Energy	0x010	Energy Register	zero; Energy (channel i)
0x002044	HistLastFirst	0x011	Last&First Entries	Histgrm: LastEntry (channel i); Histgrm: FirstEntry (channel i)
0x002080	Threshold	0x020	Thresholds	sign; prev. A; actual threshold (channel i)
0x000400	ADCsettingsA	0x000	ADC - SPI Reg	ADC_A byte
0x010400	ADCsettingsB	0x000	ADC - SPI Reg	ADC_B byte
0x050400	ADCsettingsC	0x000	ADC - SPI Reg	ADC_C byte
0x003000	RAMdata	0x000	ADC track data	PT; TC; res; res; ADCsample(i+1); ADCsample(i)

Legend

Colour coding:
- Read only
- Read Write
- Status bits cleared by writing 1
- Write only
- bits cleared after read-out
- KATRIN specific fields

FR – filter run	AR – ADC run	ST – start self-test routine	PE – power error
TR – trigger run	QR – QDR RAM run	TE – test pattern enable	SE – statistics error
SR – statistic run	Ov – overflow	swR – set interrupt on	P1/2 – PLLs error
		Bsy – busy flag (for long access)	QD – QDR DLL error
DaltaMAX – max. increment/decrement value for hitrate control		rstTP – reset Test Pulse pointers	QE – QDR self-test error
		LG – load gains now	SNE – BoardID error
HR sampl. time – expected max. trigger length in 50ns ticks		ABE – wrong AB interface linked	UP – unlock phase 10MHz
beh – FIFObehaviour: "1"- stop when overflow, "0"- overwrite		HM – histogram mode	hClr – HistPage clearing
ABHW – AB hardware code		StFF – stop when full	hcD – HistPage cleared
– code of compiled AB-interface			