3-Phase Inverter for Electric Powered Cessna-172

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1 Project Description

The goal of this project was to design an efficient three phase inverter capable of driving an electric powered Cessna-172.

The key design goals were to be able to deliver the 80kW necessary for takeoff while maximizing efficiency and minimizing our total solution area. In order to do this we used emerging technologies such as SiC FETs and paid close attention to our component choice and design. We also thought about additional considerations outside the immediate scope of the project, which are detailed in the future directions section of this report.

Our design is capable of delivering 80kW to a balanced three phase resistive load, from an 870V DC bus. This bus voltage could be supplied from battery packs in conjunction with a DC-DC boost regulator (assuming our battery pack is similar to the 375V output from the packs used in Tesla automobiles).

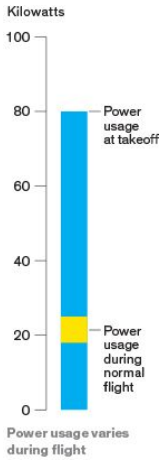


Figure 1. Cessna-172 Power Requirements

2 Background

Electric aircraft propulsion is a uniquely challenging problem. Not only are the power requirements very high, but it is an application which is extremely weight, size, and safety sensitive. Additionally, operation at high altitude and temperature extremes further complicates designing for an aerospace environment. It is also an emerging area of research and interest, meaning there is not a great wealth of resources available to consult and many of the problems posed by the application are yet to be entirely solved. However, emerging technologies such as SiC MOSFETs hold great promise in helping to solve some of these challenges.

For the power rating necessary for our design, the only traditional choice would be to use silicon IGBTs. SiC FETs have the advantage over Si IGBTs in that they have much lower conduction and switching losses, while being able to support similar Drain-Source Voltages and currents. Since high efficiency is a stated design goal for us, using SiC devices was a natural choice. SiC devices also have the advantage of being operable at higher junction temperatures than Si devices, a useful characteristic for an inverter which may be sitting in the same compartment as the motor which it is driving.

As with any power transistor, gate drive design is also an important consideration. Some of the design choices involved with this are discussed further in the Proposed Design Section.

It was also important that we carefully select our switching frequency and dead time in order to maximize efficiency. Dead time is defined as the time between the active transistor switching off, and the inactive transistor switching on in one arm of the inverter. It is important to incorporate dead time in the

PWM control of the inverter in order to prevent a short circuit path from the DC power bus to ground, or "shoot through current". It is equally important to use the minimum dead time possible since this dead time is time where the inverter is not driving power to the load. Switching frequency is a balancing act between minimizing harmonics, maximizing efficiency, and preventing human audible humming.

3 Proposed Design

Our design is built around 3 half-bridge inverters with each arm phase shifted to create a 3-phase sinusoidal output. Each half-bridge inverter is composed of a high-side and a low-side switch. These switches are made out of 2 parallel SiC FETs with an antiparallel diode to prevent flyback. The choice to use two transistors in parallel for each switch was a result of not being able to find devices with a high enough current rating (and also a SPICE model). We chose Wolfspeed C3M0065090 N Channel devices for our application, since they supported 900V, and 35A. Perfect for our design.

While driving SiC MOSFETs is easier than IGBTs in many ways, it was still necessary to use a gate driver to supply the drive current for our switches. We used the LT4440 gate driver for this. This was a nice device to work with, since it provided the gate voltage we needed (15V) from a standard 5V digital logic input. It also required few external components, and was already modeled in LTSpice. This choice works in simulation only however, since the maximum Vin it can support is 80V (much lower than our 875V bus). We chose to use it anyway, since we could not find a publicly available model for a more suitable device. If this design were to be implemented in an actual system, this driver would need to change to something more robust.

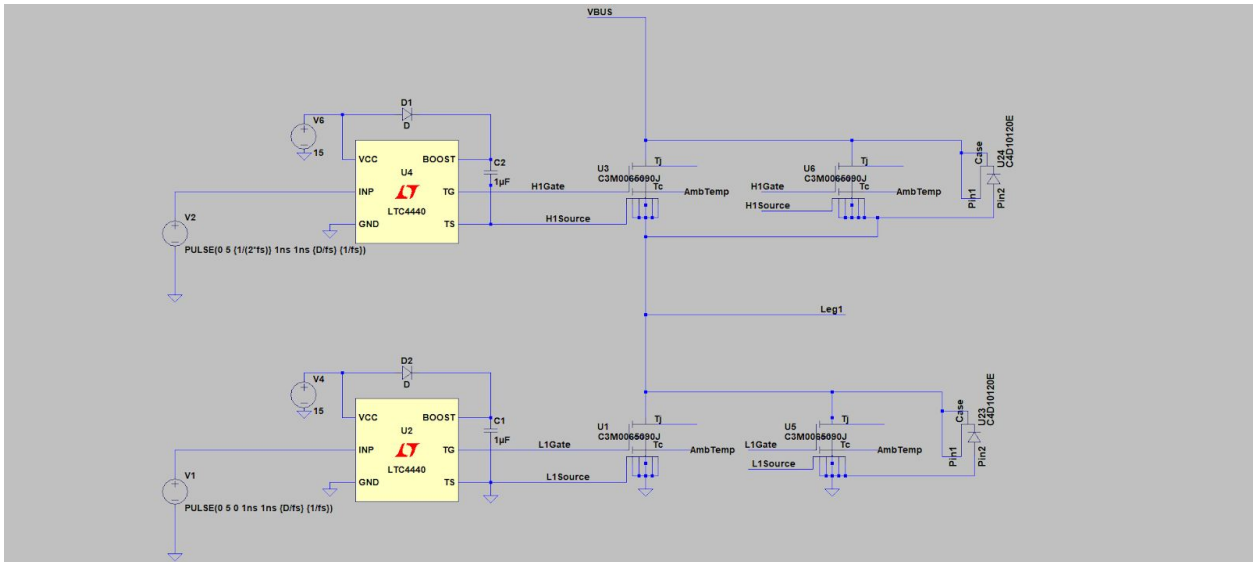


Figure 2. Single Half-Bridge Inverter Leg (1 of 3)

Another design consideration for the gate drive was the choice of bootstrap capacitance. This was selected based on maintaining gate drive to 1% given the total amount of charge lost due to gate charge (30nC per FET x 2 = 60nC) plus the amount of charge lost to the gate driver IC which was measured from simulation (shown below as the difference in diode and capacitor currents * ½ switching period):

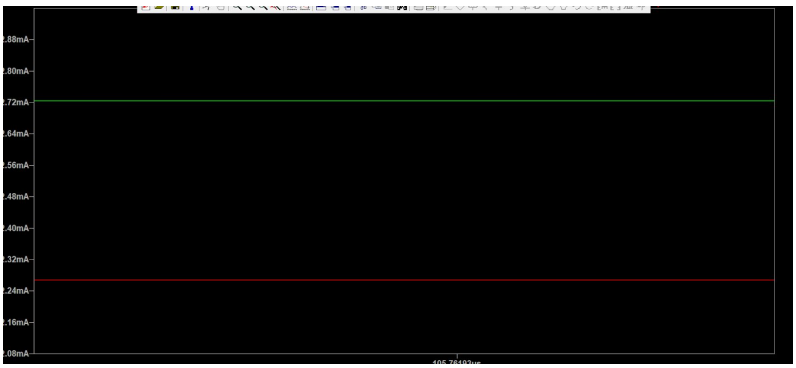
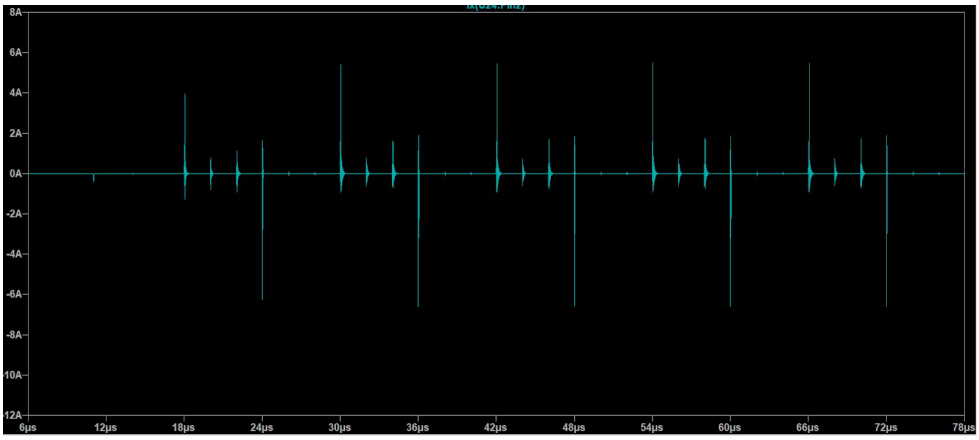


Figure 3. Gate Driver Bootstrap Current

This calculation yielded a capacitance of 406nC. 1uF was selected as a safe value.

Diode selection was based on measuring the max current through one of the switch diodes during switching transients. This was determined to be 6A max. We then selected the appropriate SiC diode from the Wolfspeed website. We chose to use C4D10120E. These models were then added to our LTSpice schematic and the max current was verified. The diode current is shown below:



The switching scheme for our design was designed to yield a 6 step output waveform (measured from one leg of the inverter to another). The relative voltages of each leg to each of the other legs produced three identical 6-step sinusoids, each phase shifted 120 degrees. This switching scheme necessitated flipping one "switch" (composed of 2 FETs each) every 1/6th of a period (while incorporating the necessary dead time). The ground referenced output voltages of each leg are shown below:

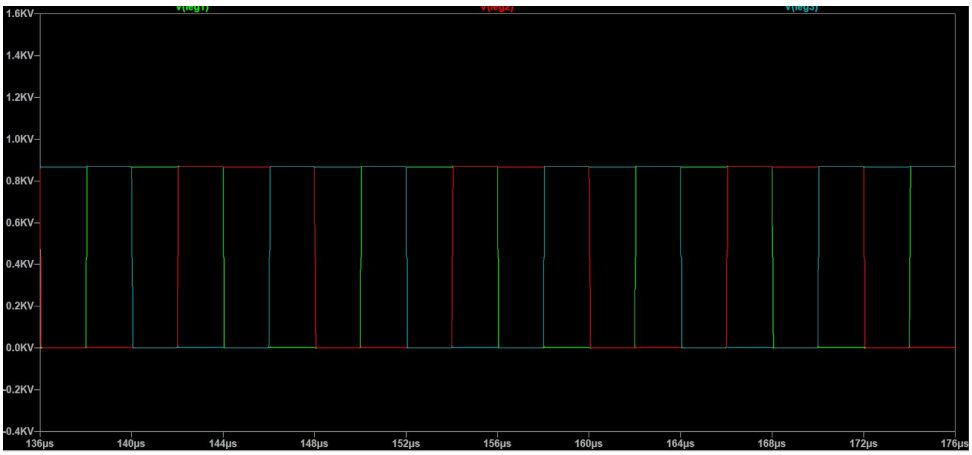


Figure 4. Output Voltage of each leg of the 3-phase motor (referenced to GND)

When the output voltage of one leg is measured relative to the central node of the load, the six step sinusoid becomes clear. The startup transient is also shown:

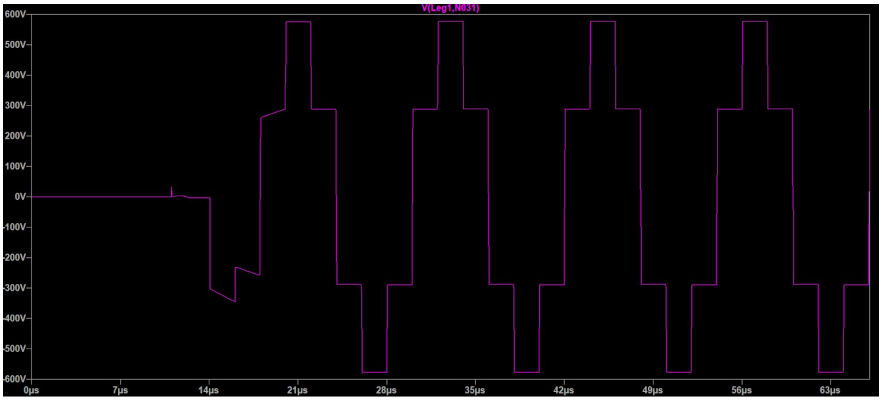


Figure 5. Output Voltage of 1 leg of the 3-phase motor (referenced to center node)

Comparing all the relative outputs makes it easy to see the three phase input to the load:

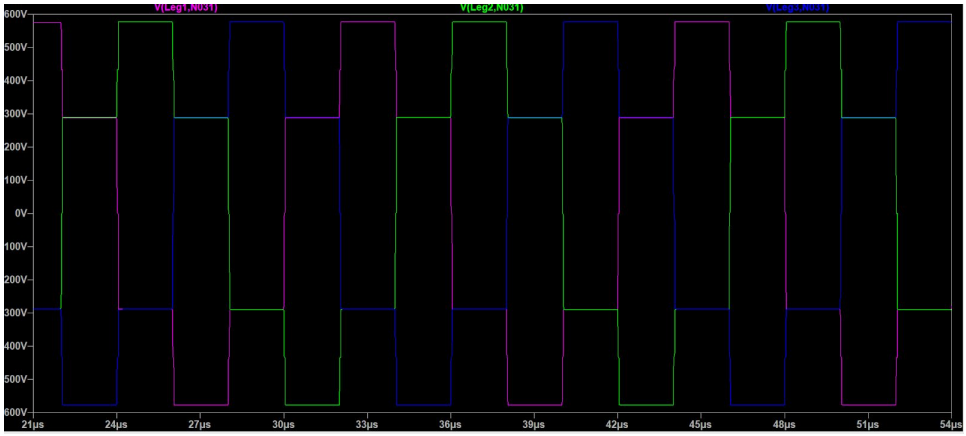


Figure 6. Output Voltage of each leg of the 3-phase motor (referenced to center node)

Switching dead time was minimized by examining the datasheet for our chosen transistor. The stated turn-off delay time is 16ns. At our switching frequency of 83.33kHz, this yields a maximum duty

cycle of 0.498. We chose to use 0.496 as our duty cycle. Below shows the drain current of a low side switch through multiple switching periods. It can be verified from this plot that we are not experiencing shoot through, and that the maximum current rating of the device of 35A is never exceeded:

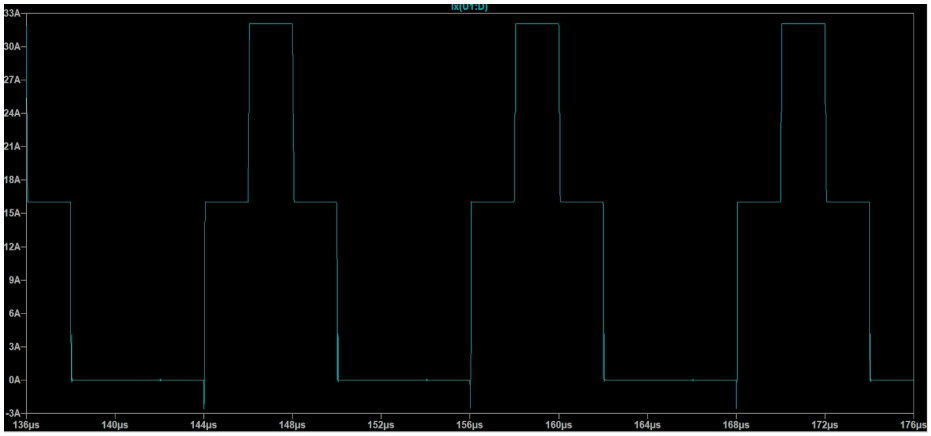


Figure 7. Drain current of low side switch of 1 of the half-bridge inverters

Finally, the output power of our inverter, needed to be verified. Shown below are our load configuration and the power through one of the three load resistors.

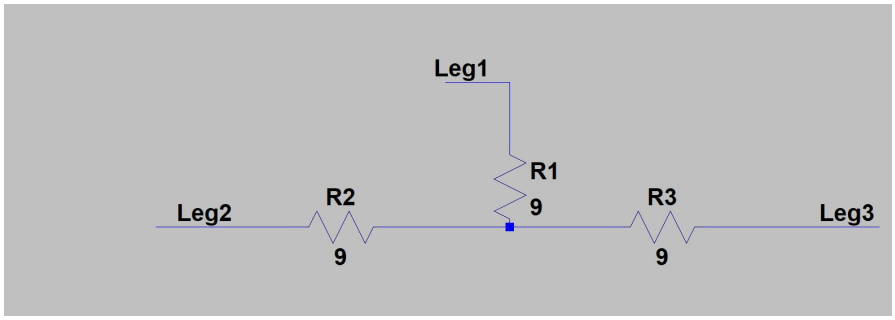


Figure 8. Resistive load as a model for BLDC motor

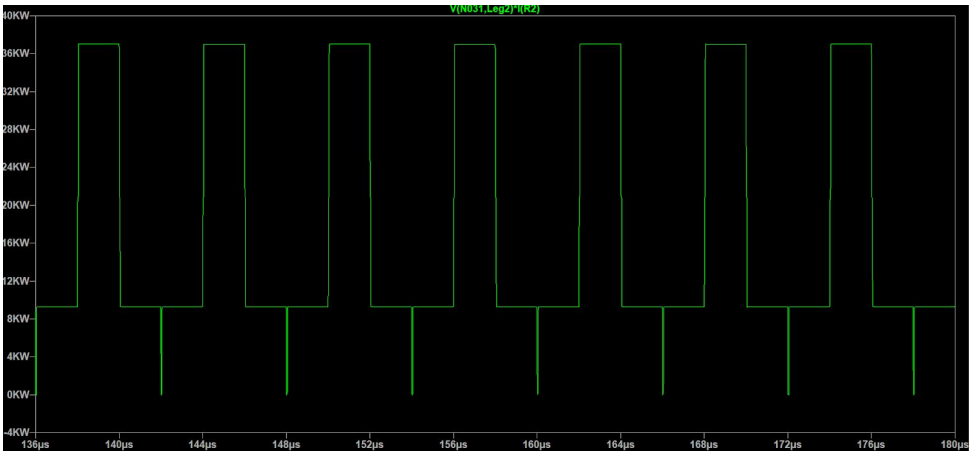


Figure 9. Output power of one of BLDC motor resistive loads

The RMS value of this waveform is 26kW. All three load resistors combined dissipate 78kW of power. Meeting our stated goal of 80kW for all intents and purposes. The average dissipated power is 55.2kW at a case temperature of 25C. Shown below is the is the load power through one resistor, and the input power from the DC bus.

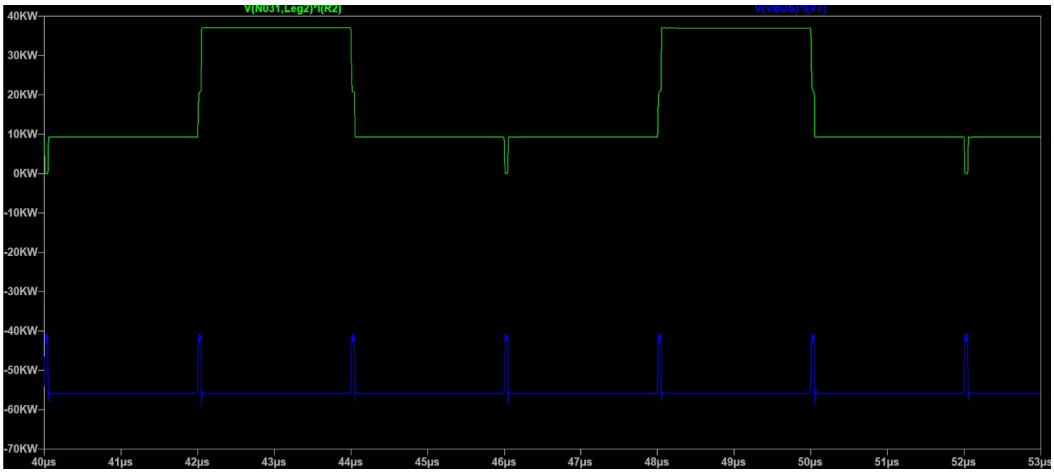


Figure 10. Input Power from the 870V DC bus

The average input power is 55.5kW. This gives our design an efficiency of 99%, meeting our stated goal of high efficiency. This is of course neglecting conduction loss in the wiring, which is likely non-negligible if our design were to be practically implemented.

Junction temperature of the SiC FETs can also affect the drain source resistance and hence lower the efficiency of the device. Our SiC FET models on LTspice were packaged with junction temperature and case temperature inputs. We simulated our device at ambient temperature (25 C) as well as at higher temperatures (~100 C) keeping in mind that the device would probably be installed in the motor compartment where the motor is a major contributor to elevated temperatures.

According to our results from simulations at different temperatures, we found that the junction temperature of our FETs rose only by about ~1-2 C above the case temperature. Increased junction temperature did negatively impact our efficiency. With a case temperature of 100C, our overall efficiency dropped around half a percent.

It would be best to use copper wires for our design since it is one of the most readily available conductors with a relatively low resistivity. It was determined that we use 12 AWG wire to the resistive loads on the BLDC motor and the FETs to satisfy our power requirements as well as to reduce conduction losses.

Shown below is the bill of materials for our design.

Quantity	Description	Value	Absolute Maximum	Tolerance	Manufacturer	Manufacturer PN	Distributor	Distributor PN
6	CAP CER 1UF 25V X7R 0805	1uF	25V	10%	Murata	GCM21BR71E105KA56L	Digikey	490-4785-1-ND
12	N-Channel 900V 35A (Tc) 113W (Tc) Surface Mount D2PAK-7		900V, 35A		Cree/Wolfspeed	C3M0065090J	Digikey	C3M0065090J-ND
6	DIODE SCHOTTKY 1.2KV 10A TO252-2		1200V, 10A		Cree/Wolfspeed	C4D10120E	Digikey	C4D10120E-ND
6	IC HIGH-SIDE DVR HS HV SOT23-6		80V, 2.4A		Linear Technology/Analog Devices	LTC4440ES6#TRMPBF	Digikey	LTC4440ES6#TRMPBFTR-ND

Table 1. Bill of Materials (BOM)

4 Future Directions

The most obvious simplification in our model is the use of a simple resistive load for the three phase motor which our inverter would be driving. Obviously this is not going to be a purely resistive load and is likely to be highly inductive. Given more time and resources we would like to simulate our design with a more accurately modeled load.

There are also many physical considerations which would become significant if our design were to be actually implemented. One of these is the reduction of the dielectric breakdown field of air at altitude. The stated cruising altitude of the Cessna 172 is 14,000 feet. At this altitude, the minimum trace gap on our circuit board would need to be much larger than at sea level, increasing the total solution cost. This penalizes using a high voltage DC bus, a consideration which is not as important when designing for operation at sea level.

Eventually, a full PWM control loop based on feedback from Hall sensors or a rotary encoder, would need to be added to the design, in order to implement a feedback loop for precise motor speed control.

The boost converter used in conjunction with the battery pack to provide 870V DC bus could have a feedback loop that can adjust the converter's duty cycle to provide current at the highest efficiency.

References

[1] George Bye, *"Cheaper, Lighter, Quieter: The Electrification of Flight Is at Hand."*, *IEEE Trans. Fly the Electric Skies*, September 2017

[2] Jian Zhao, Yangwei Yu, "*Brushless DC Motor Fundamentals*", *MPS AN047 Rev 1.0*, July 2011

[3] Web link: https://en.wikipedia.org/wiki/Brushless_DC_electric_motor