Latch and flip-flop stores 1-bit.
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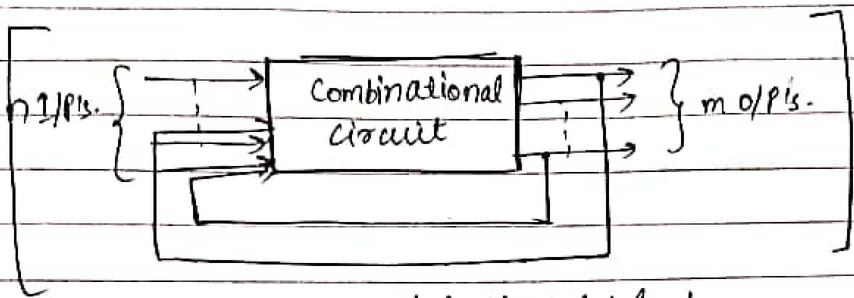
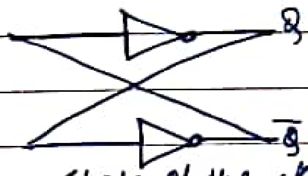
SEQUENTIAL CIRCUIT.

→ Sequential circuits are those circuits in which the present output depends not only on the present input but also on the previous output.
→ Sequential circuits have memory.
→ Basic building blocks are latches and flip-flop.

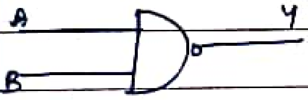


Sequential circuit Block.



State of the ckt will remain same.

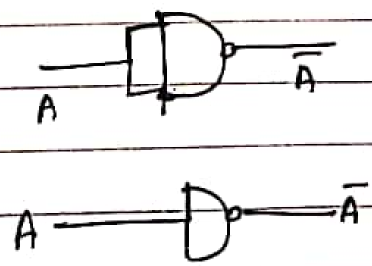
NAND GATE.



$Y = \overline{A \cdot B}$.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

⇒ O/P is low only if all the I/Ps are High.



Not using NAND.

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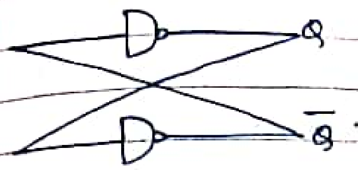
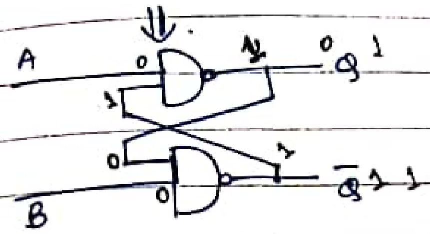
Latch.



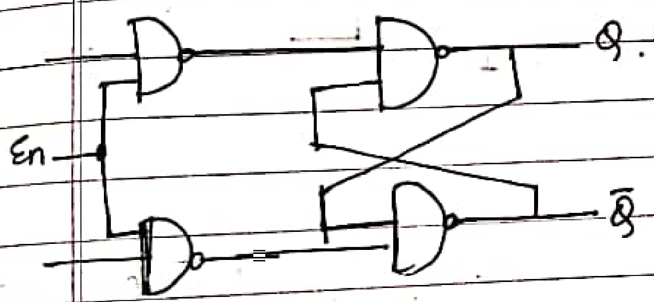
⇓



A	B	Q_{n+1}
0	0	Invalid (x)
0	1	1
1	0	0
1	1	Q_n (No change).

A	B	Q_n	Q_{n+1}
0	0	0	Invalid
0	0	1	Invalid
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1.

S-R Latch.



Set Reset

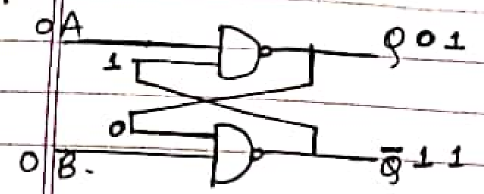
S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

Opposite of above as the inputs are inverted

En	S	R	Q_{n+1}
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Invalid.
0	X	X	Q_n

Working of A-B Latch

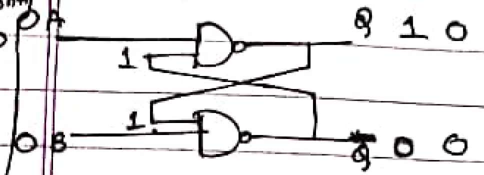
A	B	Q_n	Q_{n+1}
0	0	0	1



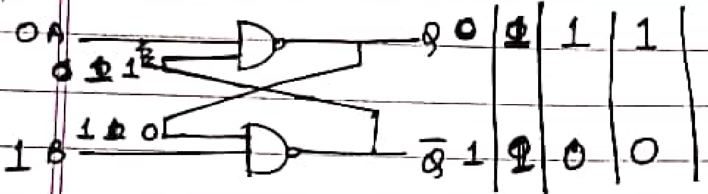
A	B	Q_{n+1}
0	0	X
0	1	1
1	0	0
1	1	Q_n

A	B	Q_n	Q_{n+1}
0	0	0	invalid
0	0	1	invalid.
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	Q_n
1	1	1	Q_n

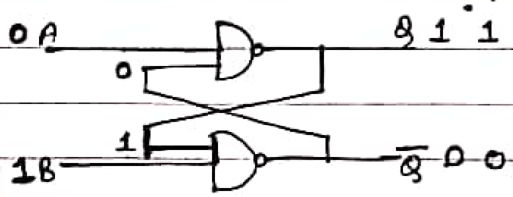
A	B	Q_n	Q_{n+1}
0	0	1	0

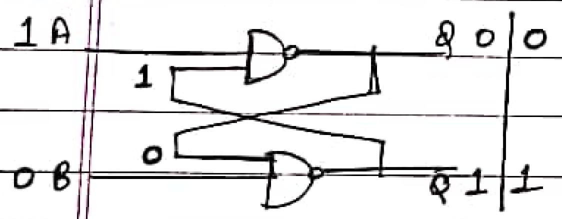


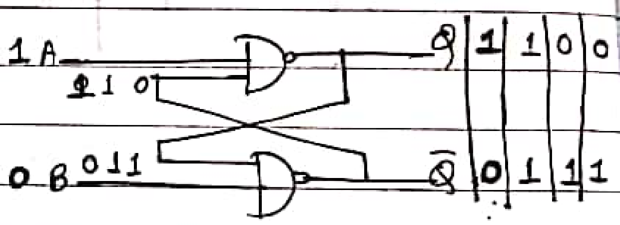
A	B	Q_n	Q_{n+1}
0	1	0	1

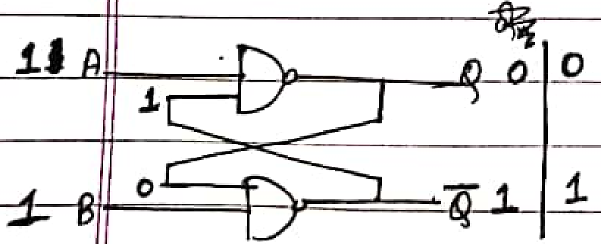


A	B	Q_n	Q_{n+1}
0	1	1	1



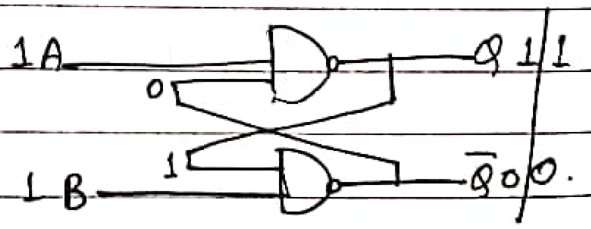






Output → Q_n

Same output. 0 → 0
1 → 1.



Output → Q_n.

Same output 1 → 1
0 → 0.

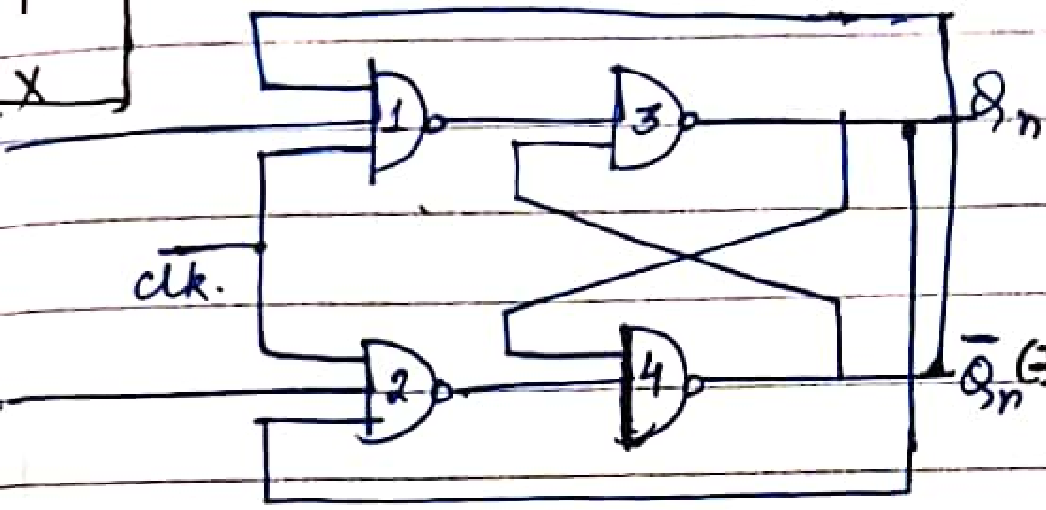
Scanned by CamScanner

Q_{n+1}
Q_n
0
1
X

Level (+,-).

J-K- Flip-Flop.

main t



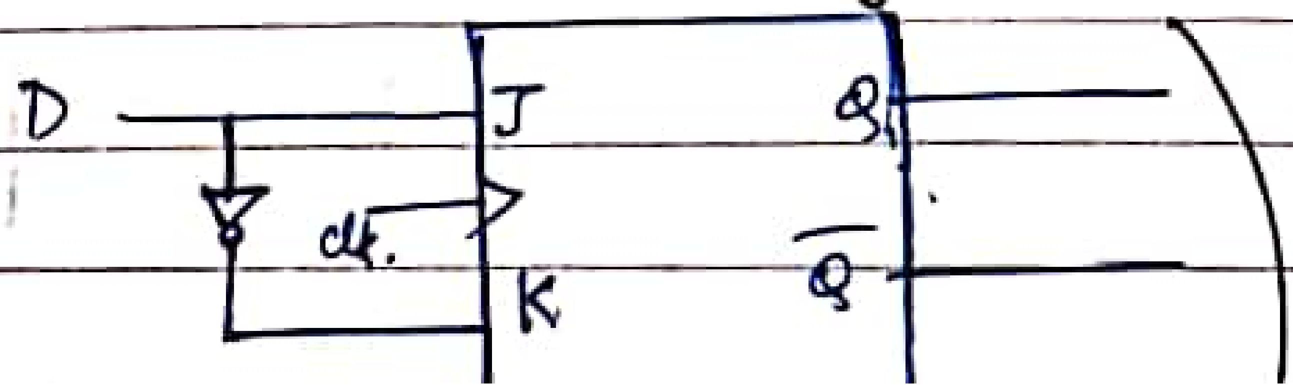
clk	J	K
✓	0	0
✓	0	1
✓	1	0
✓	1	1
X	X	X

J	K	Q_n	Q_{n+1}
1	1	0	1
1	1	1	0

In this after one output once the clk pressed so again we cannot press s
so after one revolution the (1) a
not accept the input so th
will be because

T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

D-Flip-Flop (Delay Flip-Flop).



characteristic table

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S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

$Q_{n+1} = \Sigma m(1,4,5) + \Sigma d(6,7)$.

S \ R Q_n	00	01	11	10
$\bar{S}$ 0		1		
S 1	1	1	X	X

$$\boxed{Q_{n+1} = S + \bar{R} Q_n}$$

characteristic equation.

	J	K	Q_n	Q_{n+1}
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	0
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0

$Q_{n+1} = \Sigma m(1,4,5,6)$

J \ K Q_n	$\bar{K}\bar{Q}_n$ 00	$\bar{K} Q_n$ 01	$K Q_n$ 11	$K \bar{Q}_n$ 10
$\bar{J}$ 0		1		
J 1	1	1		1

$$\boxed{Q_{n+1} = J \bar{Q}_n + \bar{K} Q_n}$$

J	Q_{n+1}
0	0
1	0

D	Q_{n+1}
0	0
1	1

characteristic table.

	T	Q_n	Q_{n+1}	
0	0	0	0	$\}\ Q_n$
1	0	1	1	
2	1	0	1	$\}\ \bar{Q}_n$
3	1	1	0	

T \ Q_n	$\bar{Q}_n$ (0)	Q_n (1)
$\bar{T}$ 0	[0]	1 [1]
T 1	1 [2]	[3]

$$Q_{n+1} = T\bar{Q}_n + \bar{T}Q_n$$
$$= T \oplus Q_n .$$

	D	Q_n	Q_{n+1}
0	0	0	0
1	0	1	0
2	1	0	1
3	1	1	1

D \ Q_n	$\bar{Q}_n$ (0)	Q_n (1)
$\bar{D}$ 0	[0]	[1]
D 1	1 [2]	1 [3]

$$Q_{n+1} = D .$$

Excitation Table.

SR.

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0.

$0 \to 0$ $\begin{array}{cc} S & R \\ \end{array}$ $\begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix}$ $\begin{array}{cc} 0 & X \end{array}$

$1 \to 1$ $\begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix}.$ $\begin{array}{cc} X & 0 \end{array}$

JK.

Q_n	Q_{n+1}	J	K
0	0	0	X.
0	1	1	0.
1	0	0	1.
1	1	1	X.

Q_n	Q_{n+1}	J	K.
0	0	0	X
0	1	1	X
1	0	X	1.
1	1	X	0

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Ans T = XOR se aa rha tha. toh kisse ka XOR kare same output aayega.

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

output ko toggled

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

As the input same output

$\boxed{Q_{n+1} = D \quad D = Q_{n+1}}$

Flip-flops with Asynchronous ~~out~~ inputs.

1. These inputs (P_r, C_r) are independent from clock and actual flip-flop inputs.
2. P_r (if activated) makes the output high.
3. C_r (if activated) makes the output zero.
4. So in order to achieve ~~to~~ normal flip-flop operation these inputs must be deactivated or disabled.

S-R Flip-Flop

Truth Table.

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

Characteristic Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

Excitation Table.

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

J-K Flip Flop.

Truth Table

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$
X	X	Q_n

Characteristic Table.

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Excitation Table.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

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flip-flop conversion.

Given ff → Target ff.

SR-JK
SR - T.
SR - D.
JK-T
JK → D.
T → JK
T → D
D → JK
D → T

SR → JK.

→ Excitation table of the given ff must be known.

→ Characteristic table of the target flip flop must be know

→ Prepare K-maps for given ff inputs
→ ~~Labelling~~ in terms of target ff inputs and previous output.

→ Make an updated block level circuit using the ~~K-Map~~ K-Map answers.

Excitation Table SR → JK. characteristic table.

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①.

Q_n	Q_{n+1}	SR
0	0	0 X
0	1	1 0
1	0	0 1
1	1	X 0

JK	Q_{n+1}
0 0	Q_n
0 1	0
1 0	1
1 1	$\overline{Q_n}$

J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

$S = \Sigma m(4,6) + \Sigma d(1,5)$.

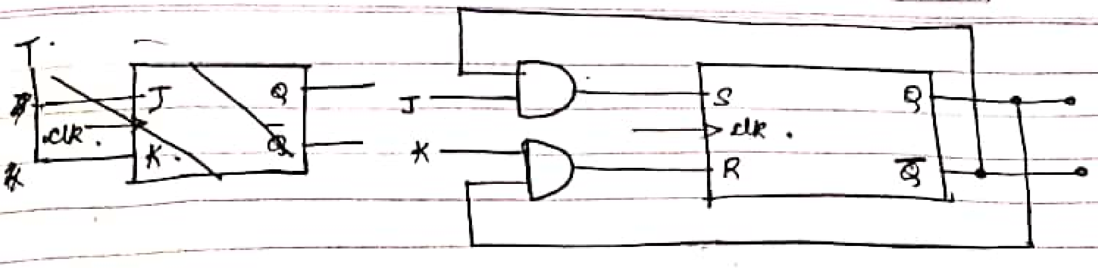
$R = \Sigma m(3,7) + \Sigma d(0,2)$.

J \ KQ_n	00	01	11	10
$\bar{J}$ 0	$_0$	X $_1$	$_3$	$_2$
J 1	1 $_4$	X $_5$	$_7$	1 $_6$

$S = J\overline{Q_n}$.

J \ KQ_n				
	X $_0$	$_1$	1 $_3$	X $_2$
	$_4$	$_5$	1 $_7$	$_6$

$R = KQ_n$.



② $SR \rightarrow T$ Characteristic Table.

Excitation table.

	T	Q_n	Q_{n+1}	S	R
0	0	0	0	0	X
1	0	1	1	X	0
2	1	0	1	1	0
3	1	1	0	0	1

Rough.

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	X	0

$S = \Sigma m(2) + \Sigma d(1)$

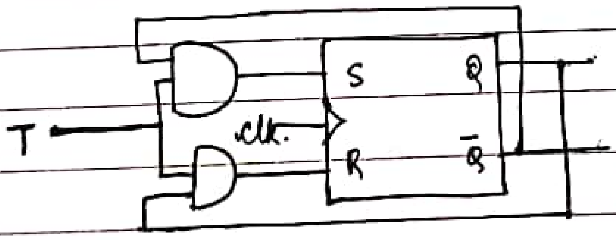
$R = \Sigma m(3) + \Sigma d(0)$.

T \ Q_n	$\bar{Q}_n$	Q_n
$\bar{T}$		X
T	1	

$S = T\bar{Q}_n$

T \ Q_n	$\bar{Q}_n$	Q_n
$\bar{T}$	X	
T		1

$R = TQ_n$.



Excitation SR → D → Characteristic table
Table.

D	Q_{n+1}
0	0
1	1

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

	D	Q_n	Q_{n+1}	S	R
0	0	0	0	0	X
1	0	1	0	0	1
2	1	0	1	1	0
3.	1	1	1	X	0

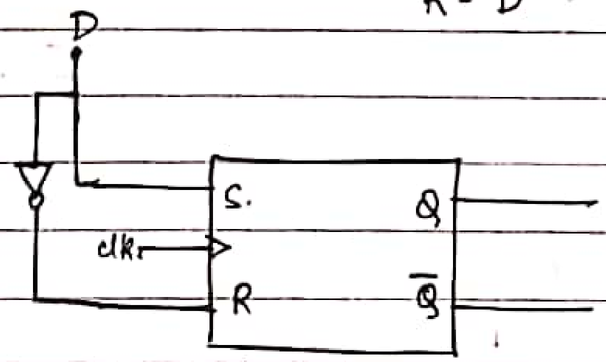
$$S = \Sigma m(2) + \Sigma d(3)$$

$$R = \Sigma m(1) + \Sigma d(0).$$

D \ Q_n	$\overline{Q_n}$	Q_n
$\overline{D}$ 0		
D 1	1	X

D \ Q_n	$\overline{Q_n}$	Q_n
$\overline{D}$ 0	X	1
D 1		

$S = D$ $R = \overline{D}$.



(4)

$JK \rightarrow T$. Characteristic table

Excitation Table.

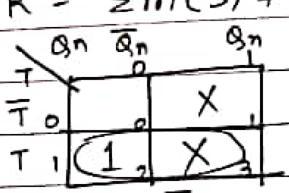
T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	~~x~~
1	0	~~x~~	1
1	1	x	0

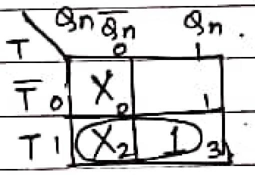
	T	Q_n	Q_{n+1}	J	K
0	0	0	0	0	X
1	0	1	1	X	0
2	1	0	1	1	~~X~~
3	1	1	0	~~X~~	1

$J = \Sigma m(2) + \Sigma d(1,3)$

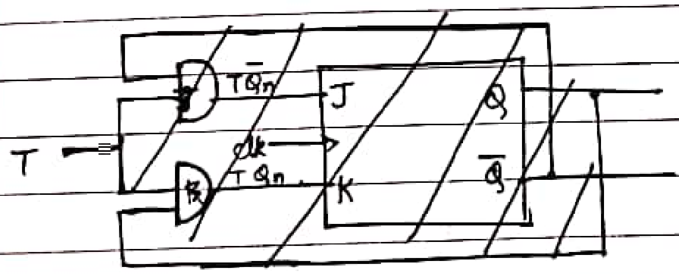
$K = \Sigma m(3) + \Sigma d(0,2)$.

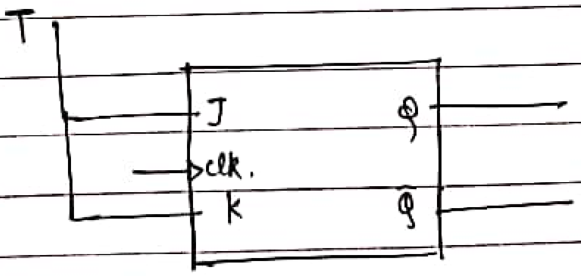


~~$J = T\overline{Q_n}$~~ $J = T$



~~$K = TQ_n$~~ . $K = T$





(5)

JK → D → characteristic Table.

Excitation Table

D	Q_{n+1}
0	0
1	1

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

	D	Q_n	Q_{n+1}	J	K
0	0	0	0	0	X
1	0	1	0	X	1
2	1	0	1	1	X
3	1	1	1	X	0

$J = \Sigma m(2) + \Sigma d(1, 3)$.

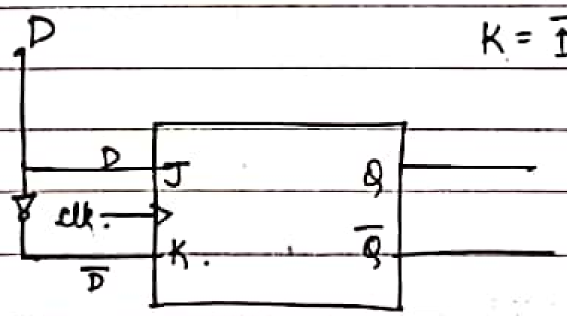
$K = \Sigma m(1) + \Sigma d(0, 3)$.

D \ Q_n	$\bar{Q}_n$ (0)	Q_n (1)
$\bar{D}$ (0)	(0)	X (1)
D (1)	1 (2)	X (3)

D \ Q_n	$\bar{Q}_n$ (0)	Q_n (1)
$\bar{D}$ (0)	X (0)	1 (1)
D (1)	(2)	X (3)

$J = D$

$K = \bar{D}$



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(6)- $T \rightarrow JK$. → Characteristic Table

Excitation Table

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

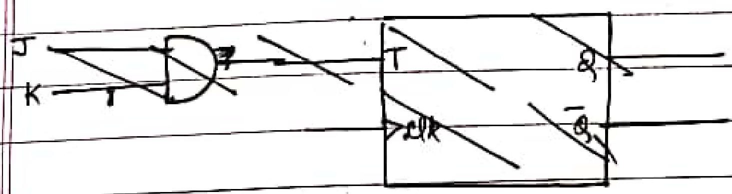
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

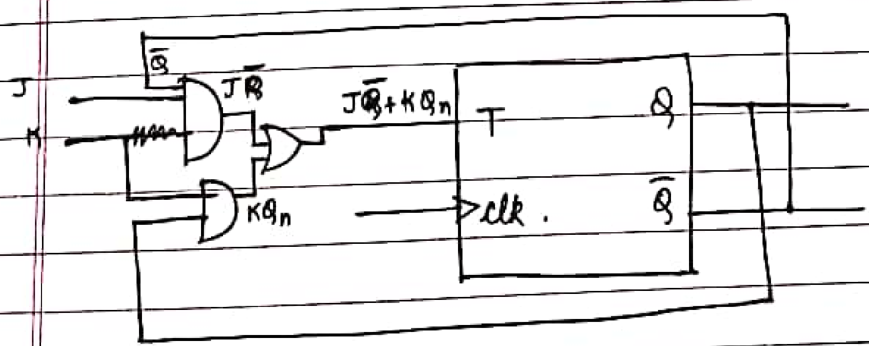
	J	K	Q_n	Q_{n+1}	T
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	0	0
3	0	1	1	0	1
4	1	0	0	1	1
5	1	0	1	1	0
6	1	1	0	1	1
7	1	1	1	0	1

$T = \Sigma m(3,4,6,7)$.

J \ KQ_n	$\bar{K}\bar{Q}_n$ 00	$\bar{K}Q_n$ 01	KQ_n 11	$K\bar{Q}_n$ 10
$\bar{J}$ 0			1	
J 1	1		1	1

$T = J\bar{Q}_n + KQ_n$.





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$T \rightarrow D$ Characteristic Table.

Excitation Table

D	Q_{n+1}
0	0
1	1

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

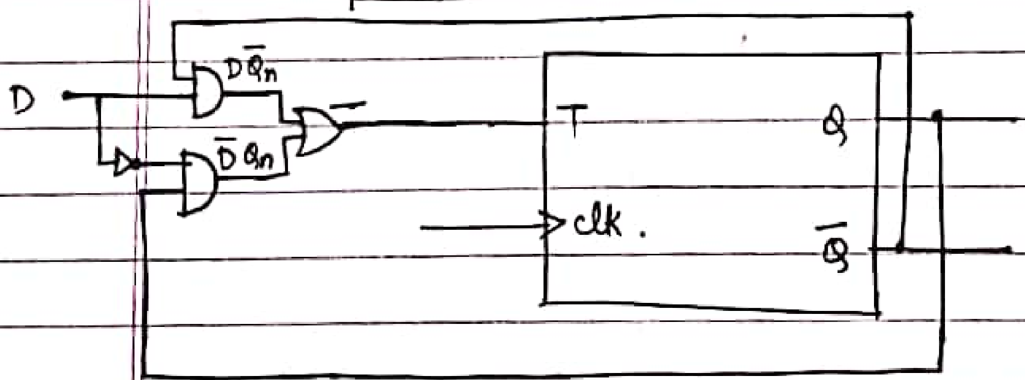
	D	Q_n	Q_{n+1}	T
0	0	0	0	0
1	0	1	0	1
2	1	0	1	1
3	1	1	1	0

~~$T = \Sigma m(1,2)$~~

$T = \Sigma m(1, 2)$.

D \ Q_n	$\bar{Q}_n$ (0)	Q_n (1)
$\bar{D}$ 0	(0)	1 (1)
D 1	1 (2)	(3)

$T = D\bar{Q}_n + \bar{D}Q_n$.



8

$D \rightarrow JK$

Excitation Table. → characteristic Table.

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

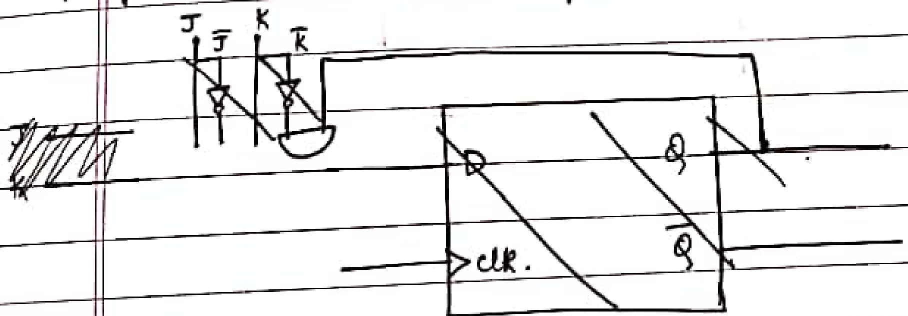
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

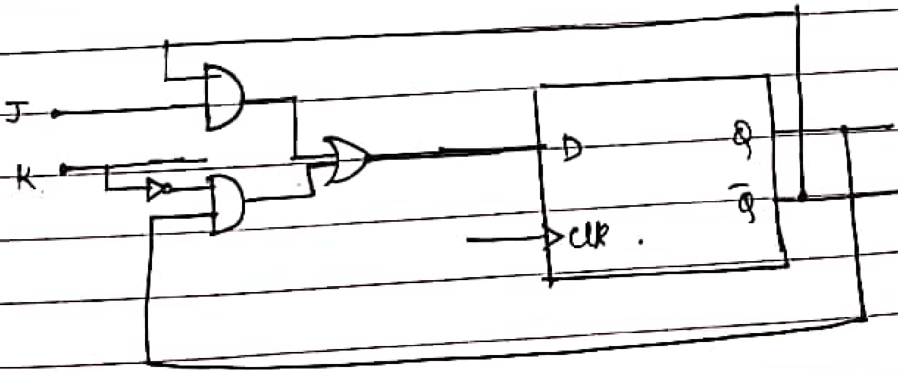
	J	K	Q_n	Q_{n+1}	D.
0	0	0	0	0	0
1	0	0	1	1	1
2	0	1	0	0	0
3	0	1	1	0	0
4	1	0	0	1	1
5	1	0	1	1	1
6	1	1	0	1	1
7	1	1	1	0	0

$D = \Sigma m(1,4,5,6)$.

J \ KQ_n	$\bar{K}\bar{Q}_n$ 00	$\bar{K}Q_n$ 01	KQ_n 11	$K\bar{Q}_n$ 10
$\bar{J}$ 0	0	1 1	3	2
J 1	1 4	1 5	7	1 6

$D = \bar{K}Q_n + J\bar{Q}_n$





(9). D → T.

characteristic Table.

Excitation Table.

T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

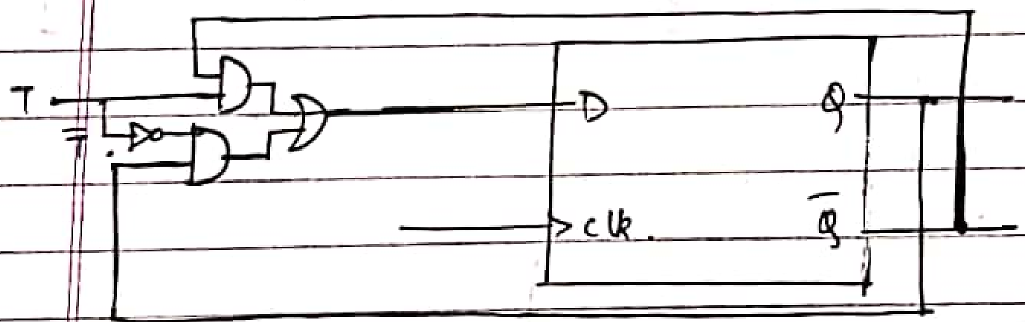
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

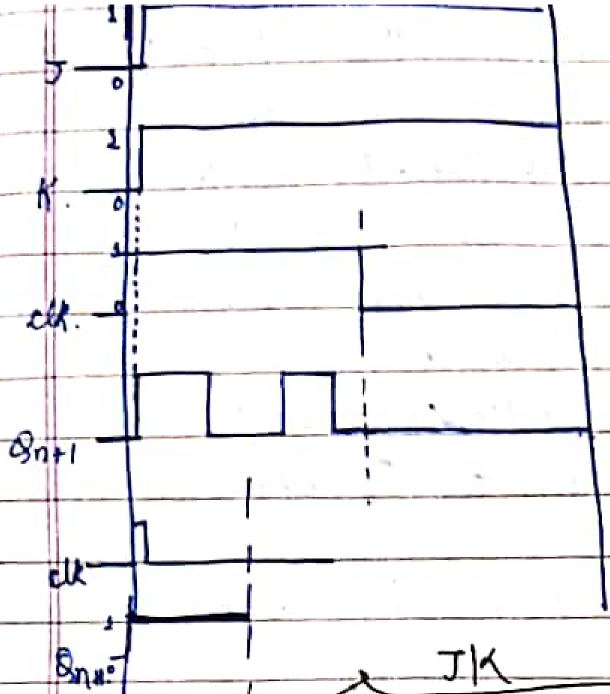
	T	Q_n	Q_{n+1}	D
0	0	0	0	0
1	0	1	1	1
2	1	0	1	1
3	1	1	0	0

$$D = \Sigma m(1, 2)$$

T \ Q_n	$\overline{Q_n}$ (0)	Q_n (1)
$\overline{T}$ 0	[0]	1 [1]
T 1	1 [2]	[3]

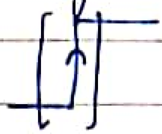
$$D = T\overline{Q_n} + \overline{T} Q_n .$$





① $t_{min} \leq t_{clk} \leq t_{p}$ (reducing the clock duration).

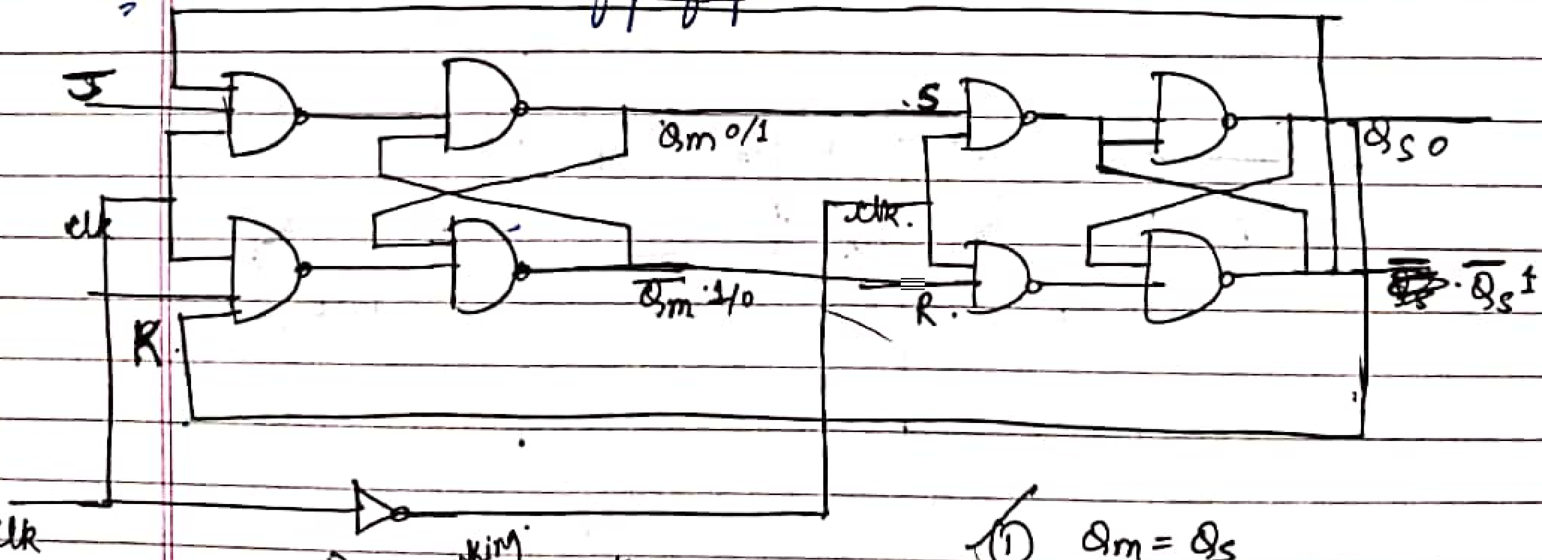
② Use edge triggered clocks (+ve, -ve).



Truth Table JK

JK SR

③ Master's-slave JK flip-flop.



clock

(+ve half) master is working.

clk (-ve) by not gate (+ve) so slave will work so slave will copy the output of master to its own output.

(This condition will never occur.)

① $Q_m = Q_s$

$\overline{Q_m} = \overline{Q_s}$.

②. SR slave Invalid problem.

③. Not Gate b/w clocks.

Counters (Up, Down, Random).

Synchronous

Asynchronous. (Ripple)

Asynchronous (Up counters)

→ No. of flip-flops required is equal to no. of bits In max count.

→ flip-flop will always be T-flip-flop (all T inputs connected to 1).

→ -ve edge clock will be used. (for +ve down counter)

→ clock is externally given only to LSB flip-flop.

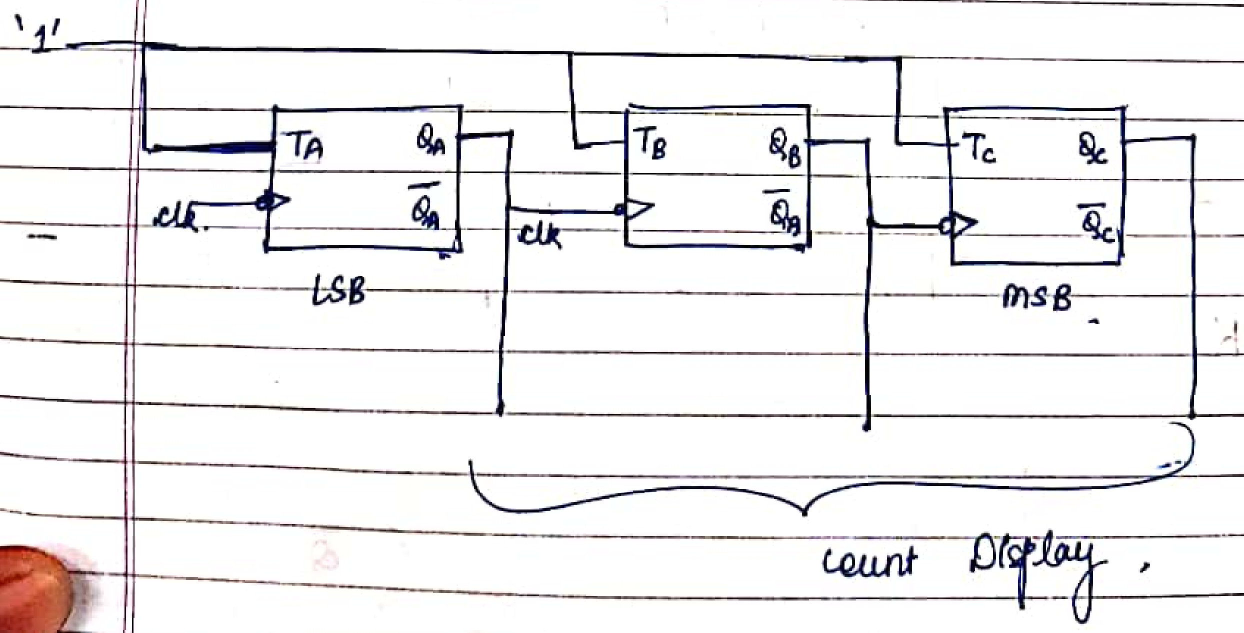
→ Rest of the flip-flops will get there clock from there left flip-flop output.

→ No. of stages in a counter is equal to mod of the counter.

$\boxed{\text{MOD / MODULUS / MODULO / DIVIDE BY.}}$

(0-7)

MOD 8 Asynchrous up counter.

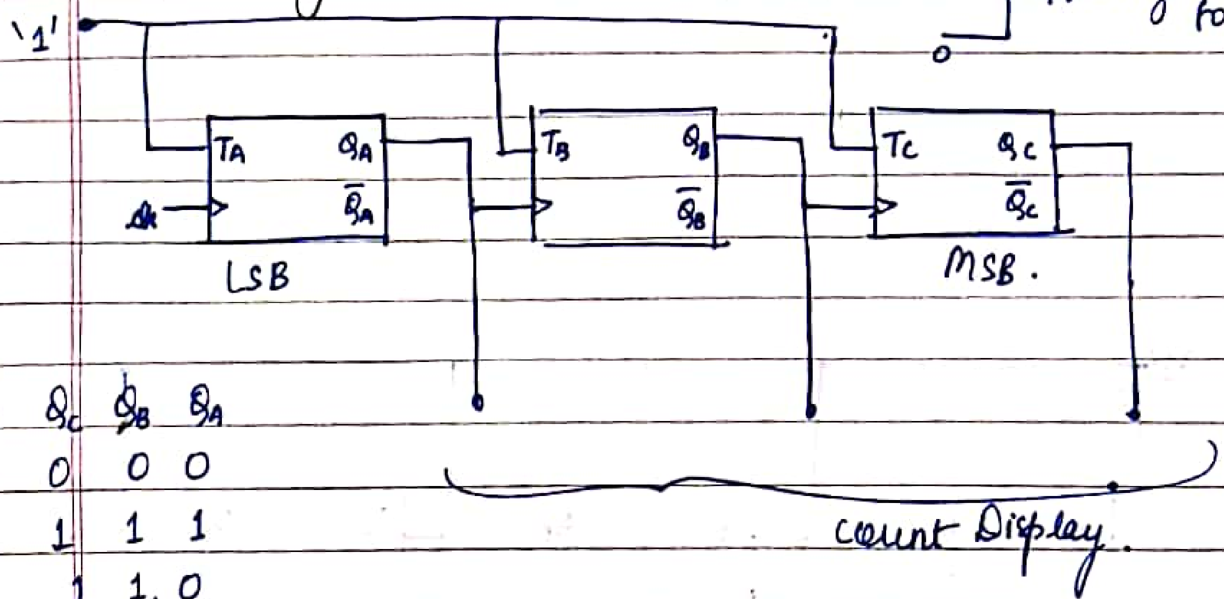


−ve edge
for up counter.

clk	Q_C (4)	Q_B (2)	Q_A (1)
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

Mod 8 Asynchronous down counter.

+ve edge for down counter.



clk	Q_C	Q_B	Q_A
0	0	0	0
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1
8	0	0	0

16 8 4 2 1

$2^{n} \rightarrow$ no. of flip-flop.

$16 = 2^{4} \rightarrow$ no. of flip-flop

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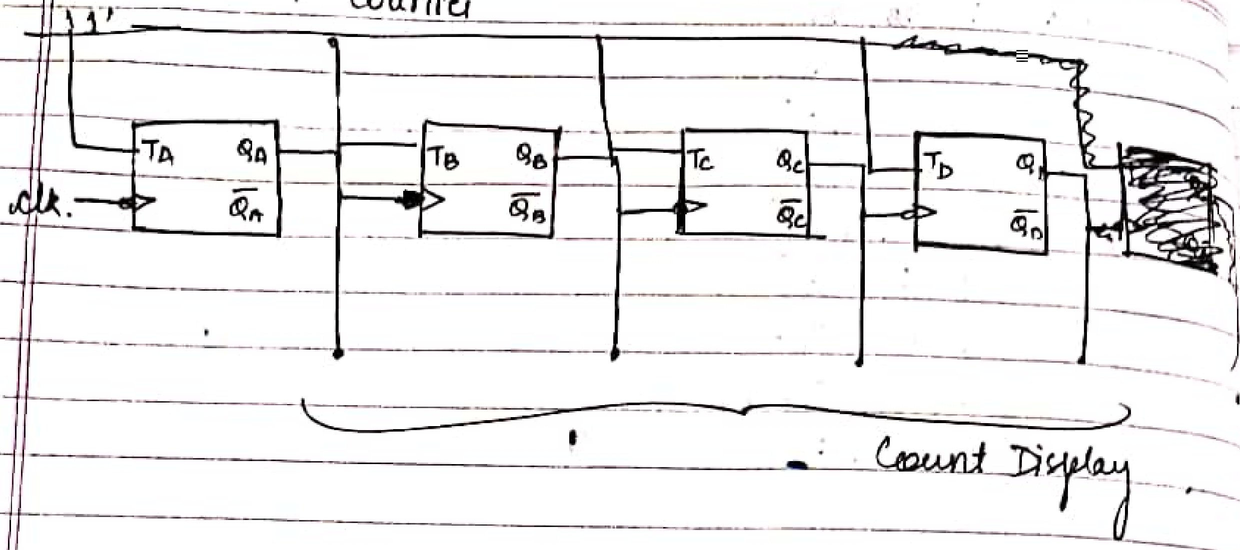
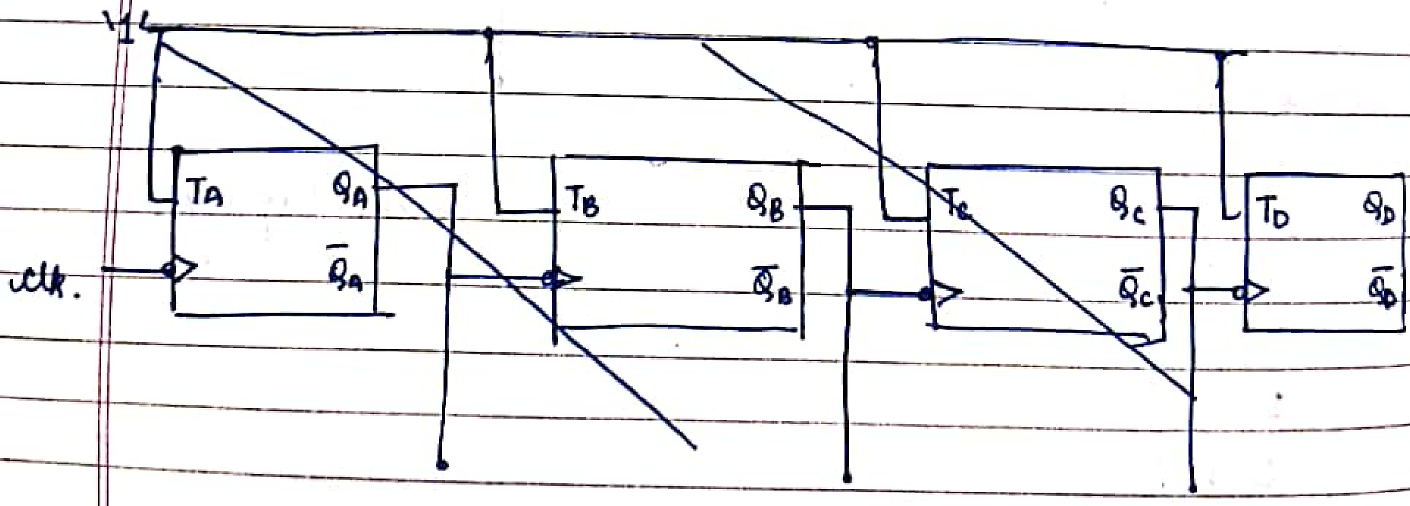
MOD-16 UP counter



MOD-12. Asynchronous up-counter.



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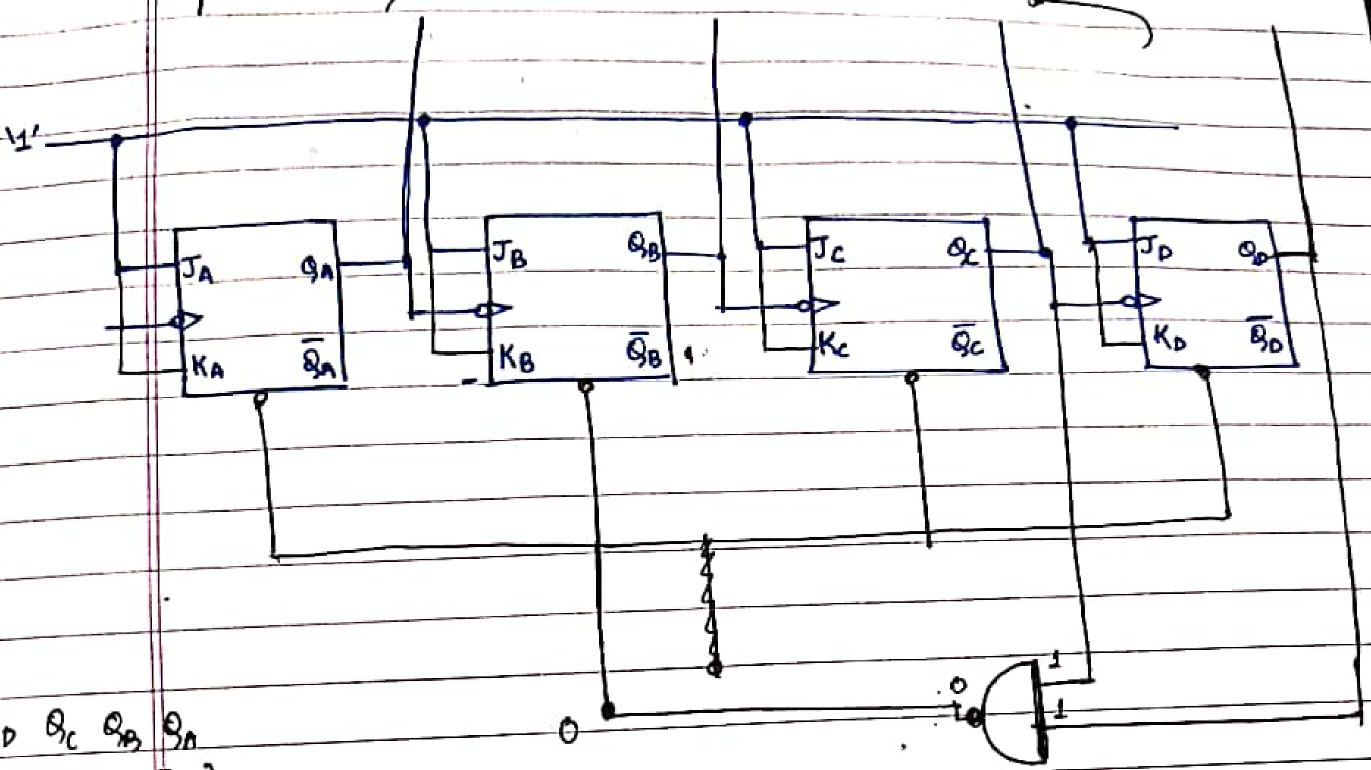
till 11 not required 12.

MOD-12 Asynchronous up counter.

Count Display.



Q_D Q_C Q_B Q_A

0 0 0 0

↓

1 0 1 1

Required.

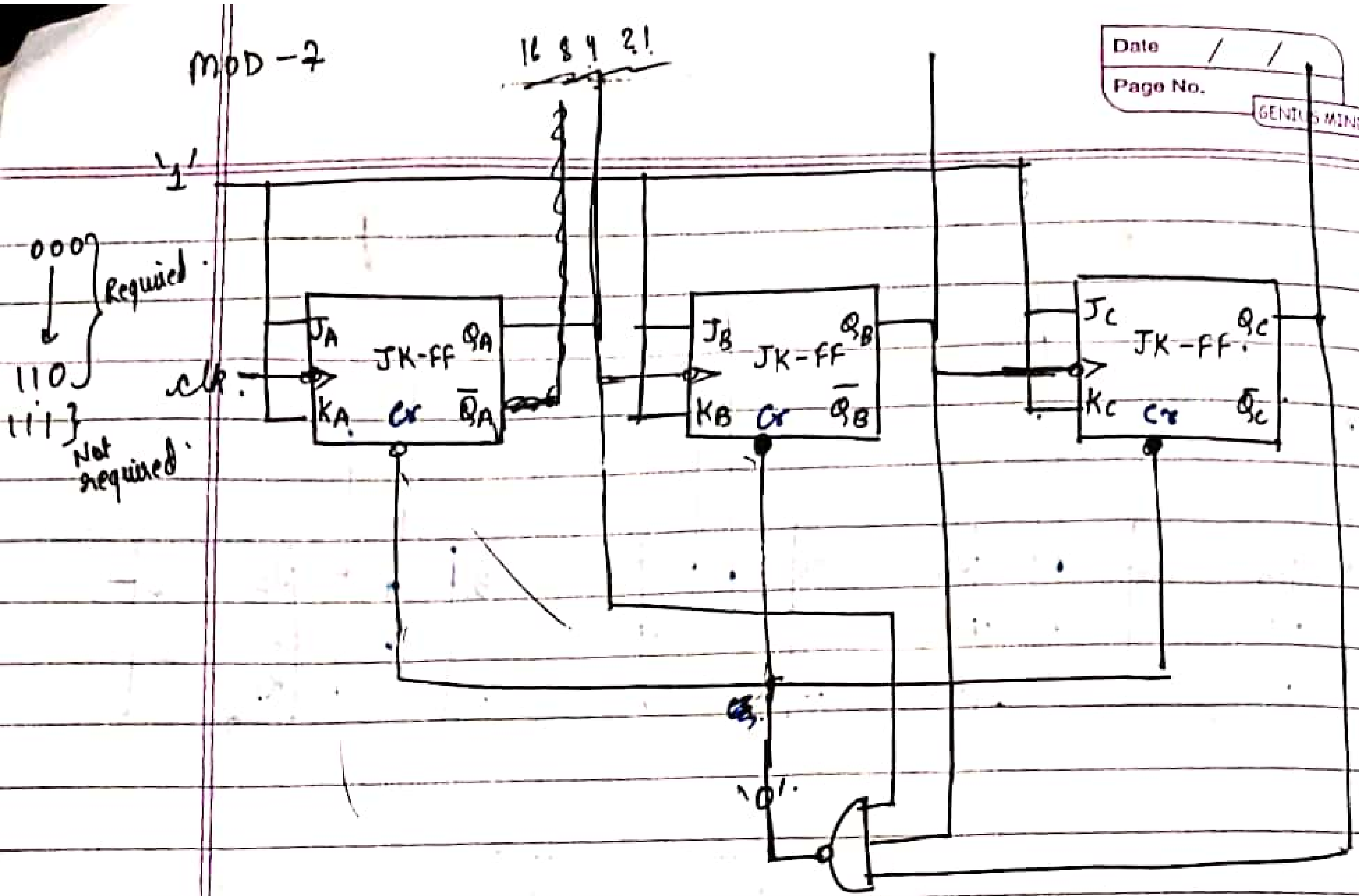
1 1 0 0

↓

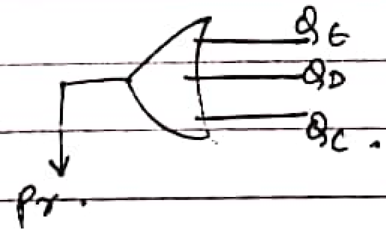
1 1 1 1

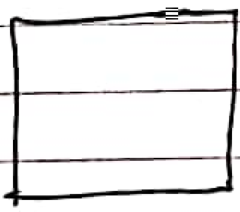
Not Required.

MOD-7



MOD-28. (3 don't want).

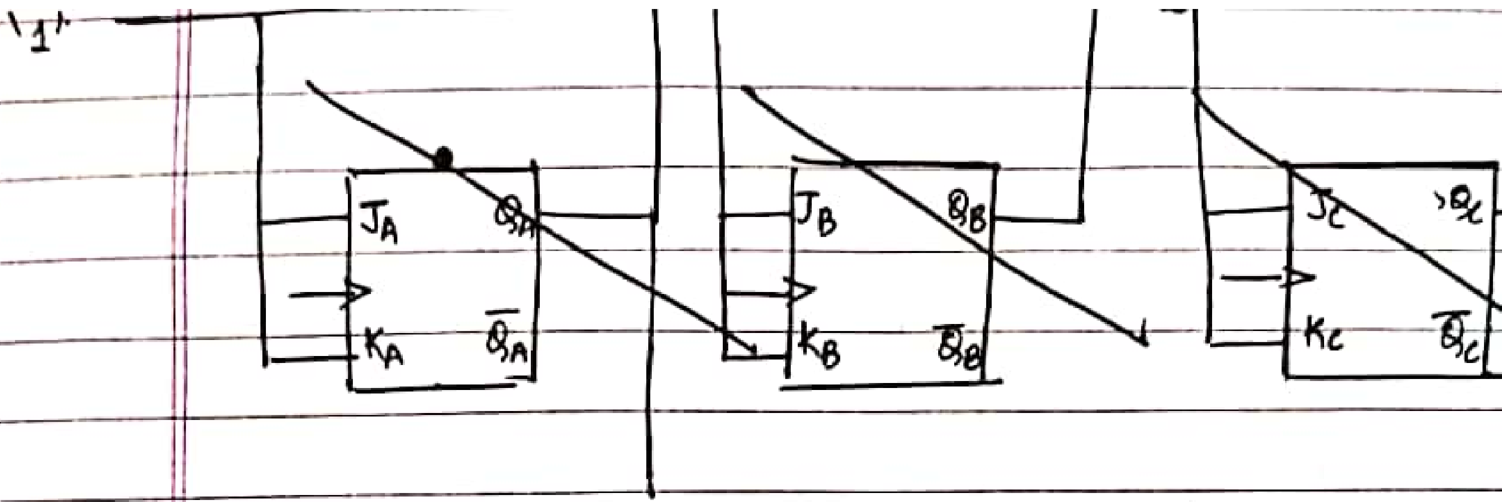


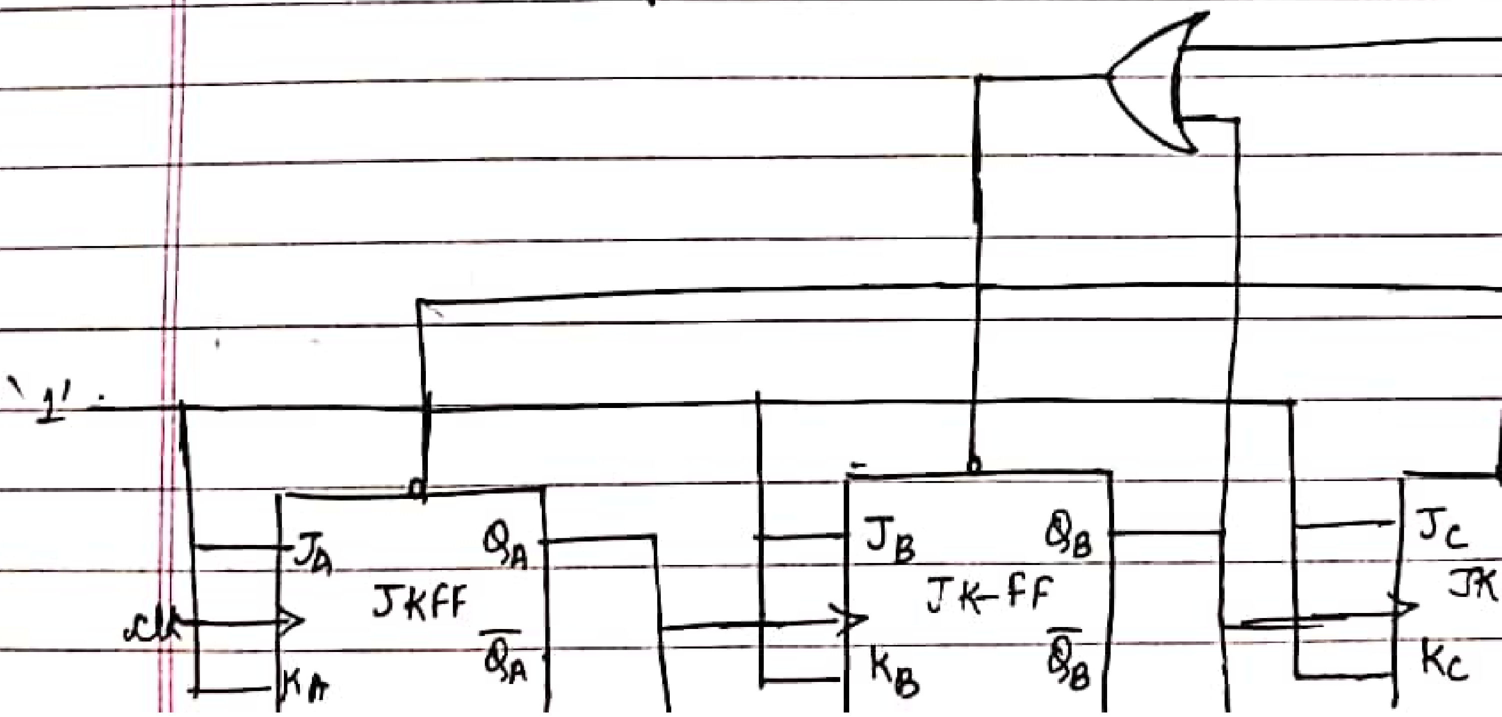


MOD-6 up.

000
001
010
011
100
101
110
111

Mod-6 Down


'1'
J_A
Q_A
K_A
$\bar{Q}_A$
J_B
Q_B
K_B
$\bar{Q}_B$
J_C
Q_C
K_C
$\bar{Q}_C$

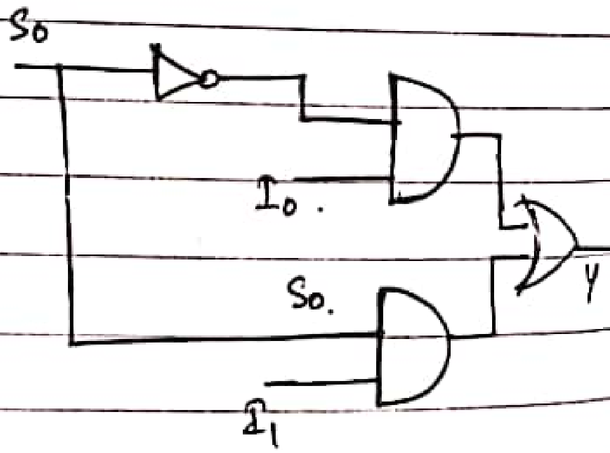

'1'
clk
J_A
Q_A
JKFF
K_A
$\bar{Q}_A$
J_B
Q_B
JK-FF
K_B
$\bar{Q}_B$
J_C
JK
K_C

T.T for 2x1 mux.

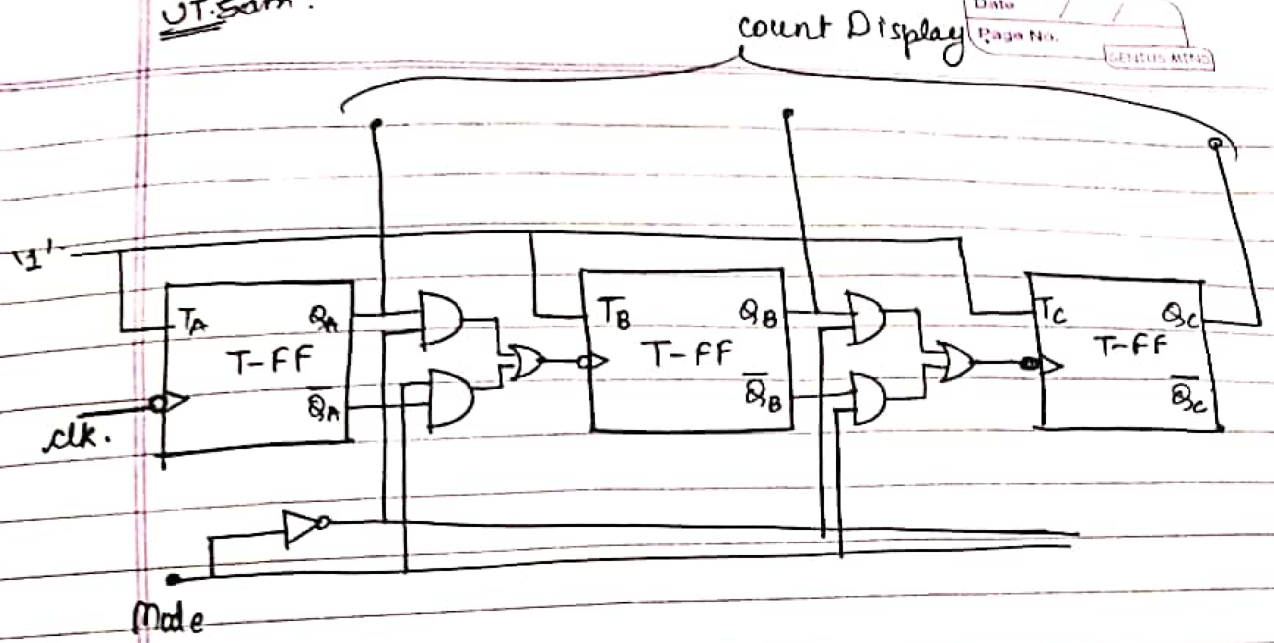
S_0	Y
0	I_0
1	I_1

$$Y = \bar{S}_0 I_0 + S_0 I_1.$$

Circuit for 2x1 mux.



UT Sem.



Synchronous counters.

→ No boundation of flip-flop.
→ No boundation of clock.
-

→ Excitation table of flip-flop must be known.
→ Prepare state diagram.
→ Prepare state table.
→ Prepare K-maps for the flip-flop inputs in terms of previous state outputs.
→ Draw circuit as per the K-Map expressions.

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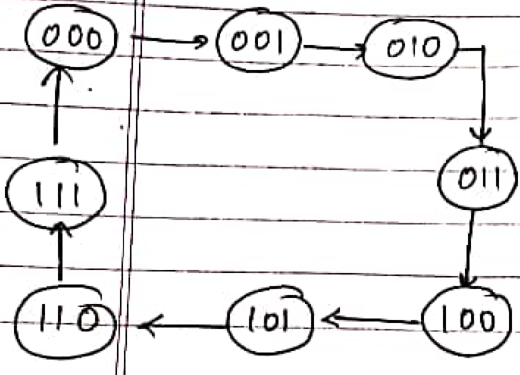
imp.

MOD - 8 Synchronous counter using J-K Flip-flop.

→ 8 States (000 → 111) (no. of FFs = 3) → $Q_C\, Q_B\, Q_A$.



Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

State Table.

In this we write the numbers of the next stage

Clk	Present st. Q_C	Q_B	Q_A	Next st. Q_{C+1}	Q_{B+1}	Q_{A+1}	FF i/p. $J_C\,K_C$	$J_B\,K_B$	$J_A\,K_A$	
1	0	0	0.	0	0	1	0 X	0 X	1 X	0
2	0	0	1	0	1	0	0 X	1 X	X 1	1
3	0	1	0	0	1	1	0 X	X 0	1 X	2
4	0	1	1	1	0	0	1 X	X 1	X 1	3
5	1	0	0	1	0	1	X 0	0 X	1 X	4
6	1	0	1	1	1	0	X 0	1 X	X 1	5
7	1	1	0	1	1	1	X 0	X 0	1 X	6
8.	1	1	1	0	0	0	X 1	X 1	X 1.	7.

$$J_C = \Sigma m(3) + \Sigma d(4,5,6,7)$$
$$K_C = \Sigma m(7) + \Sigma d(0,1,2,3)$$

$$J_A = \Sigma m(0,2,4,6) + \Sigma d(\cancel{2}, 1, 3, 5, 7).$$
$$K_A = \Sigma m(1,3,5,7) + \Sigma d(0,2,4,6).$$

Scanned by CamScanner

1	$_4$	1_5	X_7	X_6

$Q_B\ Q_A$.

J_B ~~$= \bar{Q}_{B+1} Q_{A+1}$. $\bar{Q}_B Q_A$.~~

$Q_B Q_A$ / Q_C

	X_0	X_1	1_3	$_2$
	X_4	X_5	1_7	$_6$

$K_B = Q_A$.

~~$K_B = Q_{B+1} Q_{A+1}$. $Q_B Q_A$.~~

$Q_B Q_A$

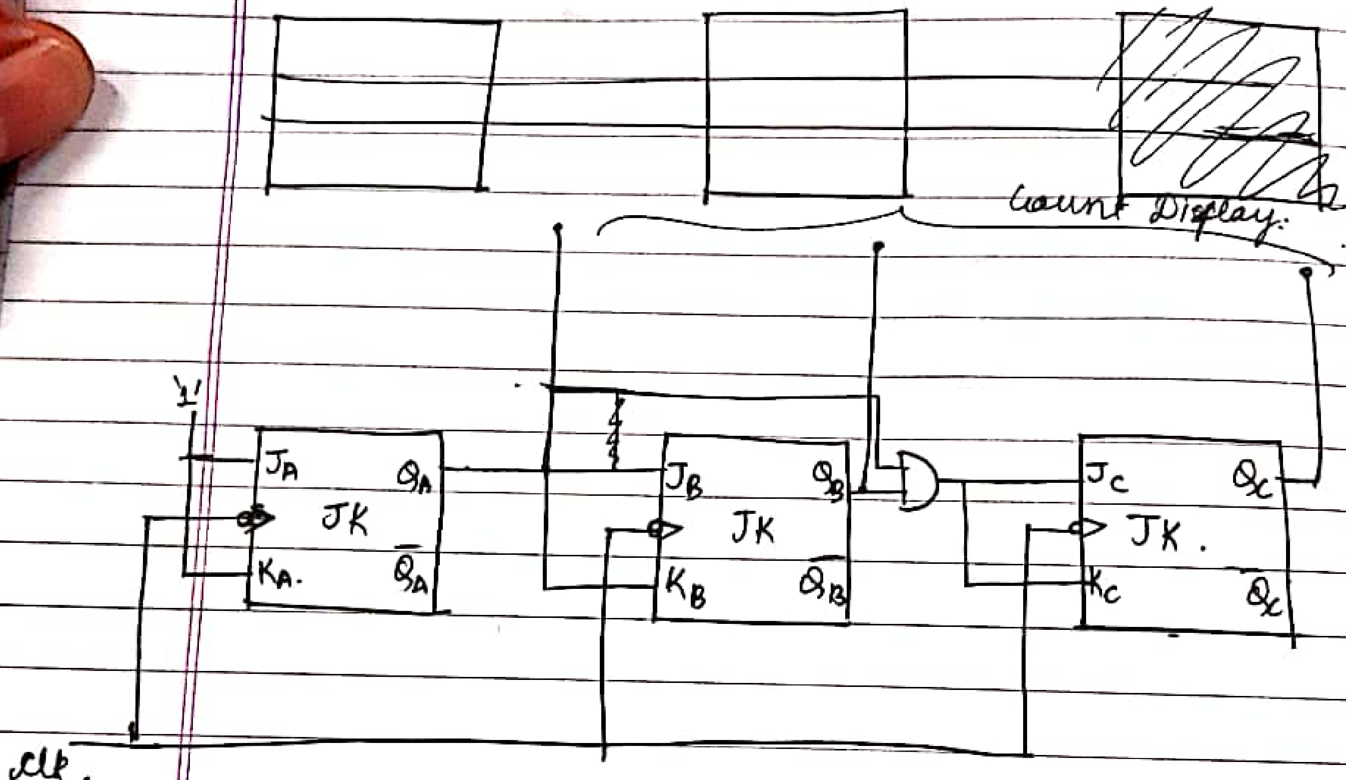
1_0	X_1	X_3	1_2
1_4	X_5	X_7	1_6

$J_A = 1$

$Q_B Q_A$.

$J_C = Q_B Q_A$ $\quad$ $J_B = Q_A$ $\quad$ $J_A = 1$

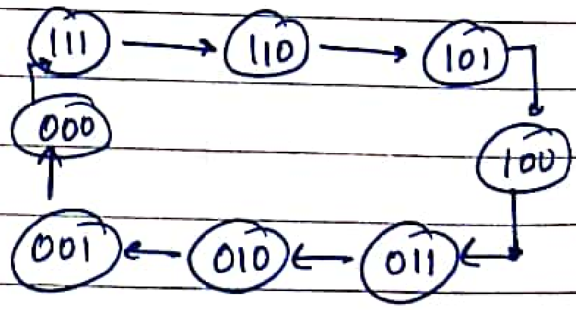
$K_C = Q_B Q_A$ $\quad$ $K_B = Q_A$ $\quad$ $K_A = 1$.



→ MOD - 8 Down Counter (using T).

3T- FF.

Q_n	Q_{n+1}	T.
0	0	0
0	1	1
1	0	1
1	1	0



Q_{C+1}	Q_{B+1}	Q_{A+1}
1	1	0
1	0	1
1	0	0
0	1	1
0	1	0
0	0	1
0	0	0
1	1	1

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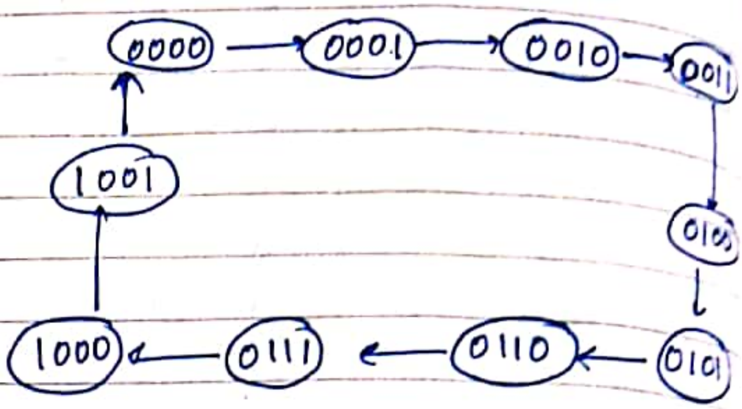
(2). MOD-10 Synchronous up counter.
9 stages 4 FF's.
(0000 → 1001).

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0



	Q_D	Q_C	Q_B	Q_A	Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_D	T_C	T_B	T_A
0	0	0	0	0	0	0	0	1	0	0	0	1
1	0	0	0	1	0	0	1	0	0	0	1	1
2	0	0	1	0	0	0	1	1	0	0	0	1
3	0	0	1	1	0	1	0	0	0	1	1	1
4	0	1	0	0	0	1	0	1	0	0	0	1
5	0	1	0	1	0	1	1	0	0	0	1	1
6	0	1	1	0	0	1	1	1	0	0	0	1
7	0	1	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	1	0	0	1	0	0	0	1
9	1	0	0	1	0	0	0	0	1	0	0	1
10	1	0	1	0	X	X	X	X	X	X	X	X
11	1	0	1	1	X	X	X	X	X	X	X	X
12	1	1	0	0	X	X	X	X	X	X	X	X
13	1	1	0	1	X	X	X	X	X	X	X	X
14	1	1	1	0	X	X	X	X	X	X	X	X
15.	1	1	1	1	X	X	X	X	X	X	X	X.

$T_D = \Sigma m(7, 9) + \Sigma d(10, 11, 12, 13, 14, 15)$

$T_C = \Sigma m(3, 7) +$ "

$T_B = \Sigma m(1, 3, 5, 7) +$ "

$T_A = \Sigma m(0, 1, 2, 3, 4, 5, 6, 7, 8, 9) +$ "

$Q_D Q_C$ \ $Q_B Q_A$	00	01	11	10
00				
01			1	
11	X	X	X	X
10		1	X	X

$T_D = Q_D Q_A + Q_C Q_B Q_A$.

$Q_D Q_C$ \ $Q_B Q_A$	00	01	11	10
00			1	
01			1	
11	X	X	X	X
10			X	X

$T_C = Q_B Q_A$.

		1	1	
		1	1	
	X	X	X	X
			X	X

$T_B = \overline{Q_D} Q_A$.

	1	1	1	1
	1	1	1	1
	X	X	X	X
	1	1	X	X

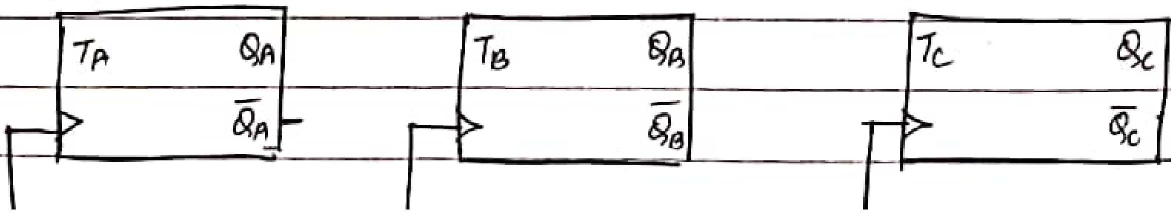
$T_A = 1$.

MOD-8 Synchronous even counter · using D-flip flop.

8 stages (000 ⟶ 111). ·3 flip-flops.

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	D_C	D_B	D_A
0	0	0	0	0	0	1	0	0	1
1	~~0~~	~~0~~	~~1~~	X	X	X	X	X	X
2	0	1	0	0	1	1	0	1	1
3	0	1	1	X	X	X	X	X	X
4	1	0	0	1	0	1	1	0	0
5	1	0	1	X	X	X	X	X	X
6	1	1	0	1	1	1	1	1	1
7	1	1	1	X	X	X	X	X	X
8									



MOD-8.

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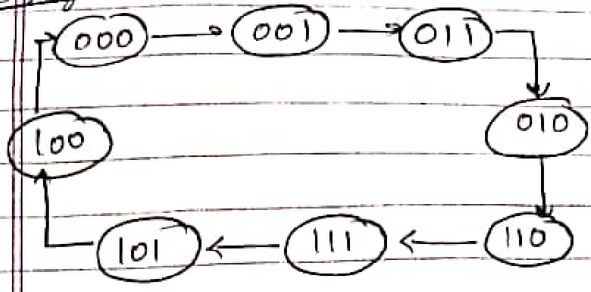
Design a 3-bit Gray counter (synchronous).
↳ 8 States (000-111) (No. of ff's = 3) → $Q_C\,Q_B\,Q_A$.

State Diagram.



Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

	Q_C (4)	Q_B (2)	Q_A (1)	
0	0	0	0	000
1	0	0	1	001
2	0	1	0	011
3	0	1	1	010
4	1	0	0	110
5	1	0	1	111
6	1	1	0	101
7	1	1	1	100.

	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_C	T_B	T_A
0	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	1	0	1	0
3	0	1	1	0	1	0	0	0	1
2	0	1	0	1	1	0	1	0	0
6	1	1	0	1	1	1	0	0	1
7	1	1	1	1	0	1	0	1	0
5	1	0	1	1	0	0	0	0	1
4	1	0	0	0	0	0	1	0	0.

$T_C = \Sigma m(2, 4)$

$T_B = \Sigma m(1, 7)$

$T_A = \Sigma m(0, 3, 6, 5).$

$Q_C \backslash Q_BQ_A$	00	01	11	10
0	0	1	3	1_2
1	1_4	5	7	6

$T_C = \overline{Q}_C Q_B \overline{Q}_A + Q_C \overline{Q}_B \overline{Q}_A$.

	0	1_1	3	2
	4	5	1_7	6

$T_B = \overline{Q}_C \overline{Q}_B Q_A + Q_C Q_B Q_A$

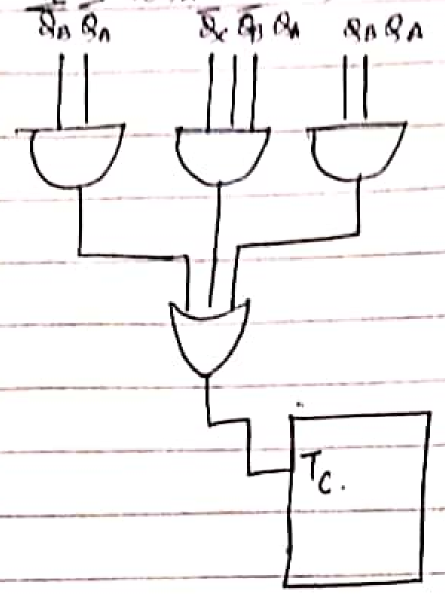
	$\overline{Q}_B\overline{Q}_A$	$\overline{Q}_B Q_A$	$Q_B Q_A$	$Q_B \overline{Q}_A$
$\overline{Q}_C$	1_0	1	1_3	2
Q_C	4	1_5	7	1_6

$T_A = \overline{Q}_C \overline{Q}_B \overline{Q}_A + Q_C \overline{Q}_B Q_A + \overline{Q}_C Q_B Q_A + Q_C Q_B \overline{Q}_A$.

Design a 3-bit synchronous up-down counter.
Design a MOD-8 even/odd D-FF.

Example:

$T_C = \bar{Q}_B\bar{Q}_A + Q_C\bar{Q}_B Q_A + Q_B Q_A$.



Design a synchronous counter which gives following O/P sequence: 0, 1, 7, 4, 9, 12, 3, 6, 15, 2.

Avoid lock out condn.

We want till 26 when 27 is there we want zero.

$27 \rightarrow (11011)$ MSB (Q_E) LSB (Q_A).

$\boxed{Q_E Q_D Q_B Q_A} \rightarrow$ must be zero

Clear.

MOD-27 Asynchronous / Ripple up counter.

count Display.