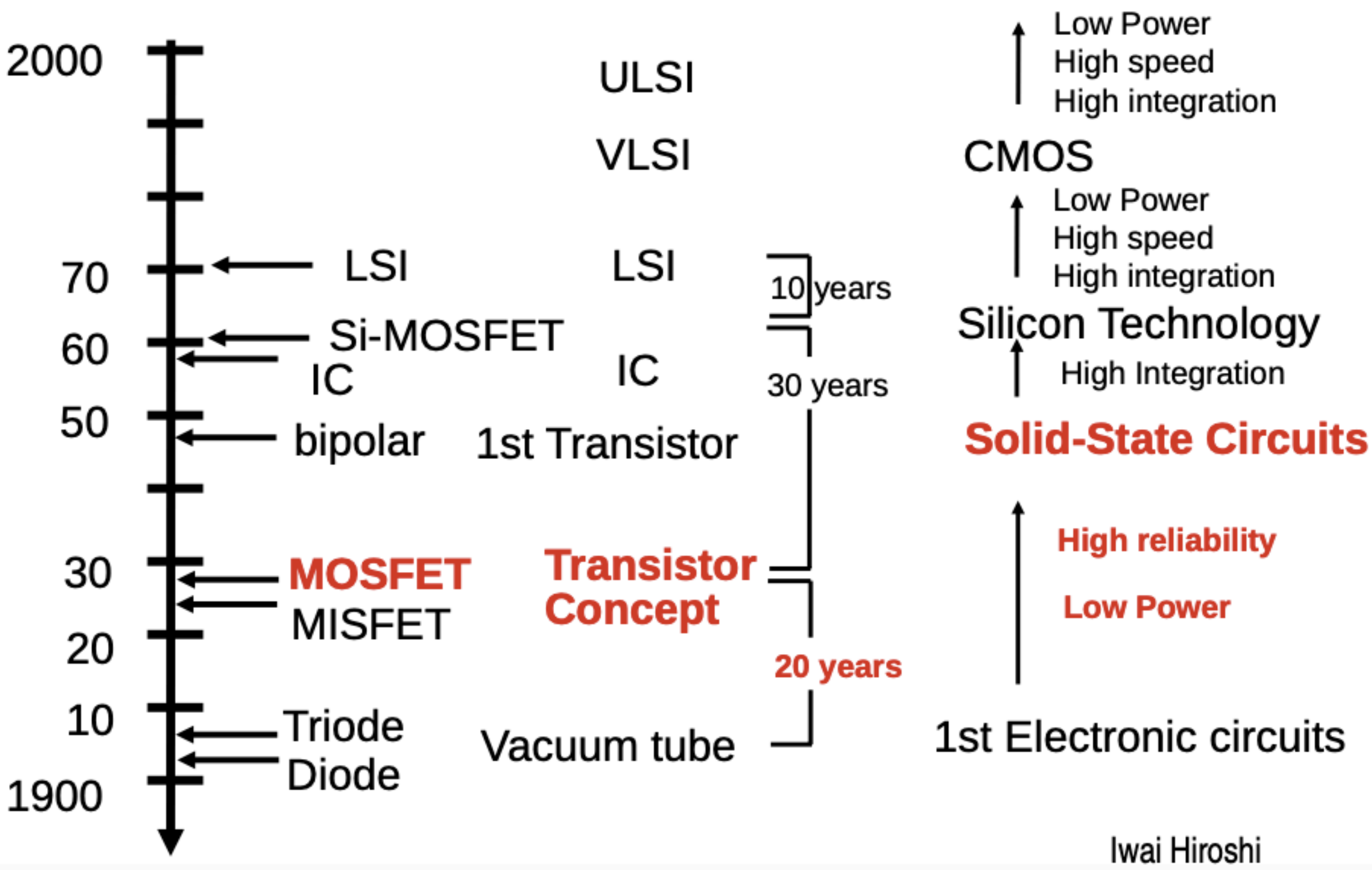
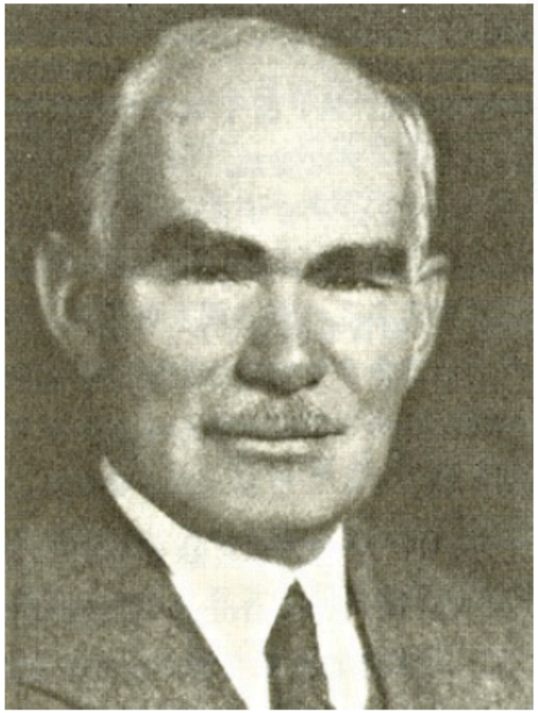
VLSI TECHNOLOGY

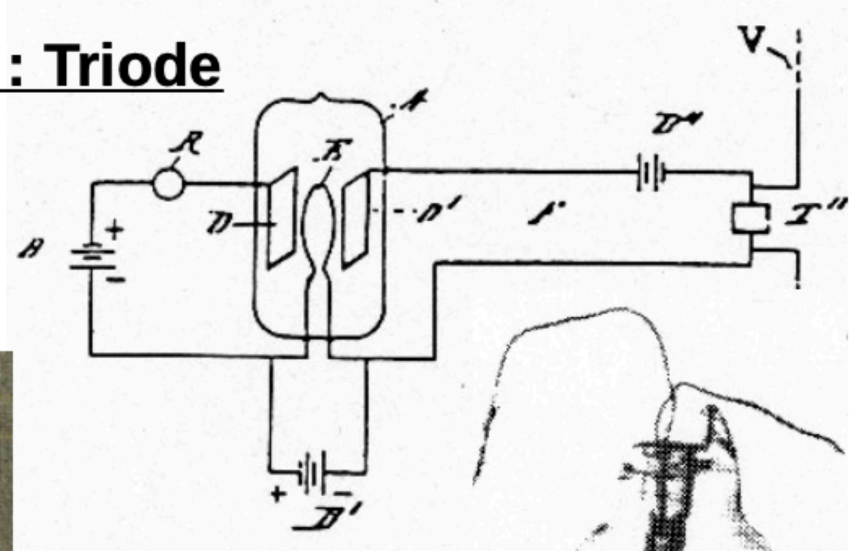
History of Electronic Devices

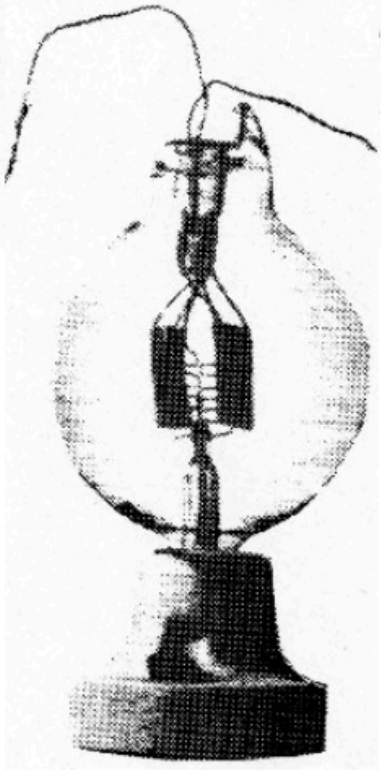


1906: Vacuum Tube : Triode

Lee De Forest





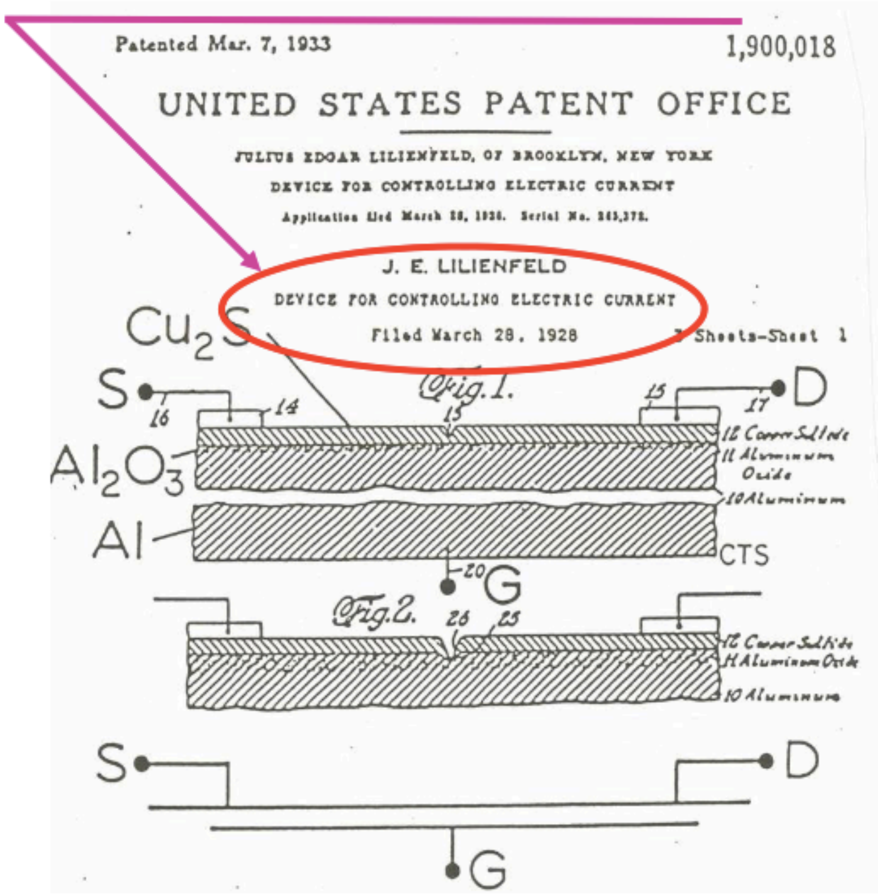


Iwai Hiroshi

J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928

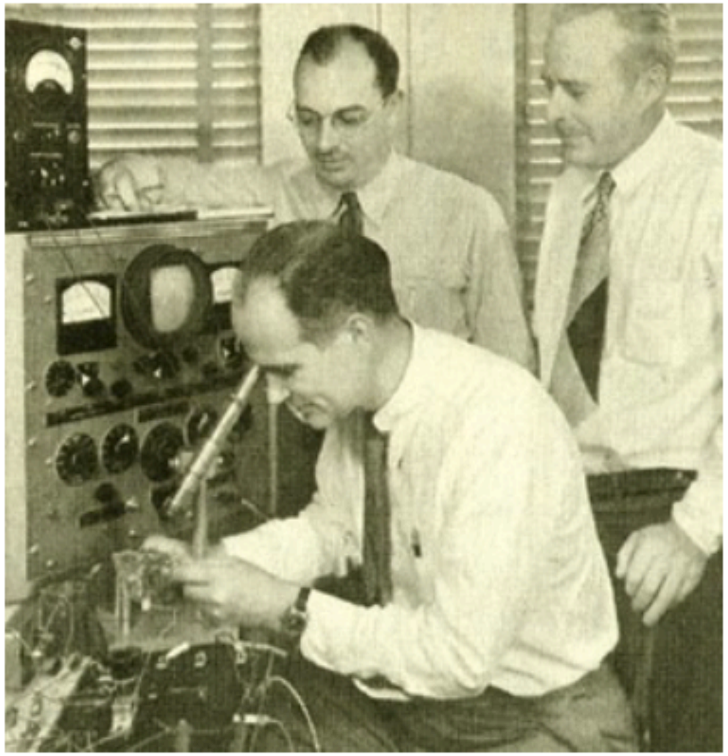


J.E.LILIENFELD

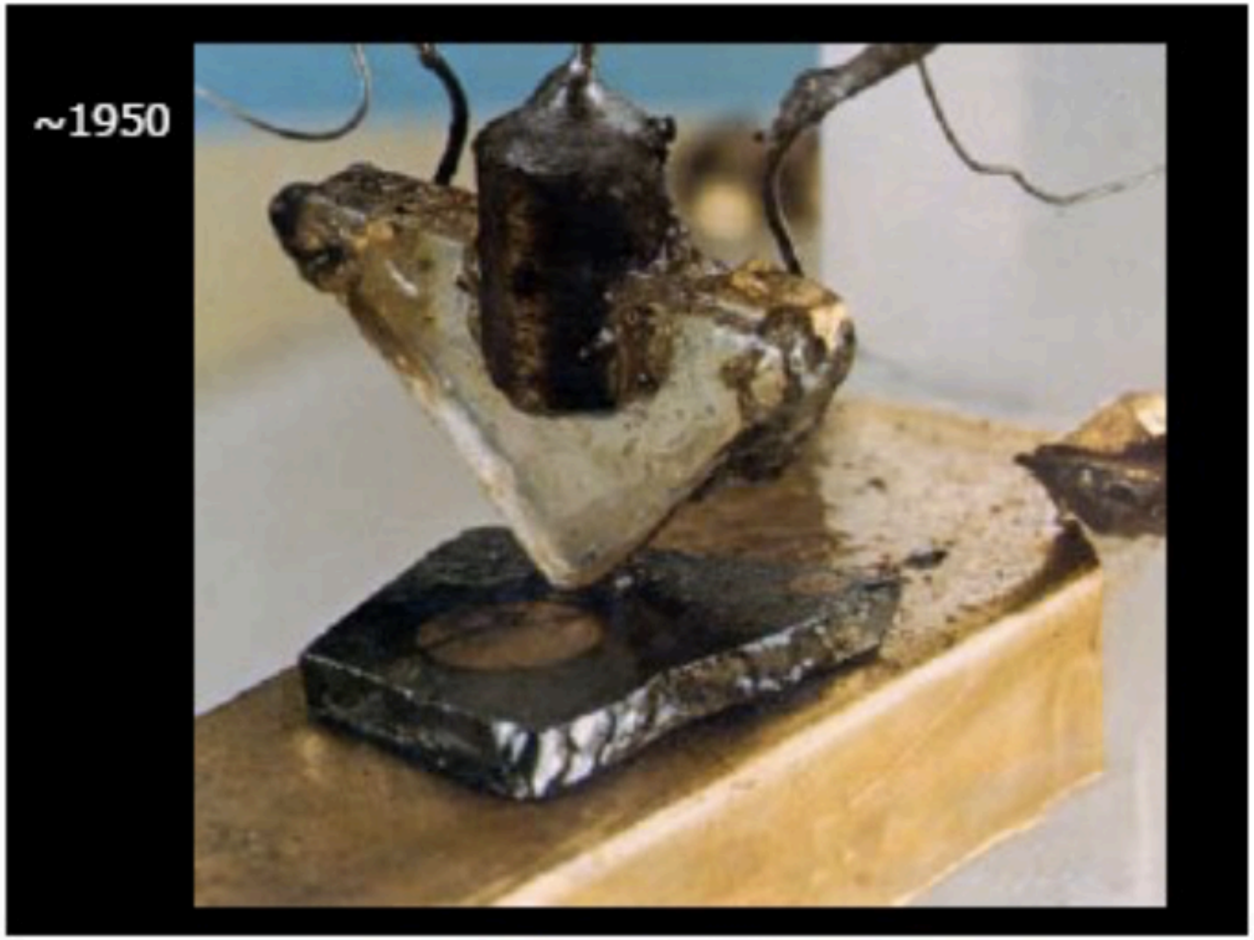
1947: 1st transistor

J. Bardeen, W. Bratten,

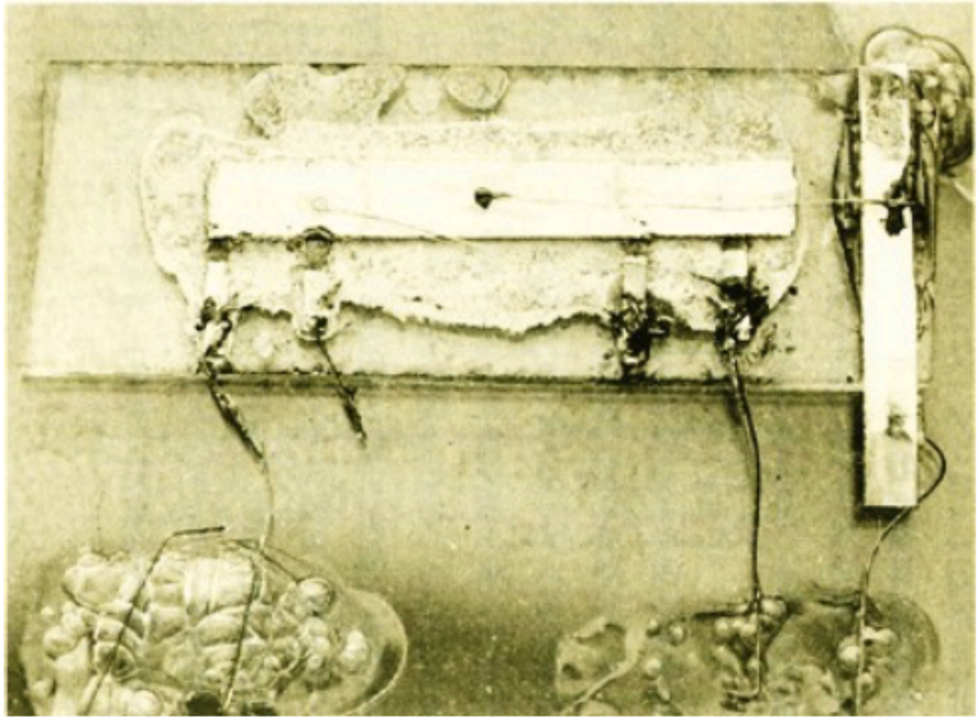
W. Shockley



First Bipolar Ge Transistor



<u>1958: 1st Integrated Circuit</u>

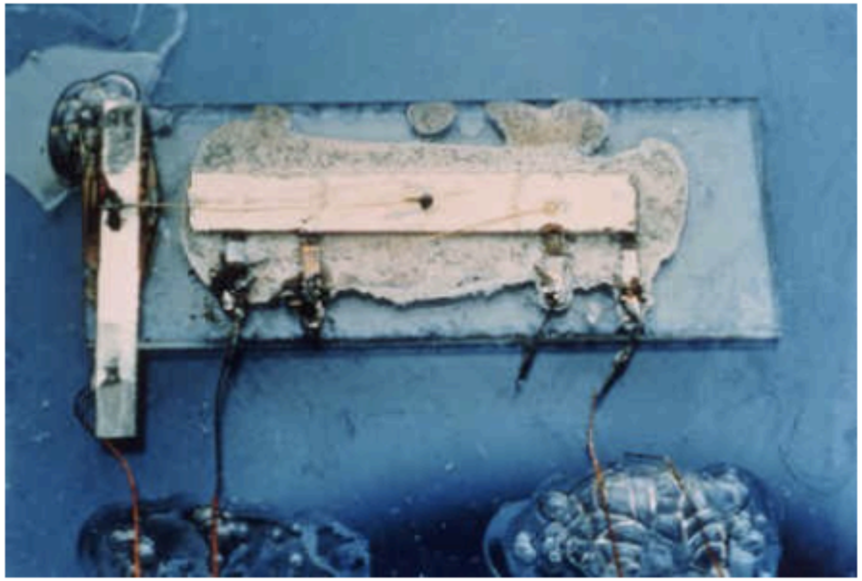


Jack S. Kilby

1958 - Integrated circuit invented

September 12th 1958 Jack Kilby at Texas instrument had built a simple oscillator IC with five integrated components (resistors, capacitors, distributed capacitors and transistors)

In 2000 the importance of the IC was recognized when Kilby shared the Nobel prize in physics with two others. Kilby was sited by the Nobel committee "for his part in the invention of the integrated circuit



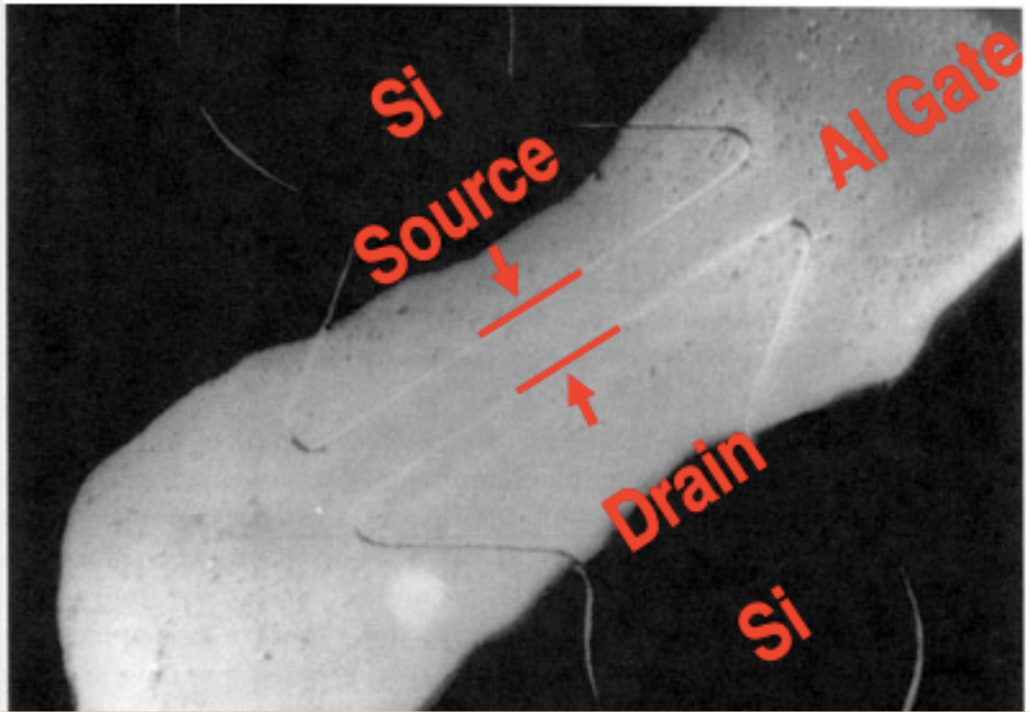
a simple oscillator IC

- Ten years later, Jack Kilby at Texas Instruments realized the potential for miniaturization if multiple transistors could be built on one piece of silicon.
- first prototype of an integrated circuit, constructed from a germanium slice and gold wires.
- The invention of the transistor earned the Nobel Prize in Physics in 1956 for Bardeen, Brattain, and their supervisor William Shockley. Kilby received the Nobel Prize in Physics in 2000 for the invention of the integrated circuit.

- Transistors can be viewed as electrically controlled switches with a control terminal and two other terminals that are connected or disconnected depending on the voltage or current applied to the control.
- Soon after inventing the point contact transistor, Bell Labs developed the bipolar junction transistor. Bipolar transistors were more reliable, less noisy, and more power-efficient.
- Early integrated circuits primarily used bipolar transistors. Bipolar transistors require a small current into the control (base) terminal to switch much larger currents between the other two (emitter and collector) terminals.

1960: First MOSFET
by D. Kahng and M. Atalla

Top View



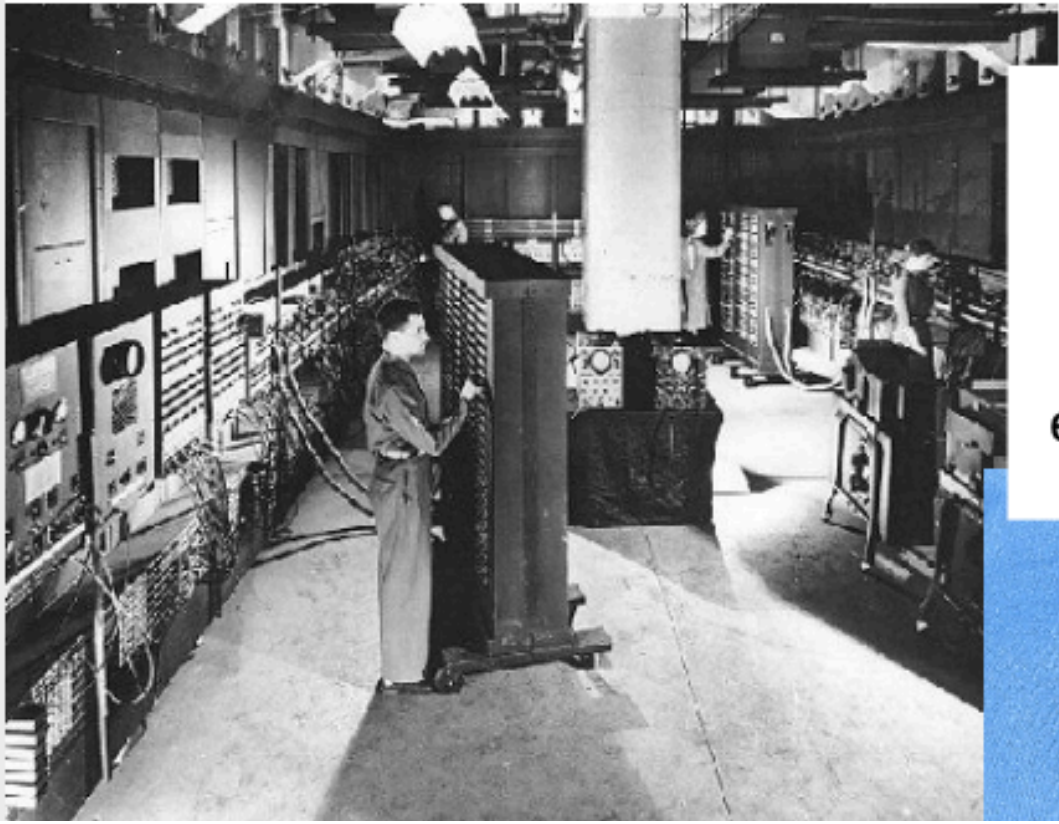
- The quiescent power dissipated by these base currents, drawn even when the circuit is not switching, limits the maximum number of transistors that can be integrated onto a single die.
- By the 1960s, Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) began to enter production.
- MOSFETs offer the compelling advantage that they draw almost zero control current while idle.
- They come in two flavors: nMOS and pMOS, using n-type and p-type silicon, respectively.

- In 1963, Frank Wanlass at Fairchild described the first logic gates using MOSFETs. Fairchild's gates used both nMOS and pMOS transistors, earning the name Complementary Metal Oxide Semiconductor, or CMOS.
- MOS integrated circuits became attractive for their low cost because each transistor occupied less area and the fabrication process was simpler.
- Early commercial processes used only pMOS transistors and suffered from poor performance, yield, and reliability. Processes using nMOS transistors became common in the 1970s.

First Computer Eniac: made of huge number of vacuum tubes 1946

Big size, huge power, short life time filament

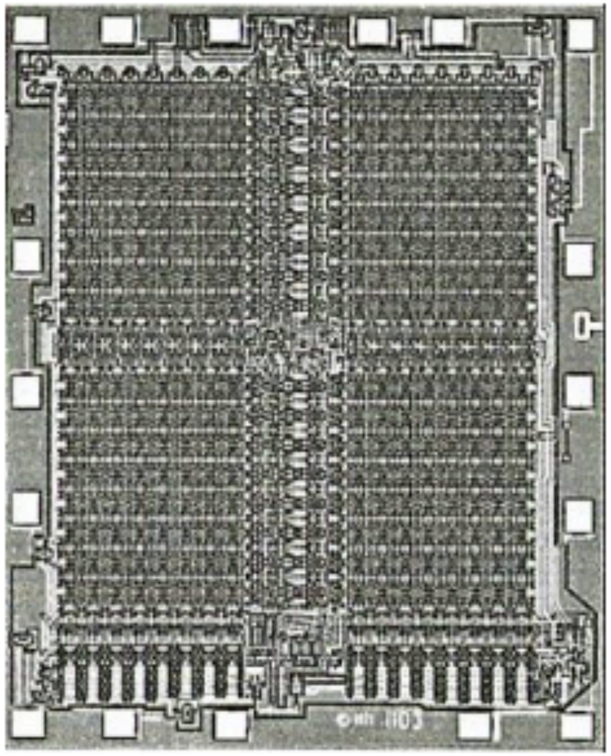
→ dreamed of replacing vacuum tube with solid-state device



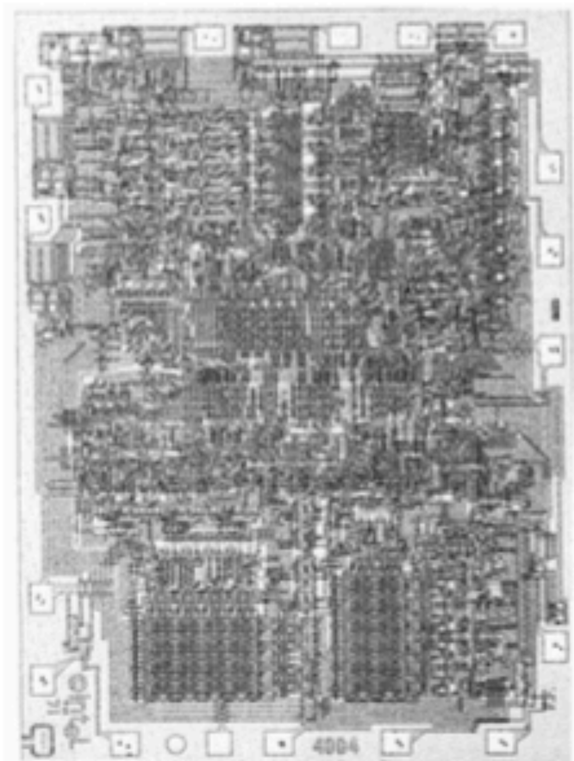
Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption

1970,71: 1st generation of LSIs

DRAM Intel 1103



MPU Intel 4004



In 2012

Most Recent SD Card

128GB (Byte)
= 128G X 8bit
= 1T(Tera)bit

1T = 1012 = 1 Trillion

World Population : 7 Billion
Brain Cell : 10 ~ 100 Billion
Stars in Galaxy : 100 Billion

128 GB = 1Tbit

2.4cm X 3.2cm X 0.21cm

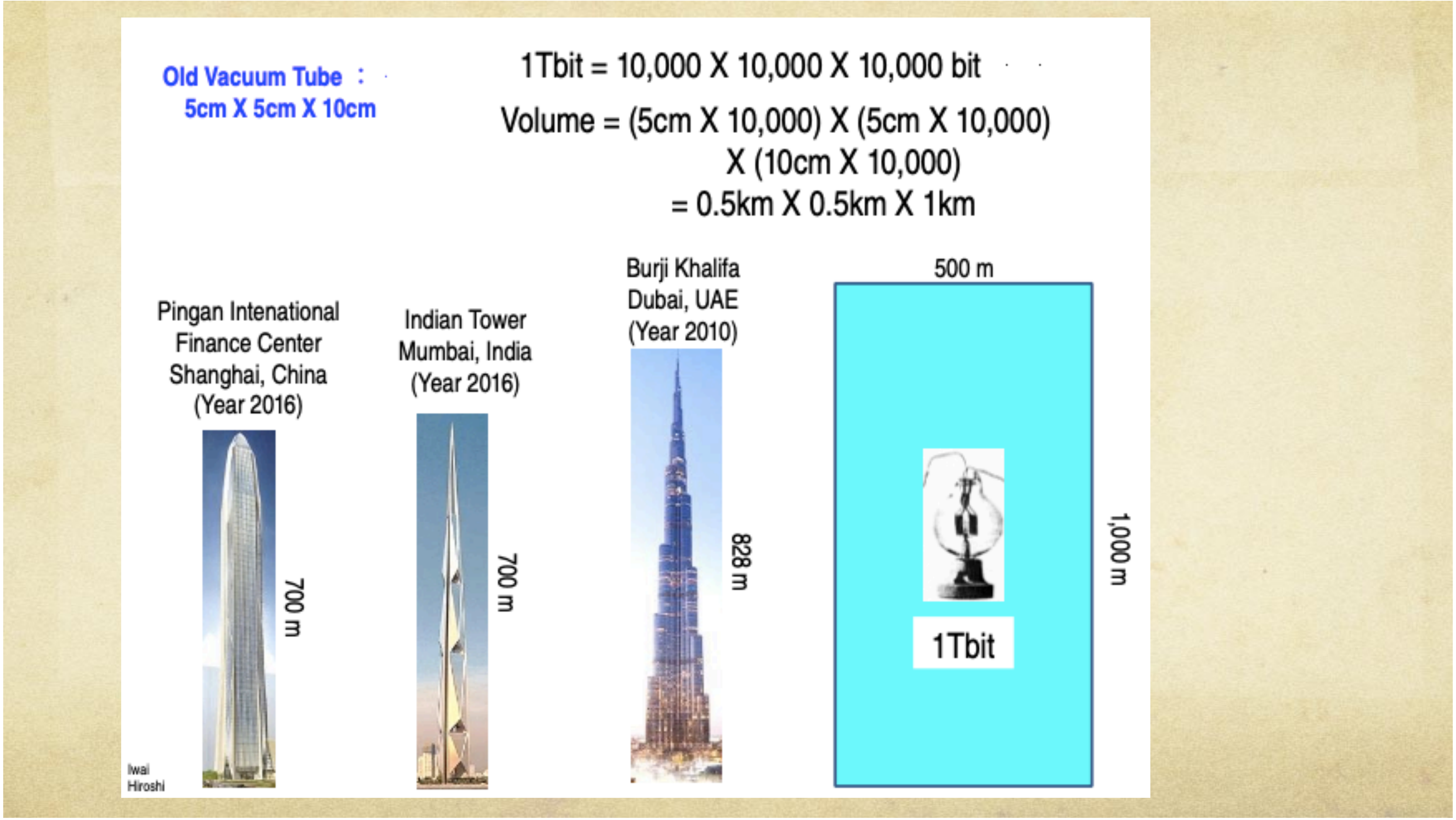
Volume ： 1. 6cm³ Weight ： 2g

Voltage ： 2.7 - 3.6V

Old Vacuum Tube ：

5cm X 5cm X 10cm, 100g, 50W

What are volume, weight, power consumption for 1Tbit


Old Vacuum Tube ：
5cm X 5cm X 10cm
1Tbit = 10,000 X 10,000 X 10,000 bit
Volume = (5cm X 10,000) X (5cm X 10,000)
X (10cm X 10,000)
= 0.5km X 0.5km X 1km
Pingan Intenational
Finance Center
Shanghai, China
(Year 2016)
700 m
Indian Tower
Mumbai, India
(Year 2016)
700 m
Burji Khalifa
Dubai, UAE
(Year 2010)
828 m
500 m
1,000 m
1Tbit
Iwai
Hiroshi

MOORE'S LAW

- In 1965, Gordon Moore observed that plotting the number of transistors that can be most economically manufactured on a chip gives a straight line on a semilogarithmic scale
- he found transistor count doubling every 18 months.
- This observation is called Moore's law
- Moore's Law is driven primarily by *scaling* down the size of transistors and, to a minor extent, by building larger chips.

LEVEL of INTEGRATION

- The level of integration of chips has been classified as small-scale, medium-scale, large-scale, and very large- scale.
- *Small-scale integration* (SSI) circuits, such as the 7404 inverter, have fewer than 10 gates
- *Medium-scale integration* (MSI) circuits, such as the 74161 counter, have up to 1000 gates.
- *Large-scale integration* (LSI) circuits, such as simple 8-bit microprocessors, have up to 10,000 gates

Why integrated circuits?

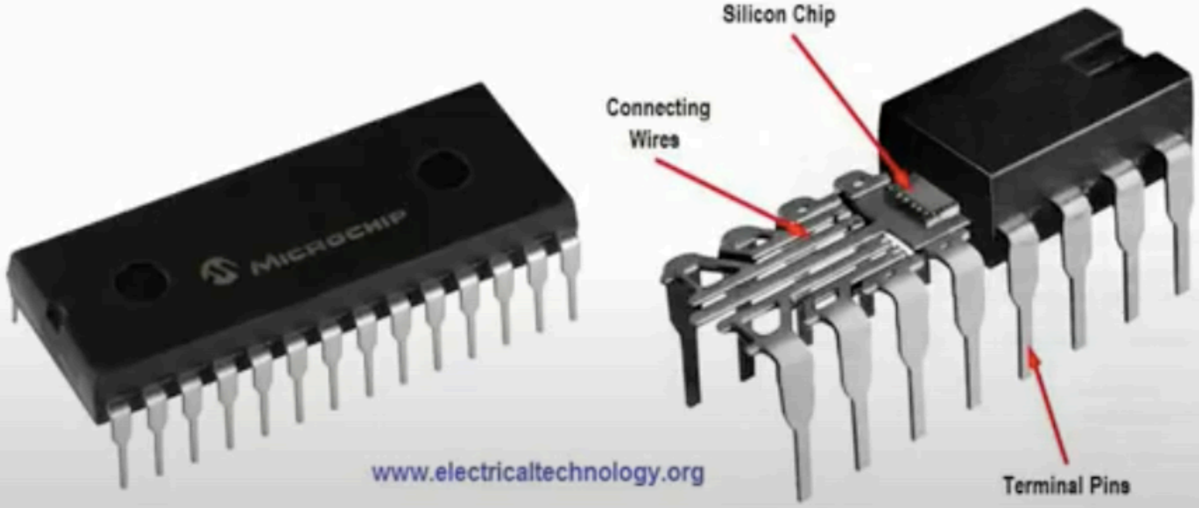
1. Miniaturization and hence increased equipment density.
2. Batch processing resulting in cost reduction.
3. Improved system reliability due to the elimination of soldered joints.
4. Better functional performance.
5. Matched devices.
6. Increased operating speeds.
7. Significant reduction in the power consumption.

ICs can be classified on the basis of their chip size as given below:

Small scale integration (SSI): 3 to 30 gates/chip.
Medium scale integration (MS): I30 to 300 gates/chip.
Large scale integration (LSI): 300 to 3000 gates/chip.
Very large scale integration (VLSI): more than 3000 gates/chip.

Integrated circuit (IC)

An integrated circuit (IC) is a miniaturized low-cost electronic circuit consisting of active and passive components fabricated together on a substrate (silicon). The active components are diodes and transistors while the passive components are resistors and capacitors.



Monolithic Integrated Circuits

The word ‘monolithic’ comes from the Greek words ‘monos’ and ‘lithos’ which means ‘single’ and ’stone’.

The monolithic IC’s refer to a single stone or a single crystal.

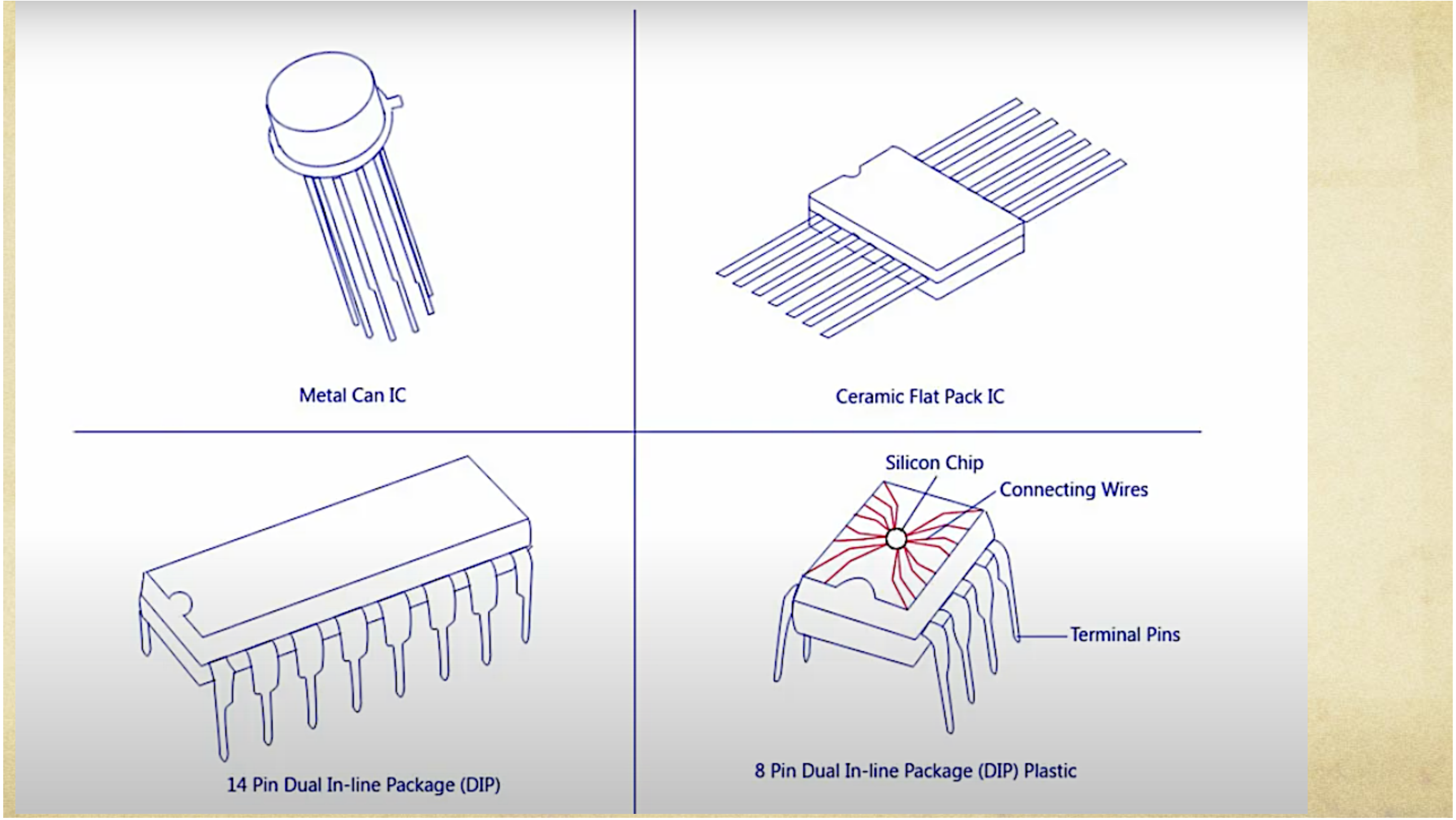
The single crystal refers to a single silicon chip as the semiconductor material, on top of which all the passive and active components are interconnected.

Monolithic Ics are considered as the best mode of manufacturing IC’ as:

1. It can be made identical,
2. High reliability,
3. Manufactured in bulk in very less time,
4. Low Cost,

Monolithic Integrated Circuits: Limitations

- Low power rating.
- Cannot be used for high power applications as it can't have power rating of more than 1 W.
- The isolation between the components within the integrated circuit is poor.
- Components such as inductor can't be fabricated.
- The passive components within the IC will have small value and an external connection is required from the IC pins to obtain high values.
- Flexible circuit is not possible.


Metal Can IC
Ceramic Flat Pack IC
14 Pin Dual In-line Package (DIP)
Silicon Chip
Connecting Wires
Terminal Pins
8 Pin Dual In-line Package (DIP) Plastic

Thin and Thick Film Integrated Circuit

These integrated circuit are larger than monolithic IC's and smaller than discrete circuits.

It can be used in high power applications.

Cannot be integrated with diodes and transistors.

Diodes and transistors if required can be externally connected on to its corresponding pins.

Resistors and capacitors can be integrated.

Thin Film Integrated Circuit

- Fabricated by depositing thin films of conducting/semiconducting materials on the surface of a glass or ceramic base.
- $R = \rho L/A$
- By controlling the thickness and width of the film we can fabricated resistors of different values. Different material will have different resistivity.
- Similarly capacitors can be fabricated by depositing two conducting films separated by an insulating layer. An inductor can be fabricated by depositing spiral form of film onto the IC.

Thick Film Integrated Circui

- Commonly called as printed film circuits.
- A screen printing or silk-screen printing technique used to obtain the desired circuit pattern on ceramic substrate.
- The inks are used for printing the circuits.
- Ink consists of materials that have resistive, dielectr or conductive, properties.
- The screens are actually made of fine stainless ste wire mesh. The films are fused to the substrate aft printing by placing them in hot high temperatu furnaces.

Thick and thin film IC's do have some advantages when compared to monolithic ICs:

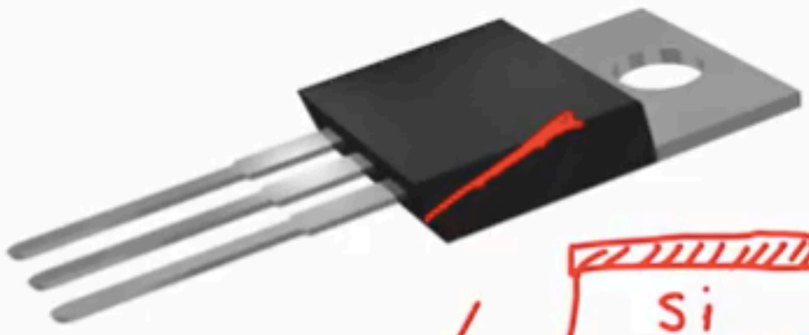
- Better tolerance
- Better isolation between components
- Flexibility in circuit design

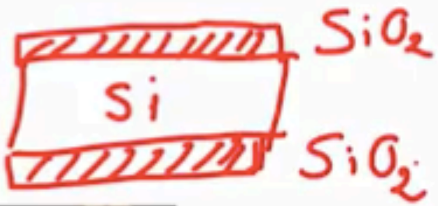
Note: Thick and Thin film IC technology can't be used to fabricate active components as it will further result in increased size.

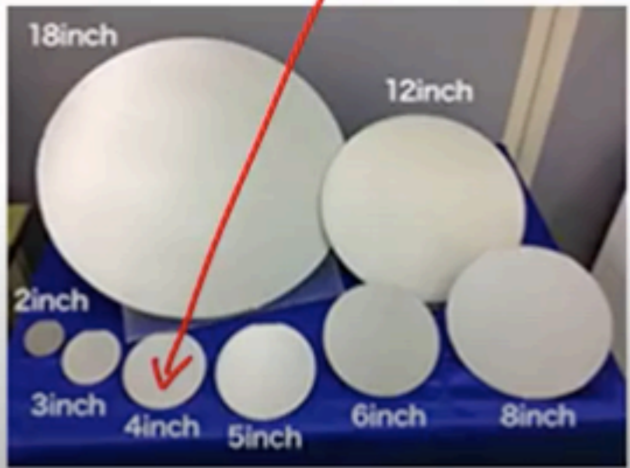
Integrated circuit (IC)

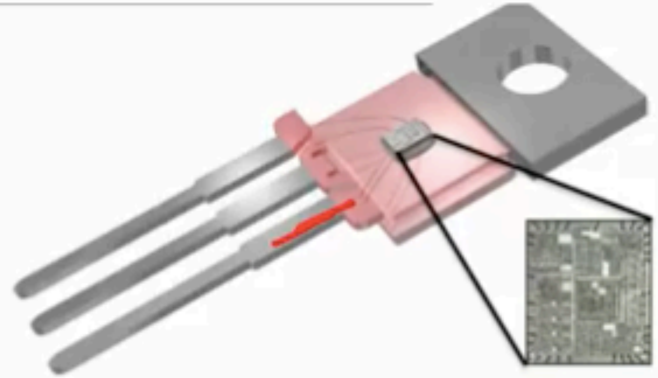
- Substrates: Silicon, Glass, and Plastic
- Microelectronic chips used semiconductor material as a substrate
- For more than 95% of all semiconductor devices fabricated, silicon is the leading semiconductor material
- Silicon substrate can be divided into four basic steps:

1. Production of electronic grade silicon
2. Crystal growing
3. Polishing of Silicon crystal
4. Slicing of Si wafers


ON semiconductor

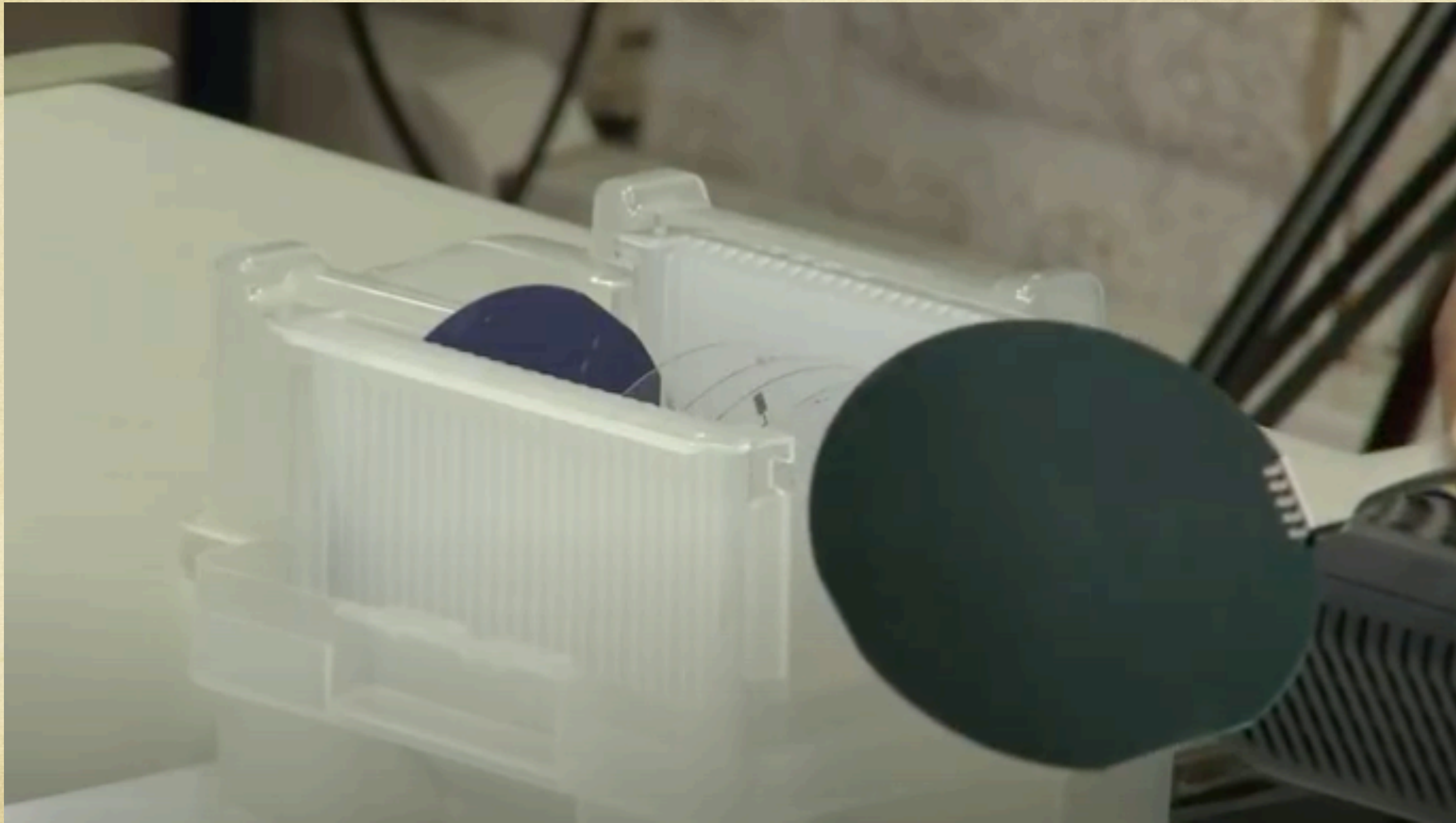


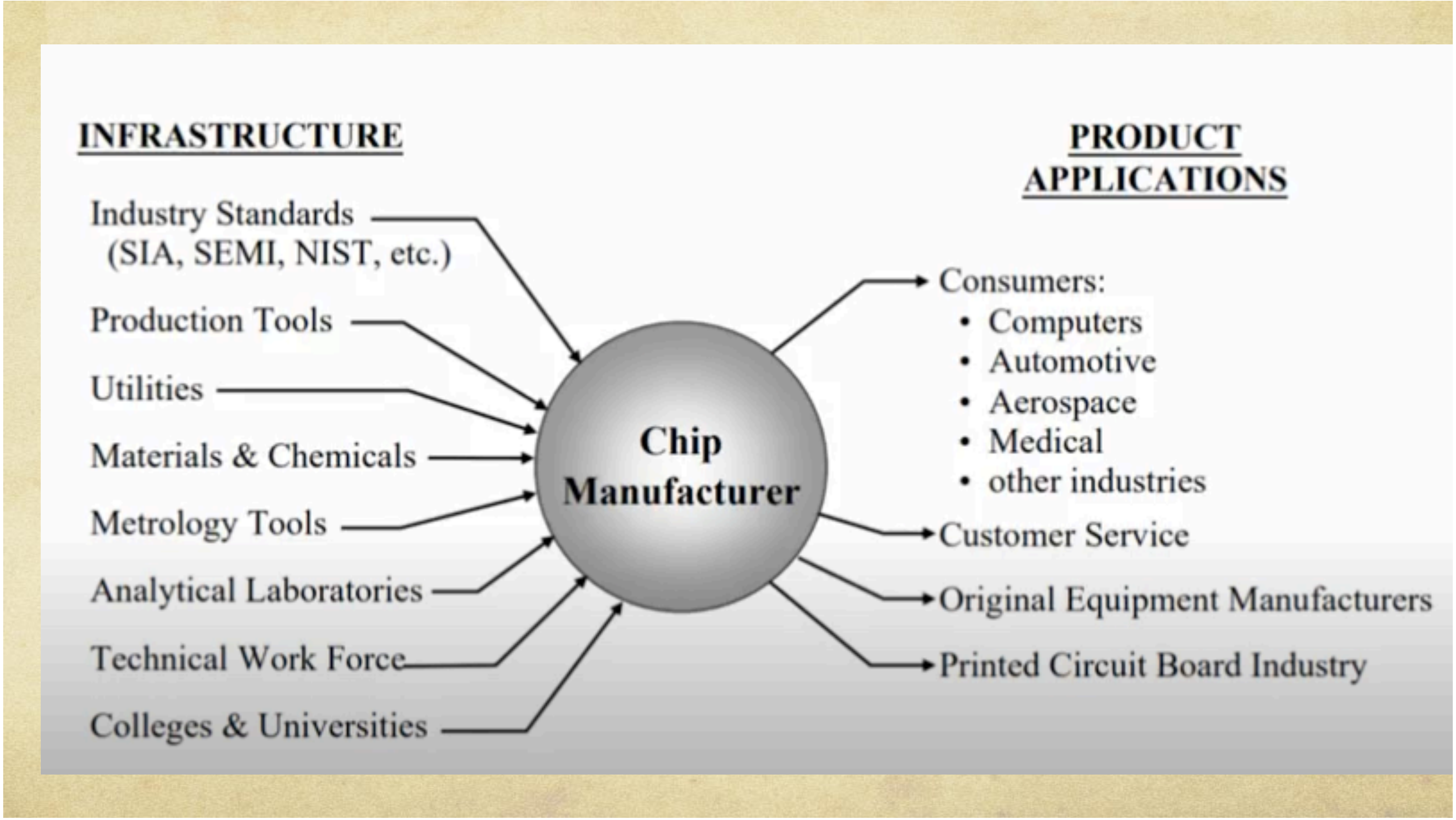


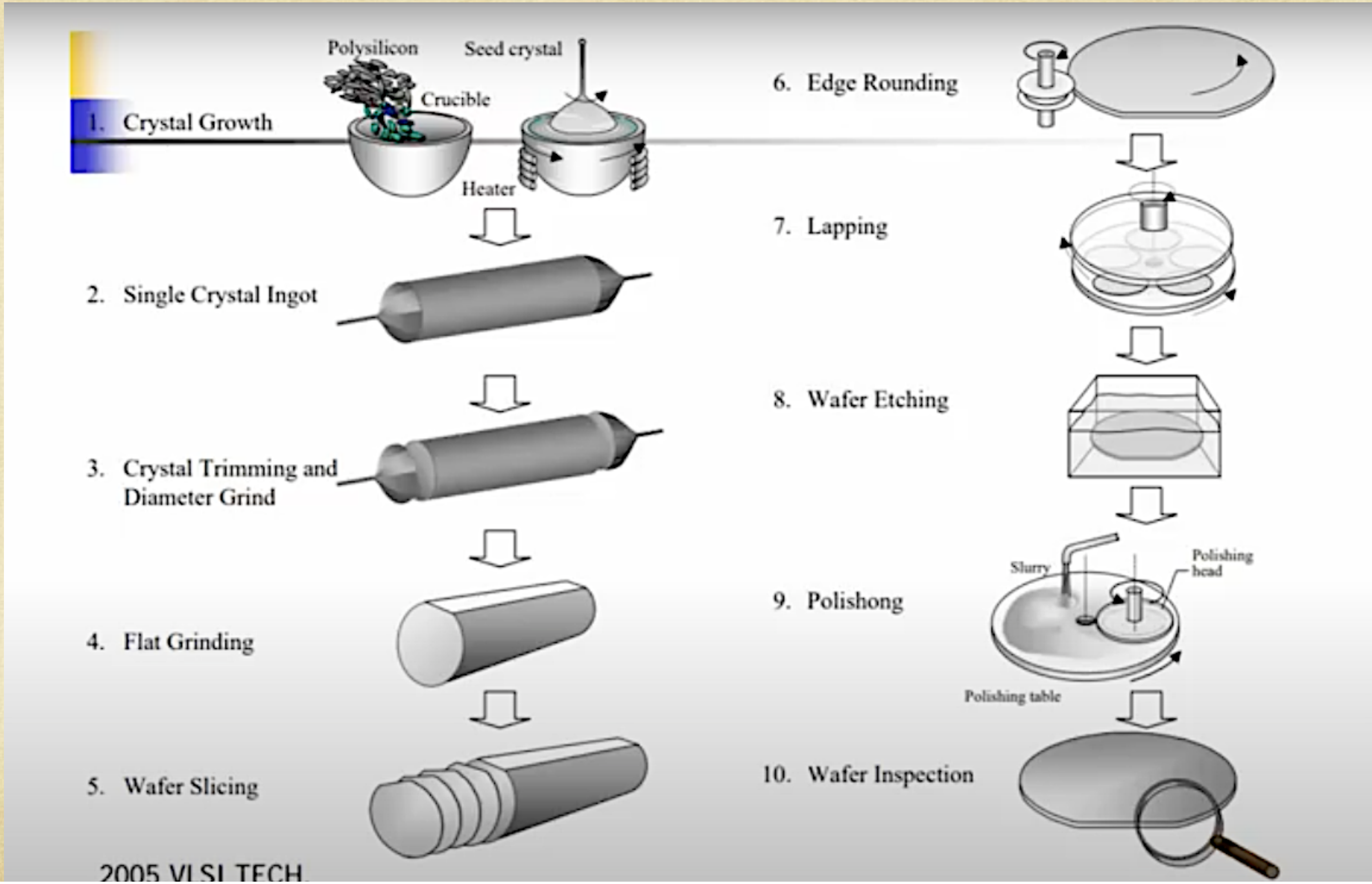

Google image

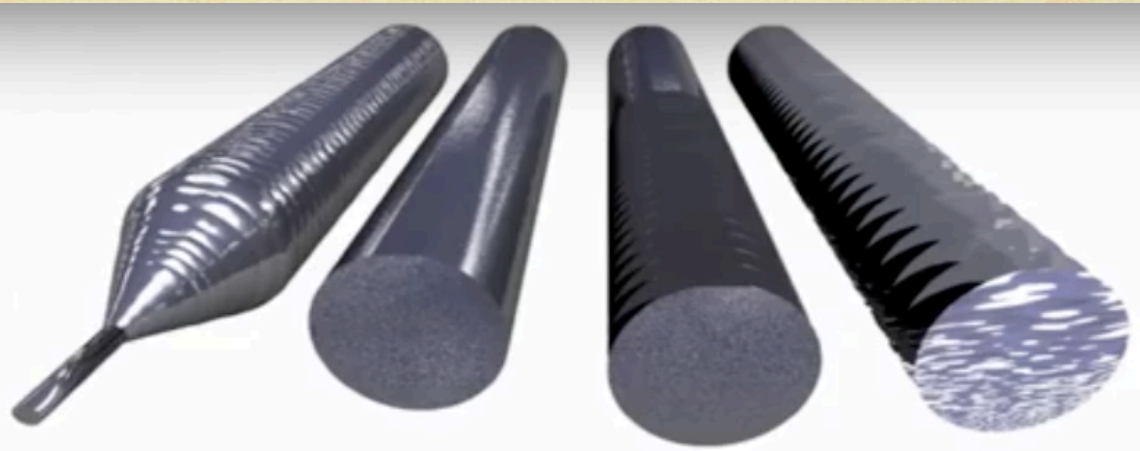
On removing the black box, what can we see?

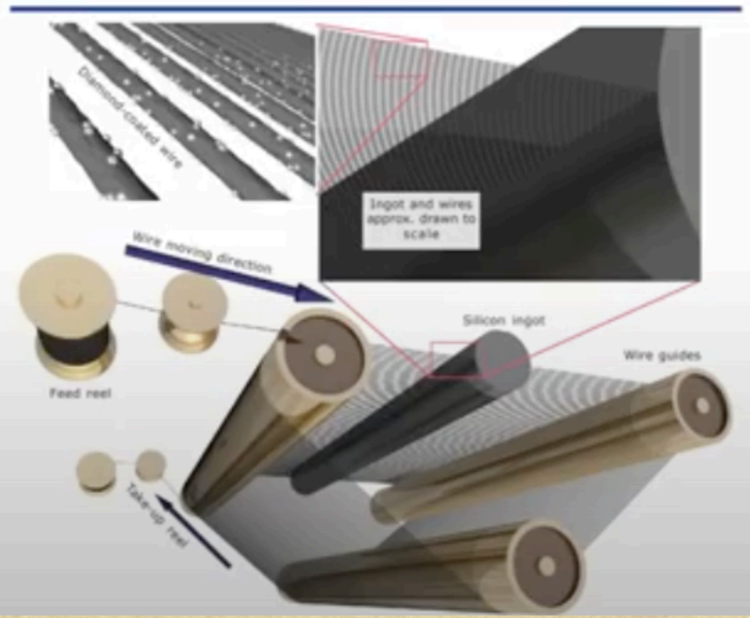
Wire-bonding from the silicon chip to the leads

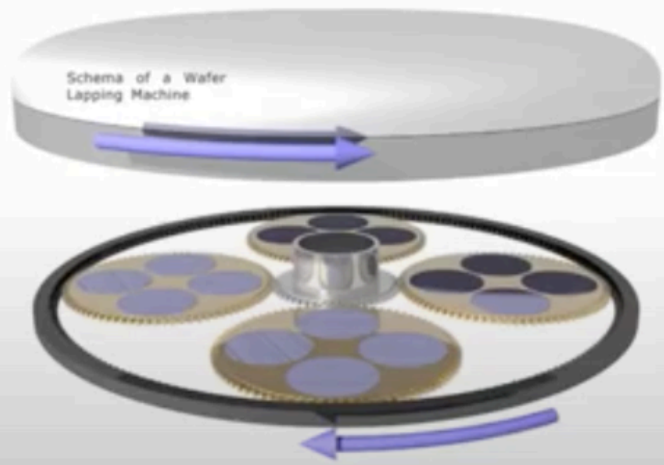


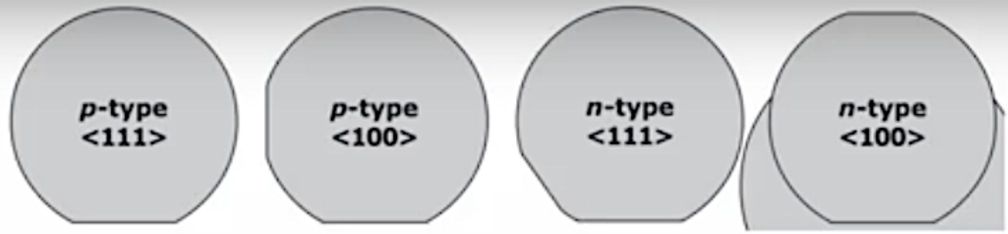

INFRASTRUCTURE
Industry Standards (SIA, SEMI, NIST, etc.)
Production Tools
Utilities
Materials & Chemicals
Metrology Tools
Analytical Laboratories
Technical Work Force
Colleges & Universities
Chip Manufacturer
PRODUCT APPLICATIONS
Consumers:
• Computers
• Automotive
• Aerospace
• Medical
• other industries
Customer Service
Original Equipment Manufacturers
Printed Circuit Board Industry

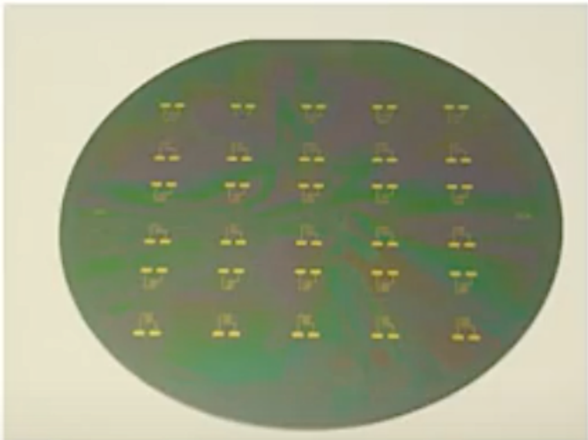

Polysilicon
Seed crystal
Crucible
1. Crystal Growth
Heater
2. Single Crystal Ingot
3. Crystal Trimming and Diameter Grind
4. Flat Grinding
5. Wafer Slicing
6. Edge Rounding
7. Lapping
8. Wafer Etching
9. Polishong
Slurry
Polishing head
Polishing table
10. Wafer Inspection
2005 VLSI TECH.

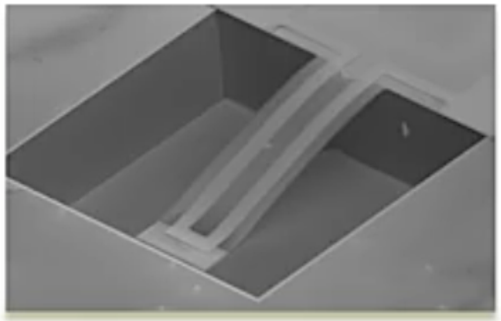


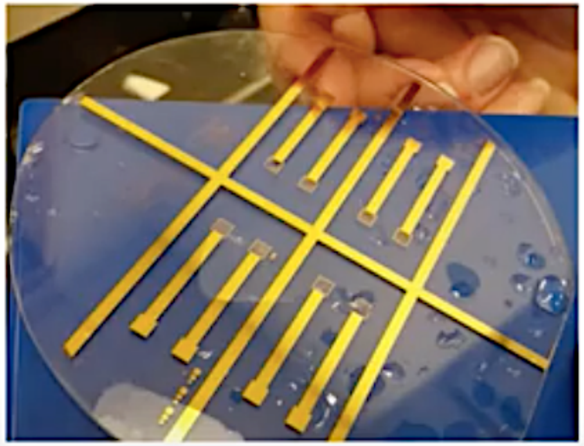

Diamond-coated wire
Ingot and wires approx. drawn to scale
Wire moving direction
Silicon ingot
Wire guides
Feed reel
Take-up reel

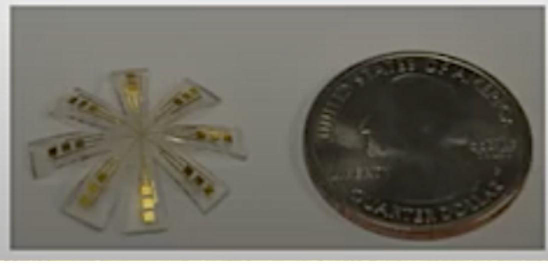

Schema of a Wafer Lapping Machine


p-type <111>
p-type <100>
n-type <111>
n-type <100>

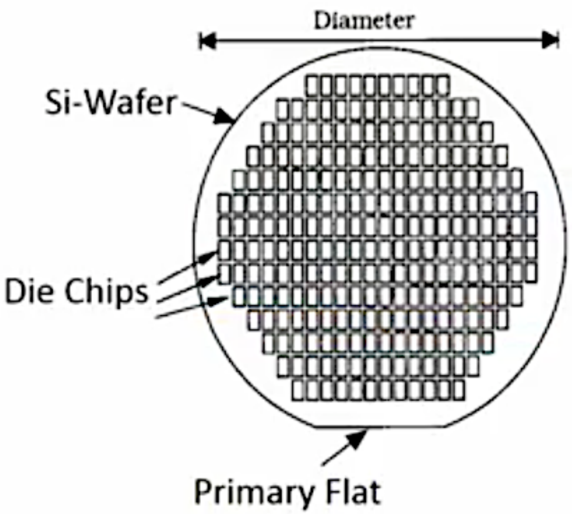






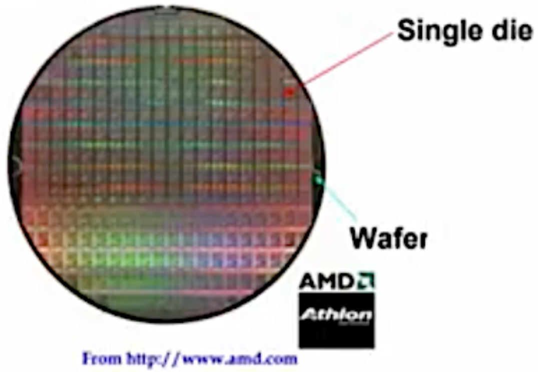


Silicon Processing - Wafers



Si ICs are created on large circular sheets of Si called wafers

- 100-300mm in diameter
- ~ 0.7 mm thick



Si IC is ~ 1 cm on a side

- Many ICs on a single wafer

Location of an IC on a wafer is called a die site

A flat on the wafer is used as a reference plane to form a grid for die placement

The number of wafer starts per week indicates the manufacturing capacity of a chip factory

How many fresh wafers are introduced into the fabrication sequence shows the number of wafer starts

Wafers are processed in groups

Typically it takes several weeks for a lot to pass the entire processing line

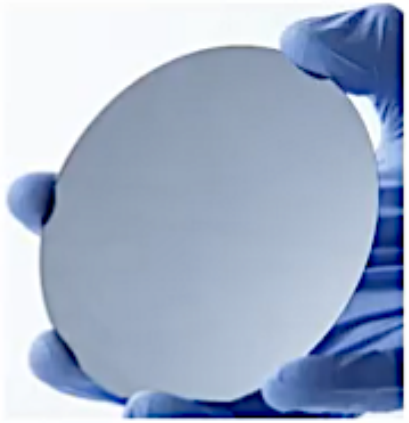
Silicon

http://mrsec.wisc.edu
en.wikipedia.org

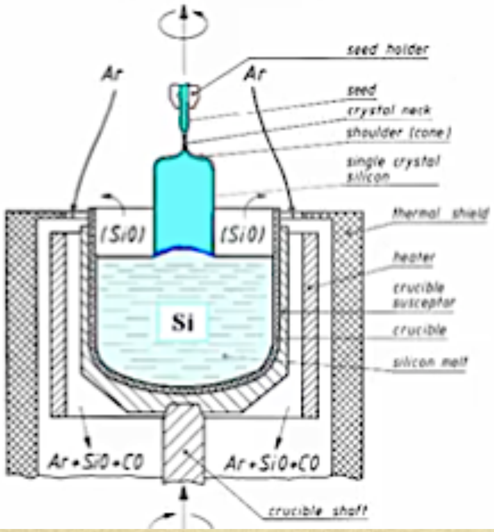
Silicon Boule and Wafers

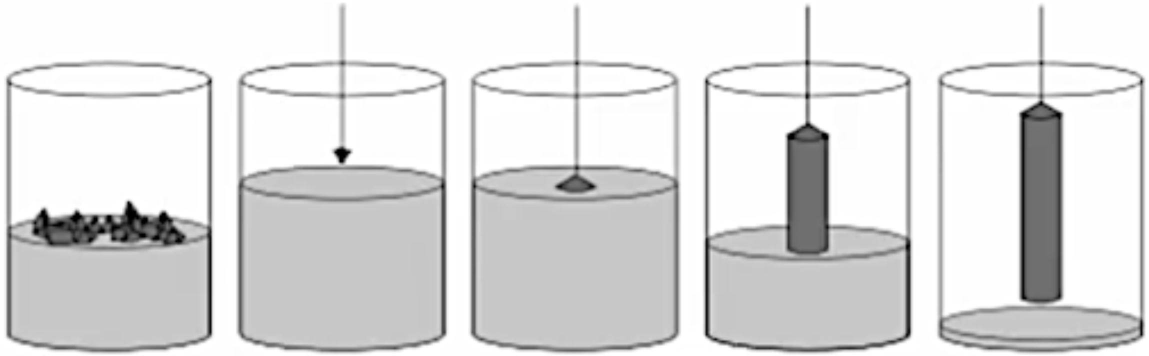
Wafers are cut from *boules*, which are large logs of uniform silicon.

Looking at this picture, *where* do you think silicon boules are made? Why do you think so?

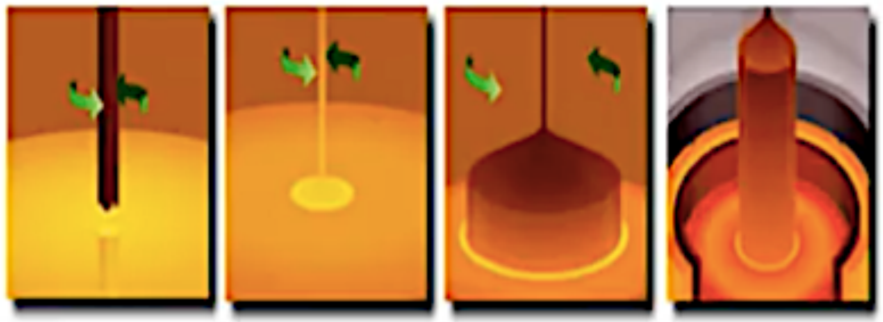


Beginning of crystal growth





Melting of polysilicon | Introduction of seed crystal | Beginning of crystal growth | Crystal pulling | Formed crystal



http://www.youtube.com/watch?v=aWVywhzuHnQ

The Starting Material…

- SiO_2 react with C (coke) at about 1800˚C to form *Metallurgical grade Si* ***(MGS)*** with impurities like Fe, Al.

$$SiO_2 + 2C \rightarrow Si + 2CO\uparrow$$

- This MGS is refined further to obtain the *Electronic grade Si* ***(EGS)*** as per following two reactions.

$$Si + 3HCl \rightarrow SiHCl_3 + H_2\uparrow$$

$$2SiHCl_3 + 2H_2 \rightarrow 2Si + 6HCl$$

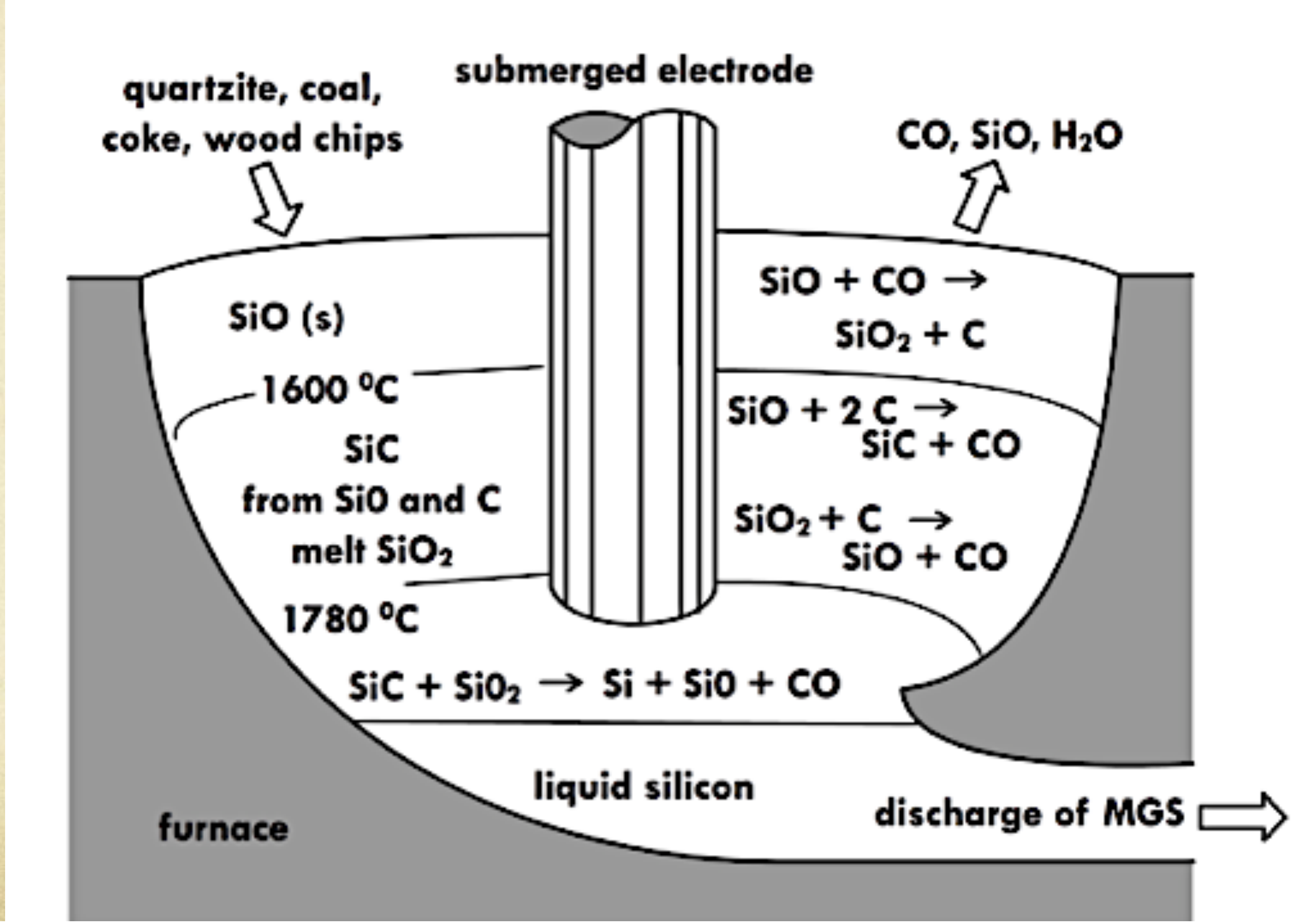
Electronic –Grade Silicon

- EGS is a poly crystalline material of high purity.
- It is a raw material for preparation of Single-crystal silicon.
- Major impurities are boron, carbon and residual donors.
- In pure EGS the doping elements should be in parts per billion(ppb) range.
- To obtain EGS multistep process is required.
- To get EGS, starting material is Metallurgical grade Silicon (MGS)

- Metallurgical grade silicon(MGS) is produced in a submerged-electrode arc furnace.
- The furnace is charged with quartize, a relatively pure form of sand(SiO_2) and carbon in the form of coal, coke and wood chips.
- In the furnace a number of reactions take place, overall reaction being

$$SiC(solid) + SiO_2(solid) \longrightarrow Si(liquid) + SiO(gas) + CO(gas)$$

Submerged Electrode arc furnace



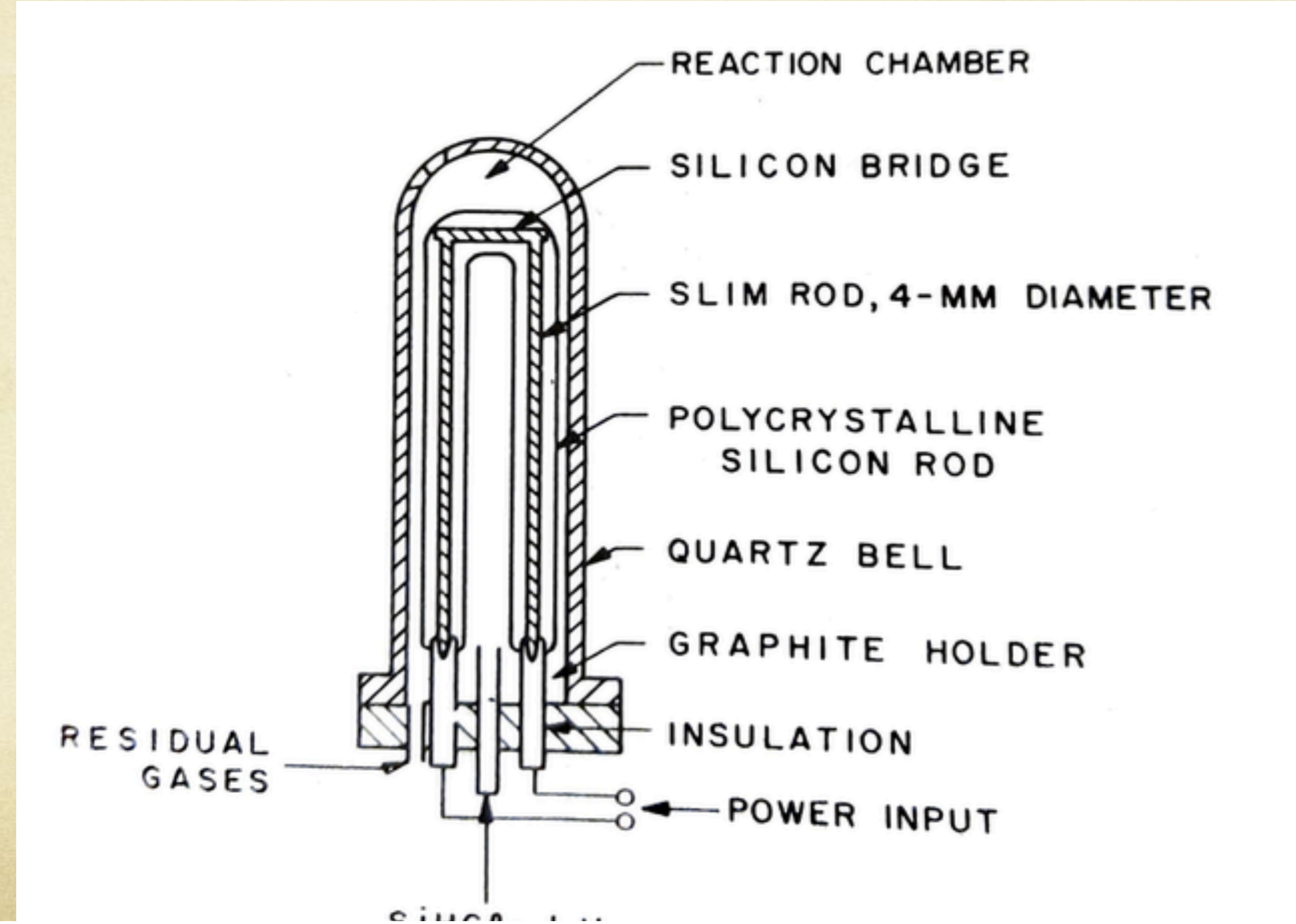
- SiO_2 is mixed with coke and heated.
- It first forms SiC, which further reacts with the remaining SiO_2 forming silicon.
- The temperature is maintained above the melting point of silicon so that the molten semiconductor is removed from the bottom.
- MGS is drawn off and solidify at a purity of 98%.
- The next step is Pulverize the silicon Mechanically and react with HCL to form trichlorosilane($SiHCL_3$)
- $Si(solid) + 3HCL(gas) \longrightarrow SiHCL_3(gas) + H_2(gas) + heat$
- The reaction takes place in a fluidized bed at 300^0c
- At this point Purification process occurs.

- Trichlorosilane is a liquid at room temperature(boiling point is 32^0C .
- Purification is done by fractional distillation
- EGS is prepared from purified $SiHCL_3$ in a chemical vapour deposition process.
- The chemical reaction is a hydrogen reduction of trichlorosilane

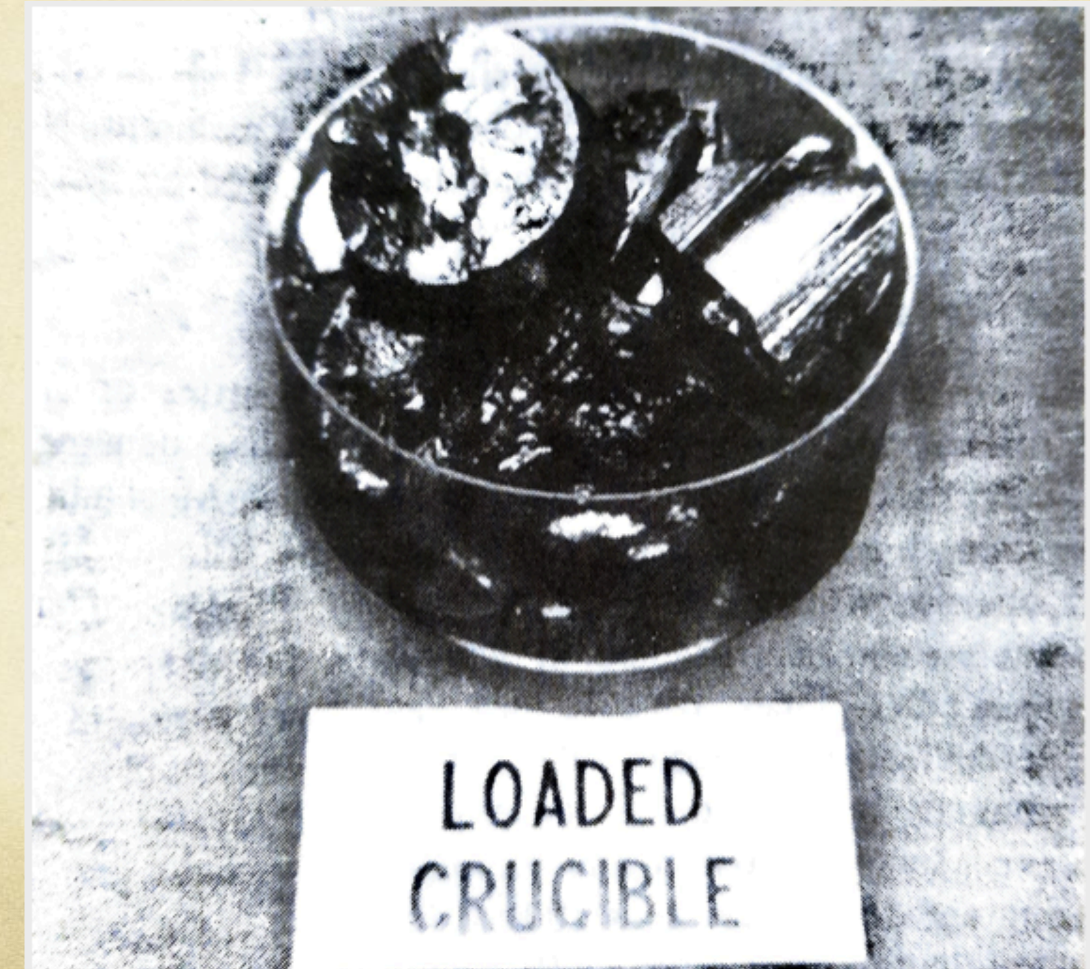
$$2\ SiHCL_3(gas) + 2H_2(gas) \longrightarrow 2Si(Solid) + 6HCL(gas)$$

This reaction is conducted int the type of system as shown in following figure

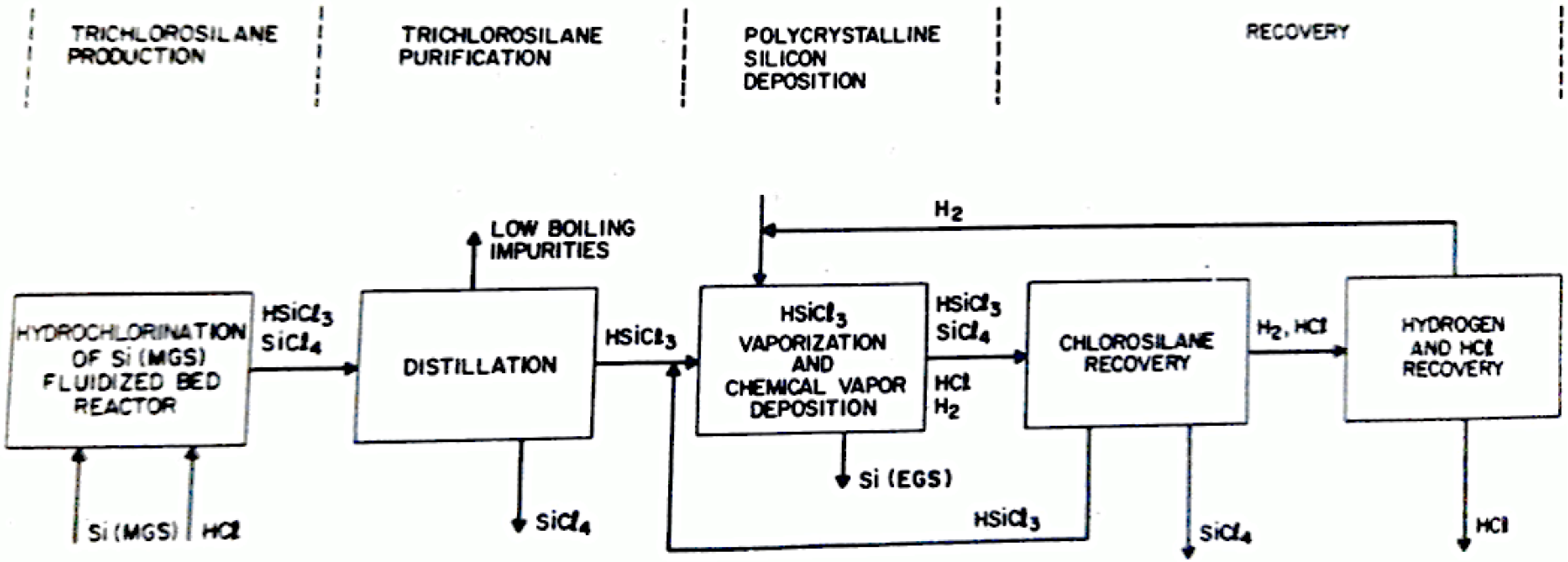
CVD Reactor used for EGS production

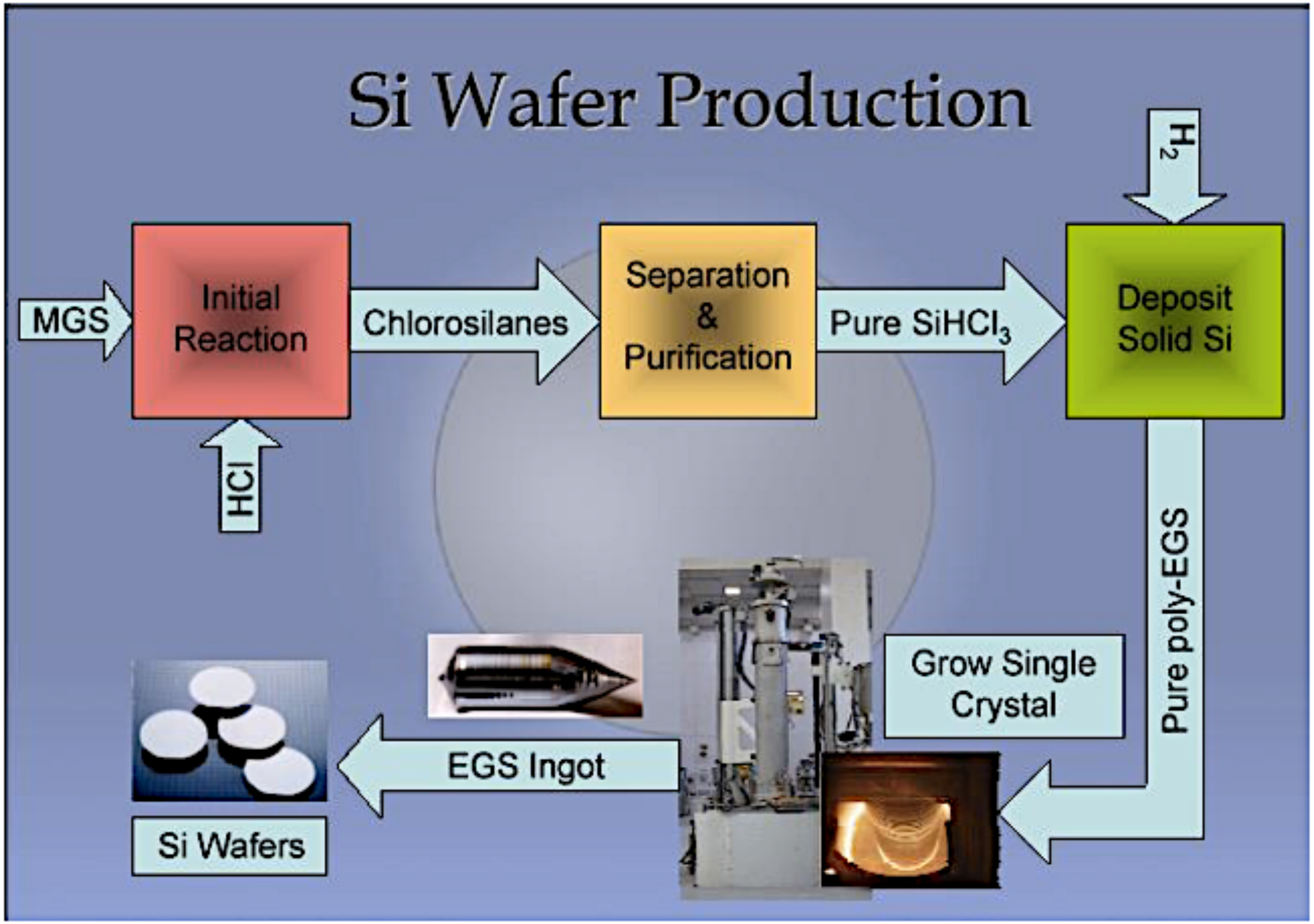


EGS in chunk form loaded in silica crucible



Production of EGS from hydrogen reduction of trichlorosilane



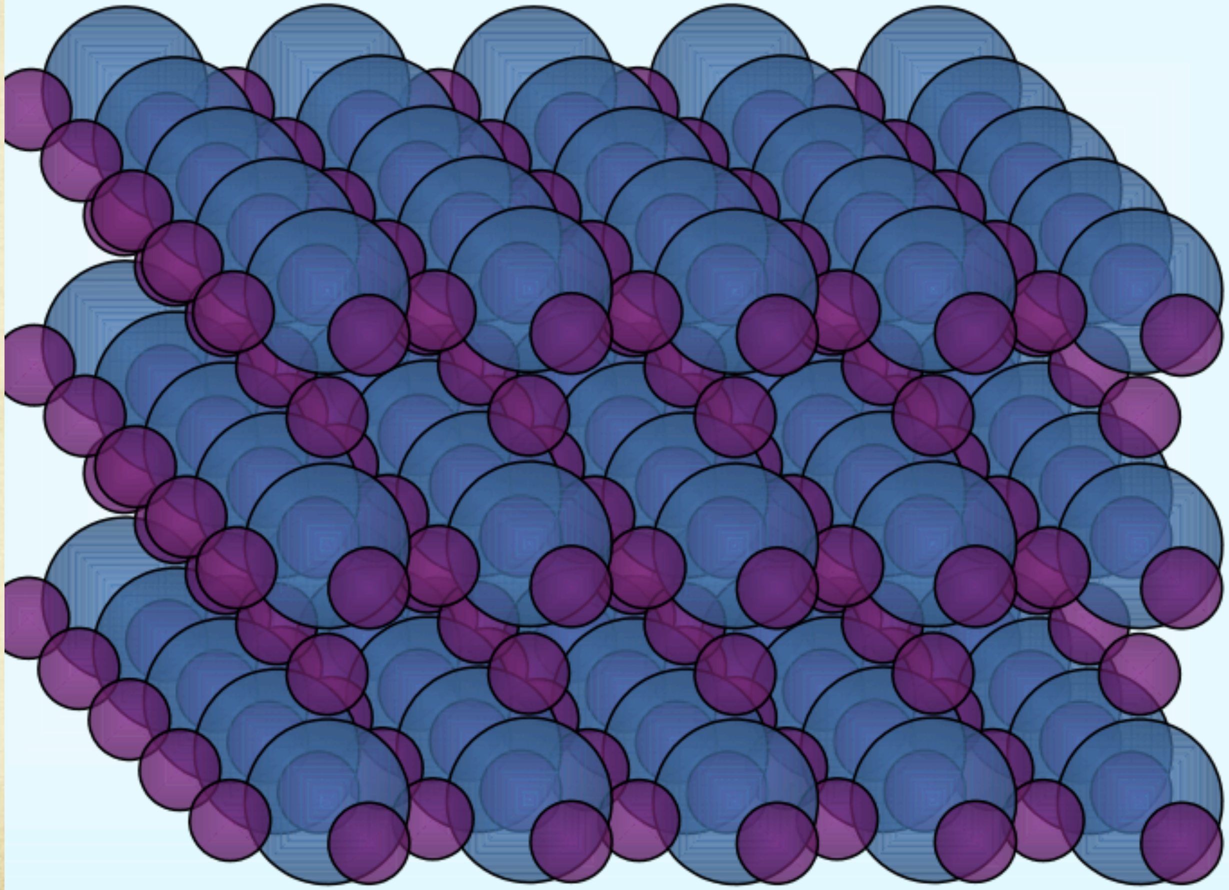


Si Wafer Production
MGS
Initial Reaction
HCl
Chlorosilanes
Separation & Purification
Pure $SiHCl_3$
H_2
Deposit Solid Si
Pure poly-EGS
Grow Single Crystal
EGS Ingot
Si Wafers

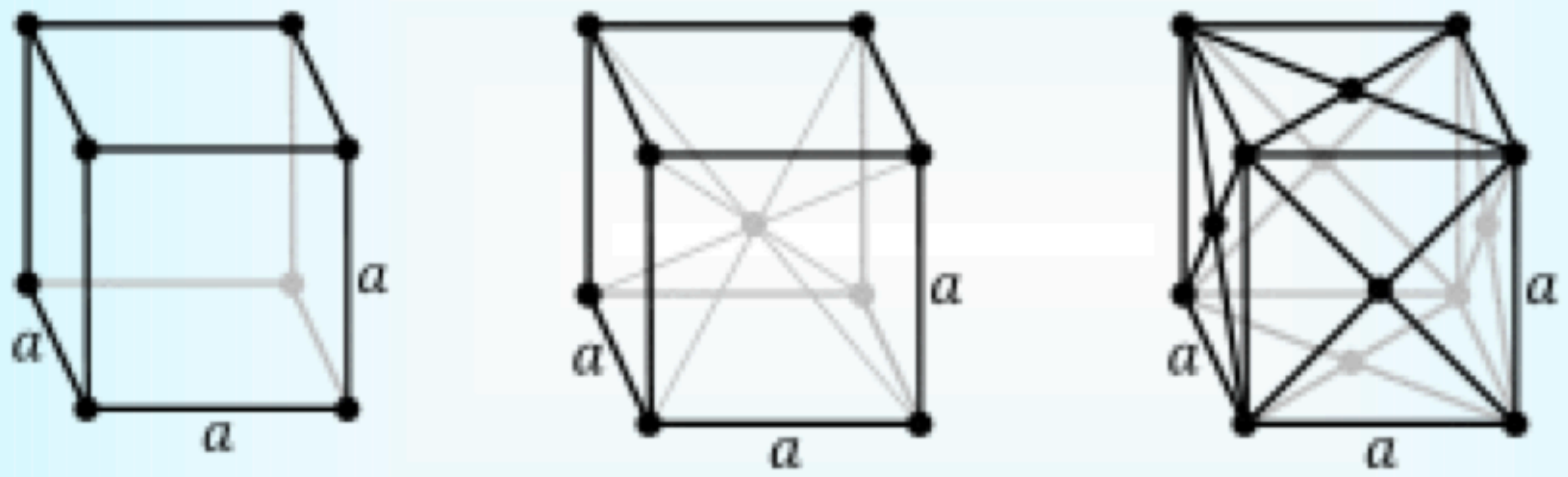
CRYSTAL STRUCTURE

- Material properties of silicon wafers depend upon its orientation
- The {111} planes have the highest density of atoms on the surface, so crystal grows more easily on these planes.
- Mechanical properties such as tensile strength are highest for <111> direction.
- Processing characteristic such as oxidation are orientation dependent.
- {111} planes oxidized faster than {100} planes. Because they have more atoms per unit surface area available for oxidation process to occur.

Atomic Order of a Crystal Structure

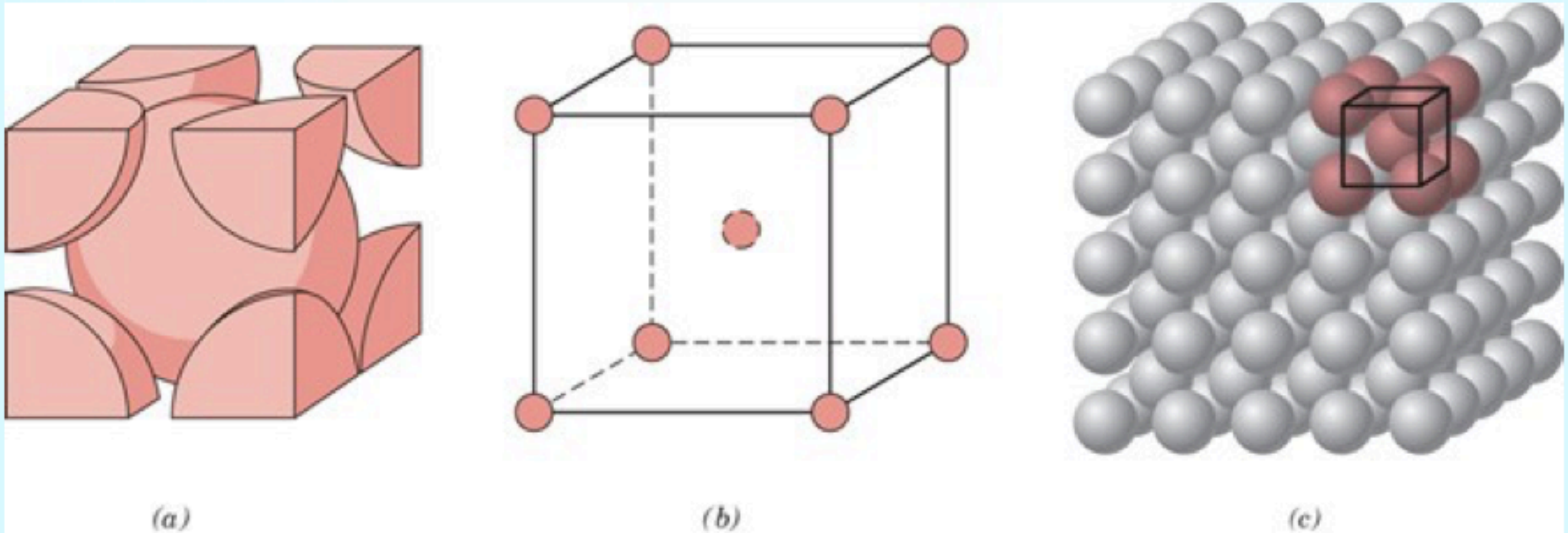


Simple Cubic lattices

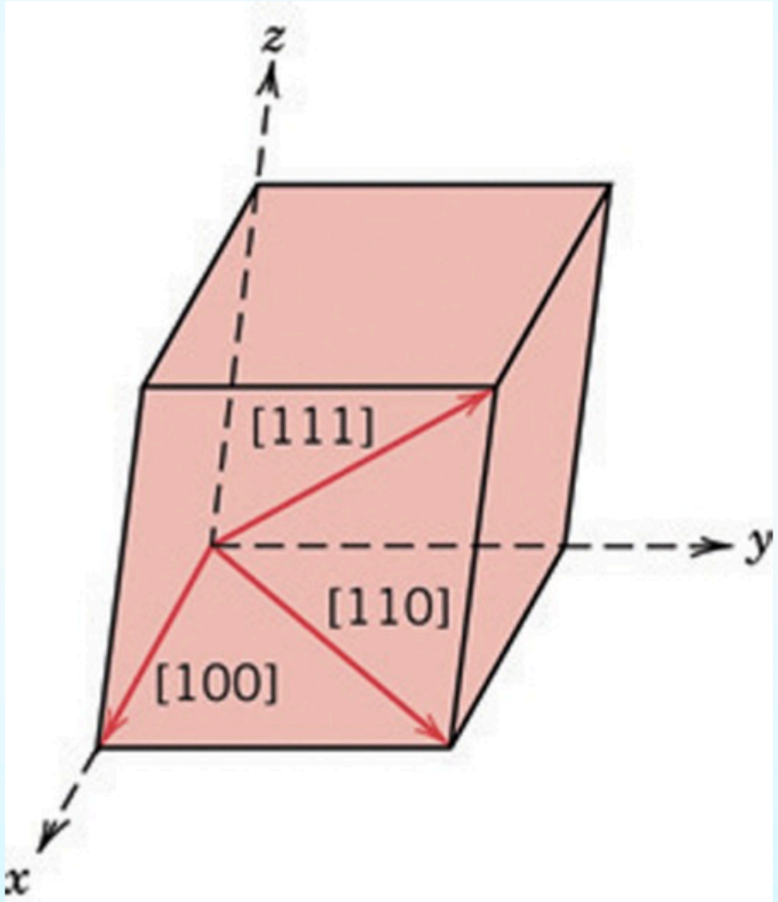


Simple **Body-Centered** **Face-centered**

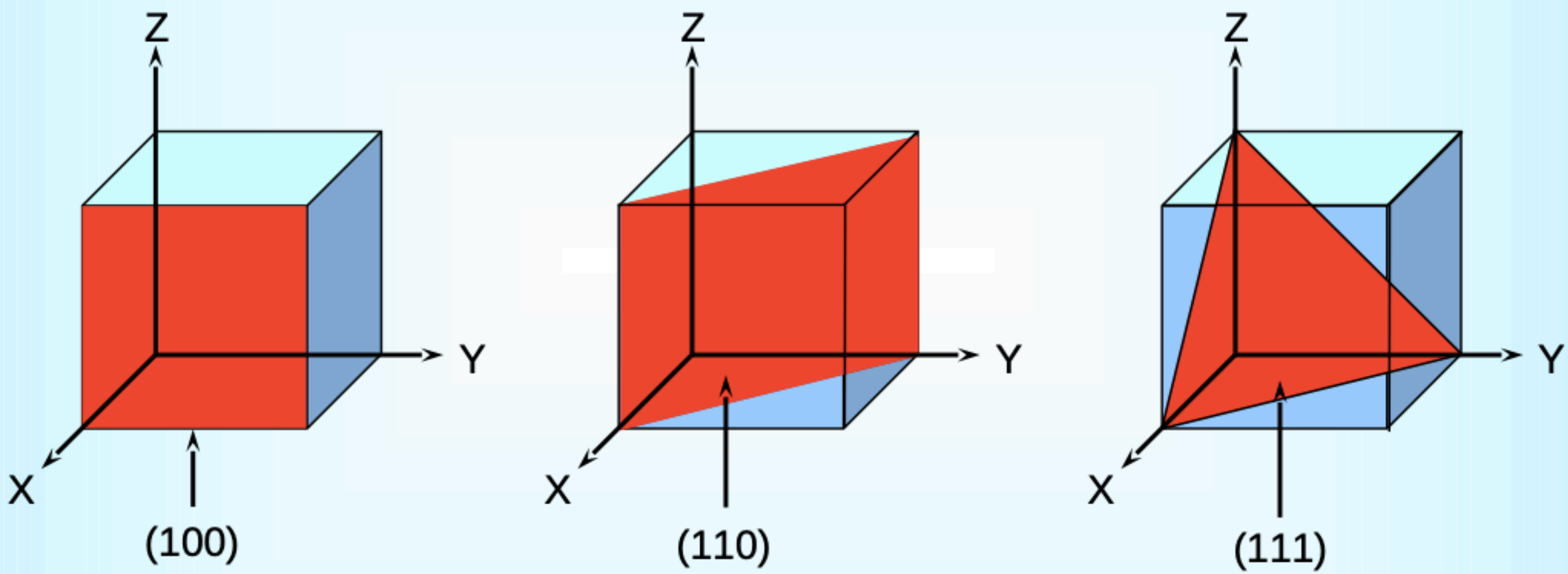
Body-Centered Cubic (BCC)



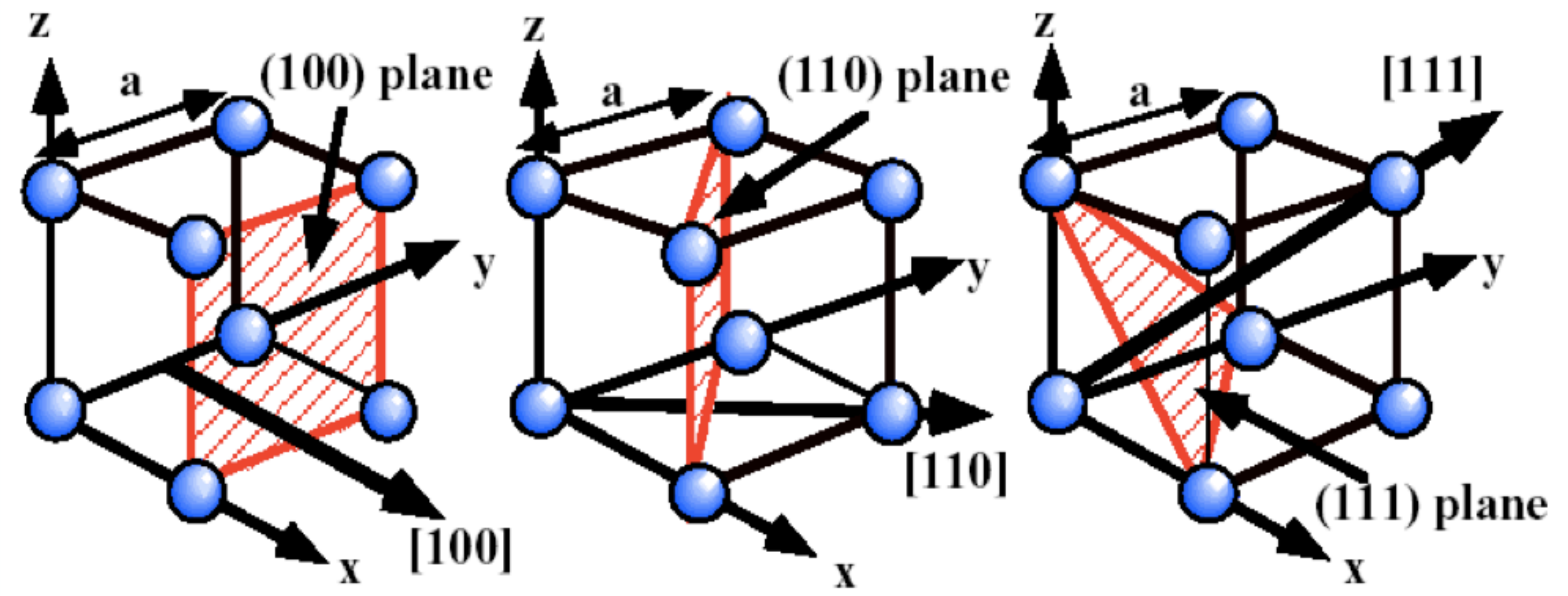
Specifying Directions in Crystals



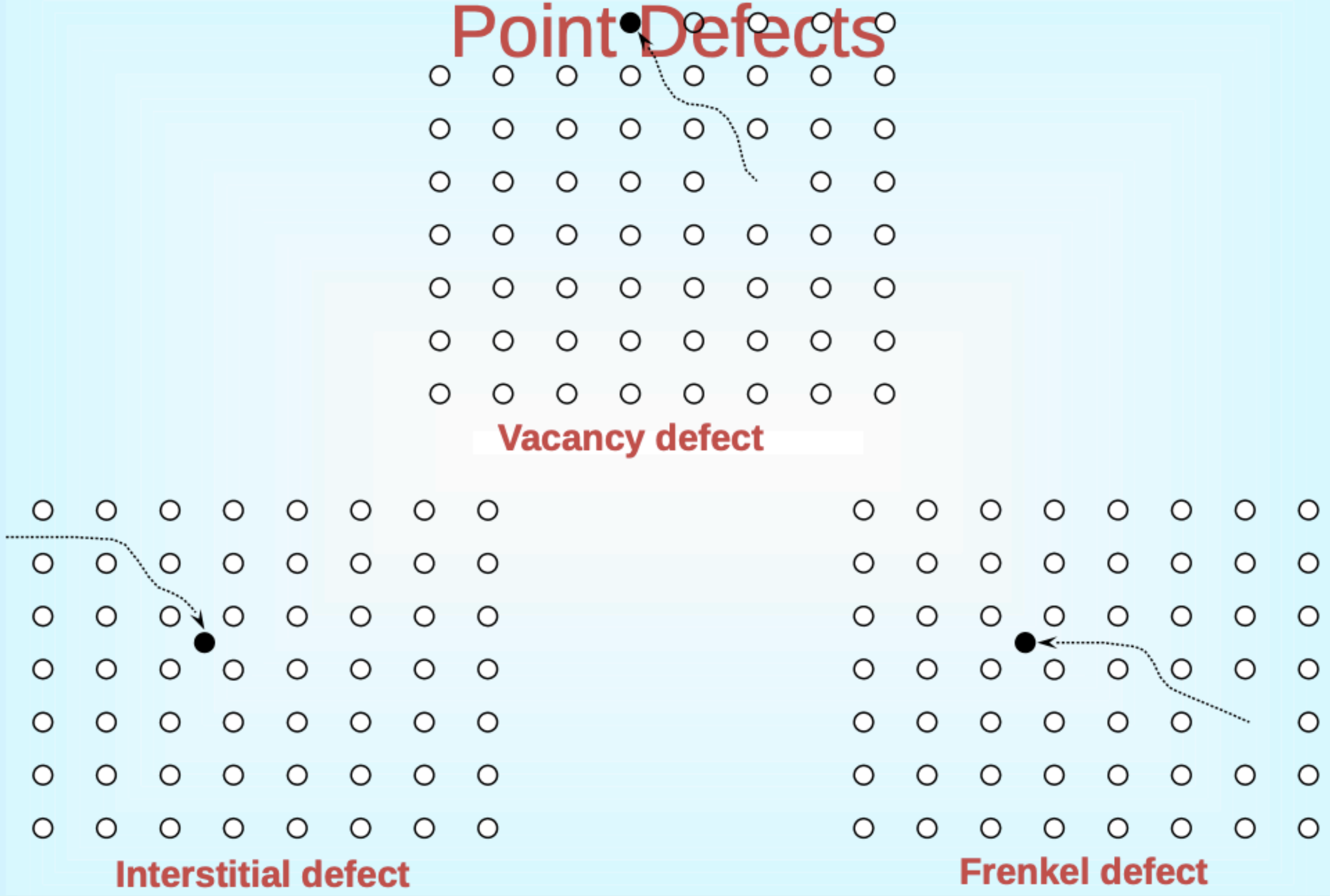
Miller Indices of Crystal Planes

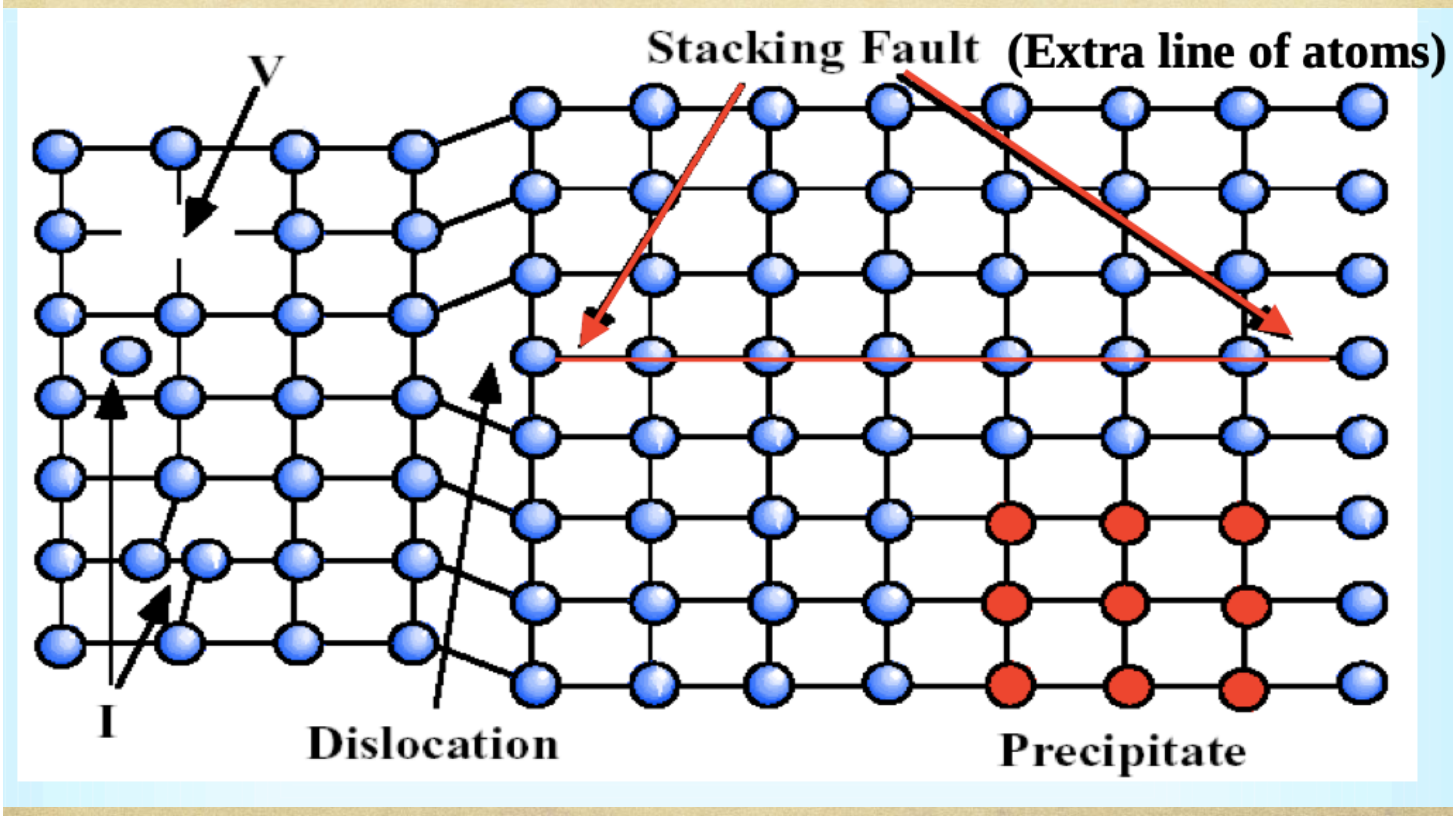


Silicon Crystal Structure

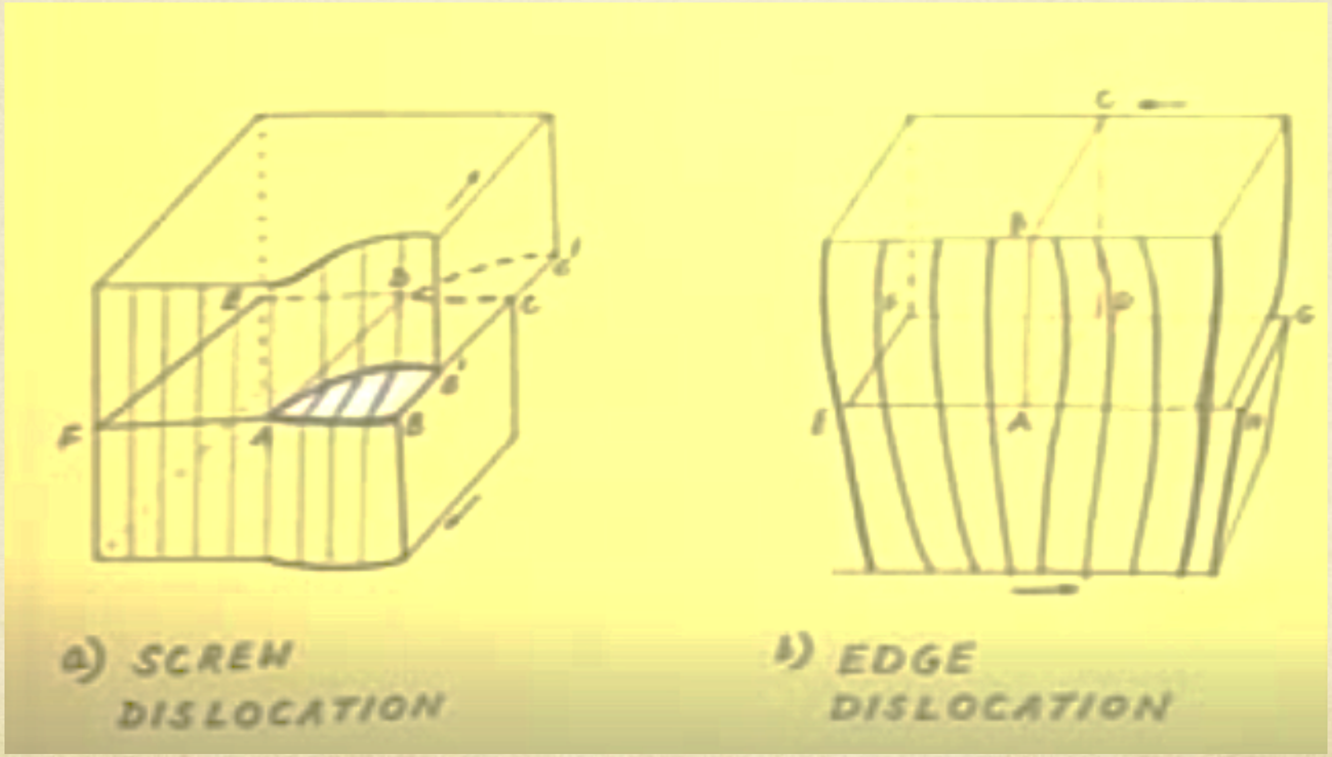


Point Defects




Stacking Fault
(Extra line of atoms)
V
I
Dislocation
Precipitate

Dislocations



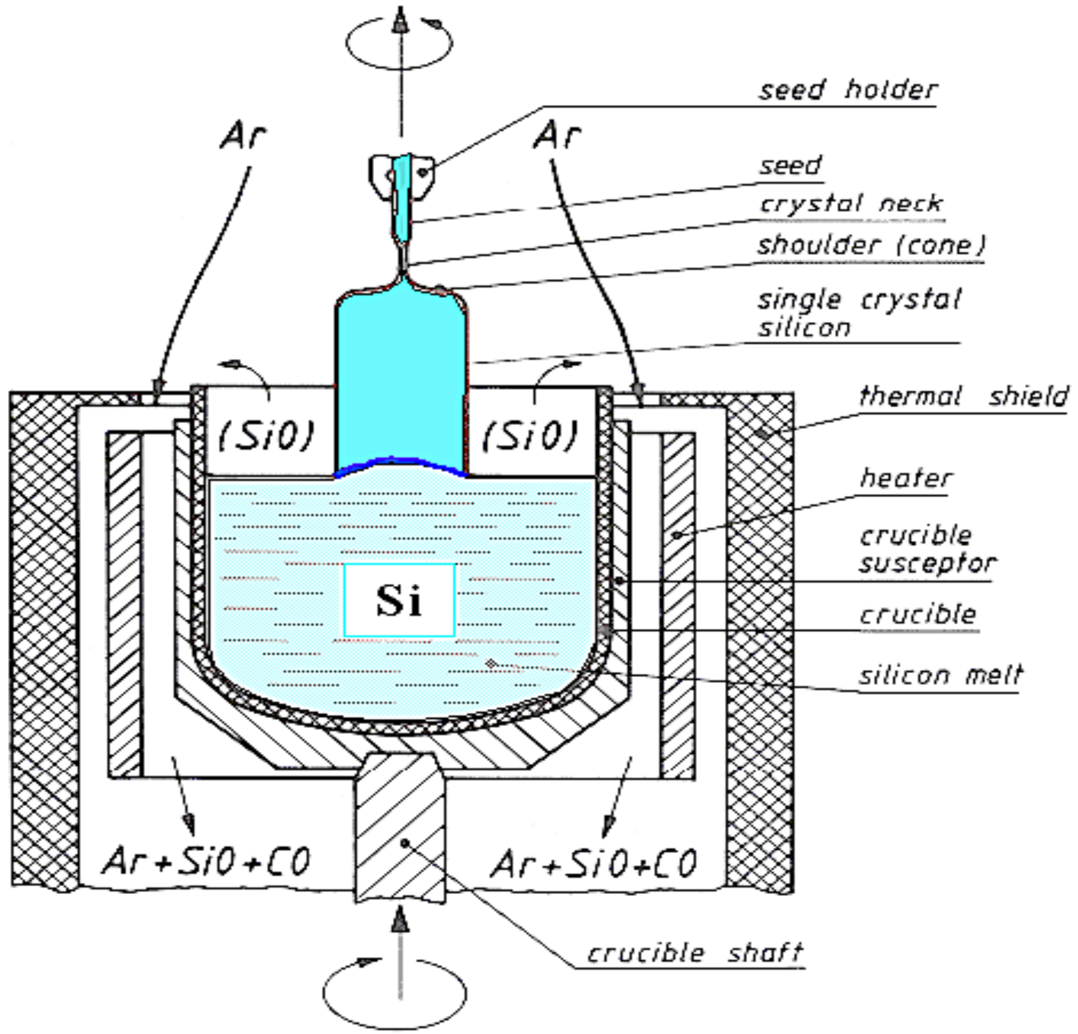
AREA and Volume Defects

- **Area Defect**: i) Twin: Twining is a change in crystal orientation. It means two parts of crystal are in intimate contact but they have some orientation with respect to each other.

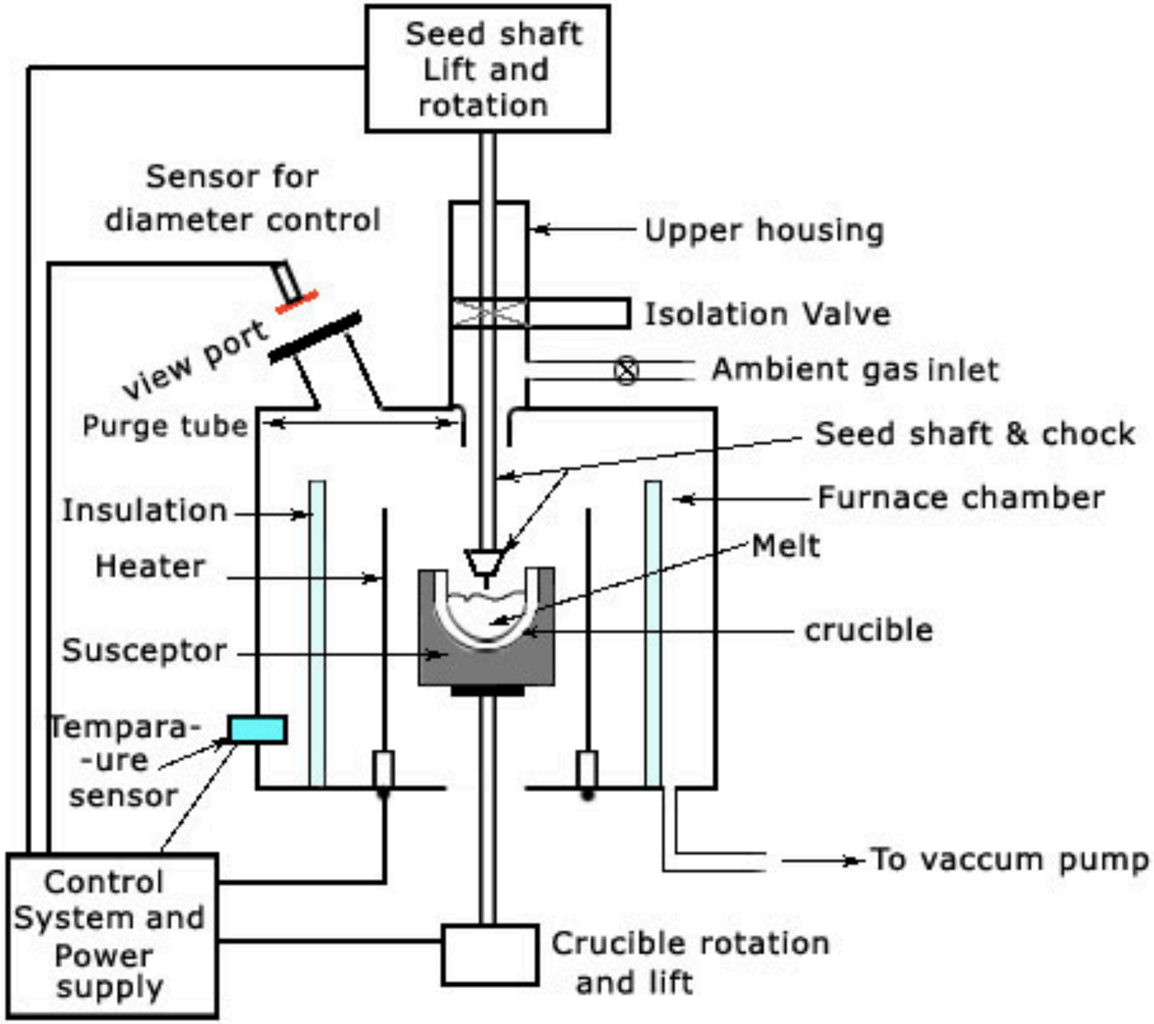
  ii) Grain Boundary: Due to some process problem various crystalline orientation may present in the same substrate(Pollycrystalline) and in between these crystalline structures which are called the grains in a poly crystalline material, resulting in a defective boundary region separating one crystalline region from another this is called grain boundary.

Volume Defect: Precipitates act as sites for dislocations

Beginning of crystal growth



A practical silicon crystal growing apparatus



Czochralski Method …

- This process uses Czochralski Crystal Grower.
- Poly-EGS is melted in a quartz-lined crucible at about 1412˚C .
- Seed crystal is introduced into the molten poly-EGS to begin crystallization.
- Seed pulled slowly, allowing the crystal to grow on to it. Simultaneously, the crystal is rotated slowly to give slight stirring of the melt to prevent inhomogeneous solidification.
- Then Ingot is cooled at a very slower rate.

- Liquid-Solid monocomponent System –CZ
- Four subsystem of CZ process

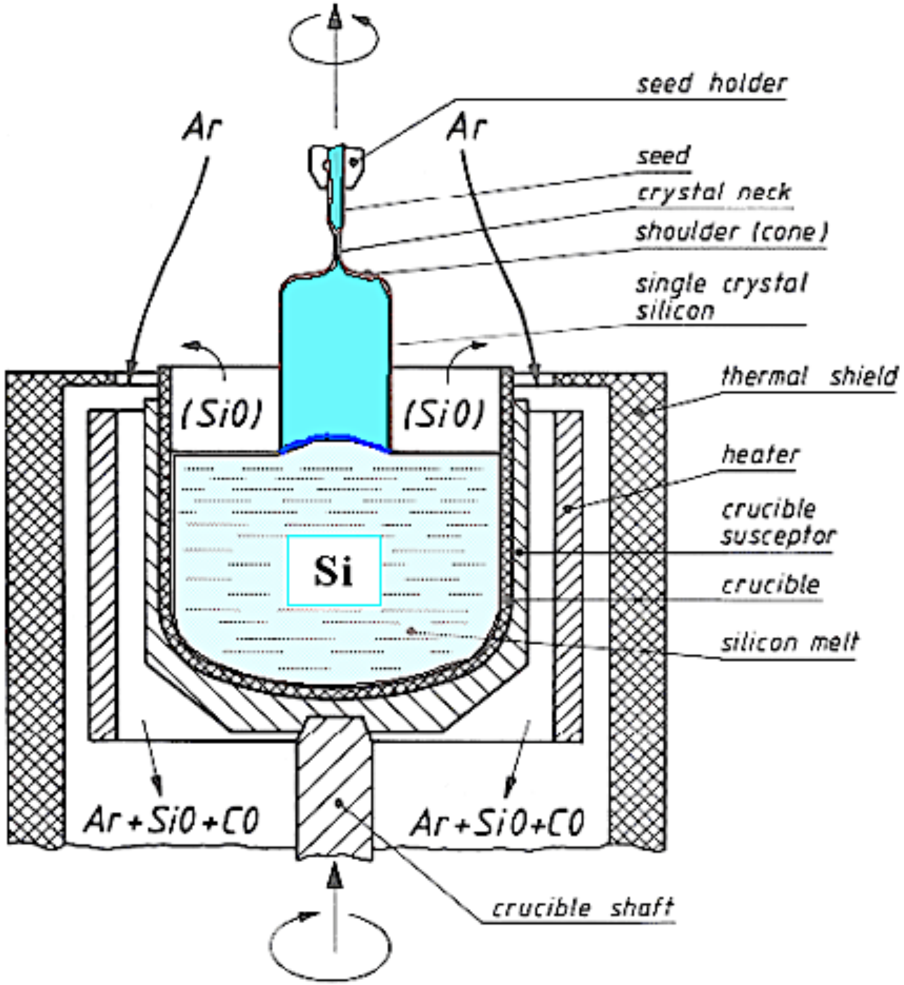
    i) Furnace-

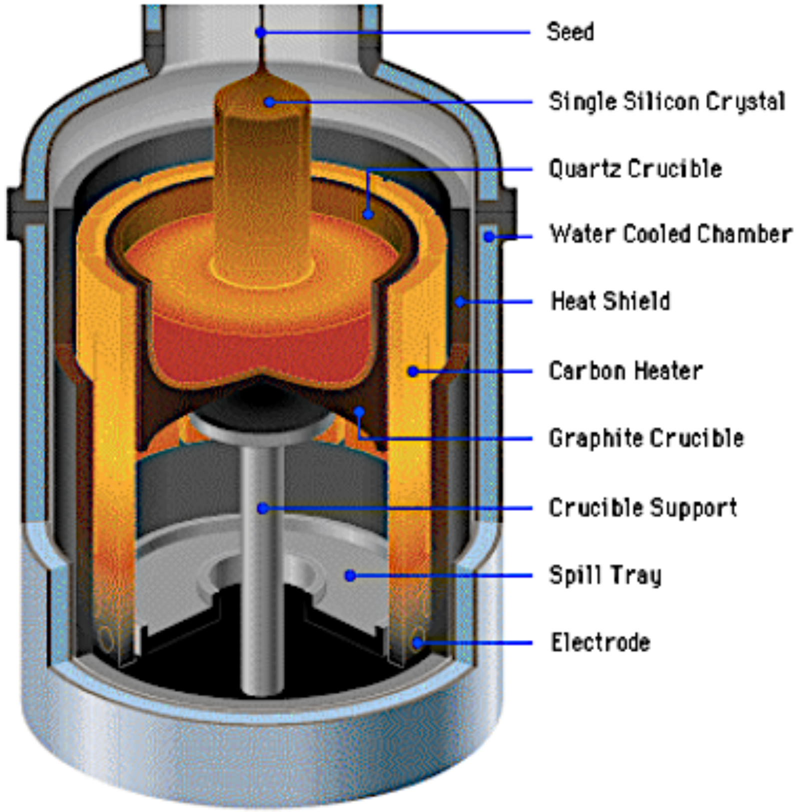
    ii)Crystal Pulling mechanism

    iii) Ambient control

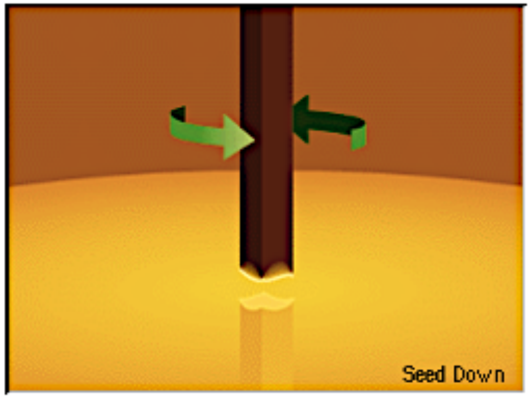
    iv) Control system

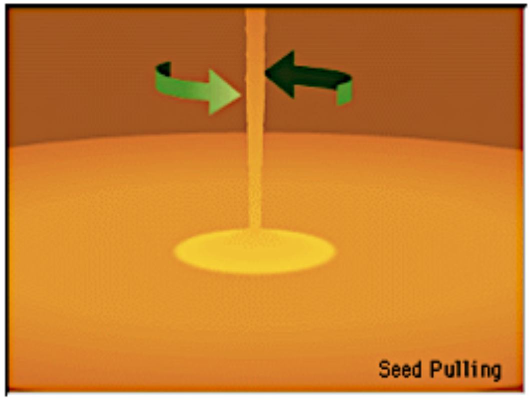
Czochralski Crystal Grower….

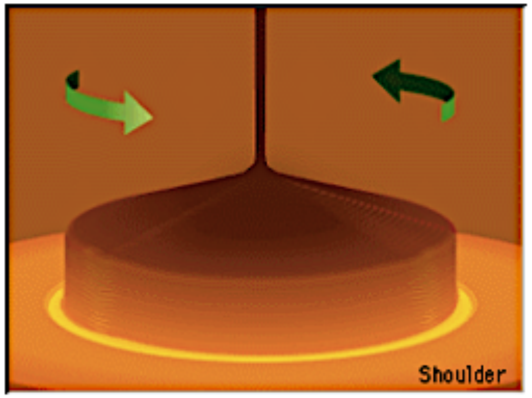


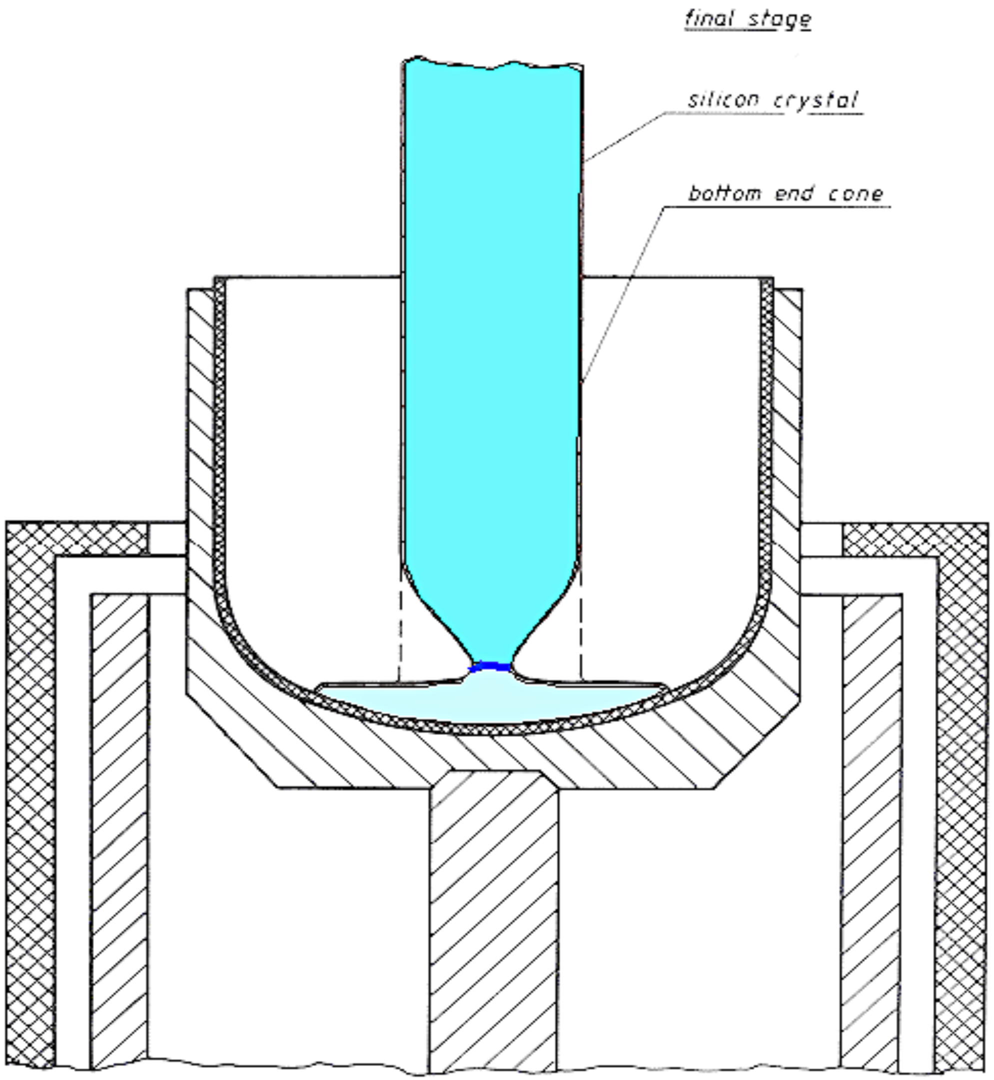


The Process…





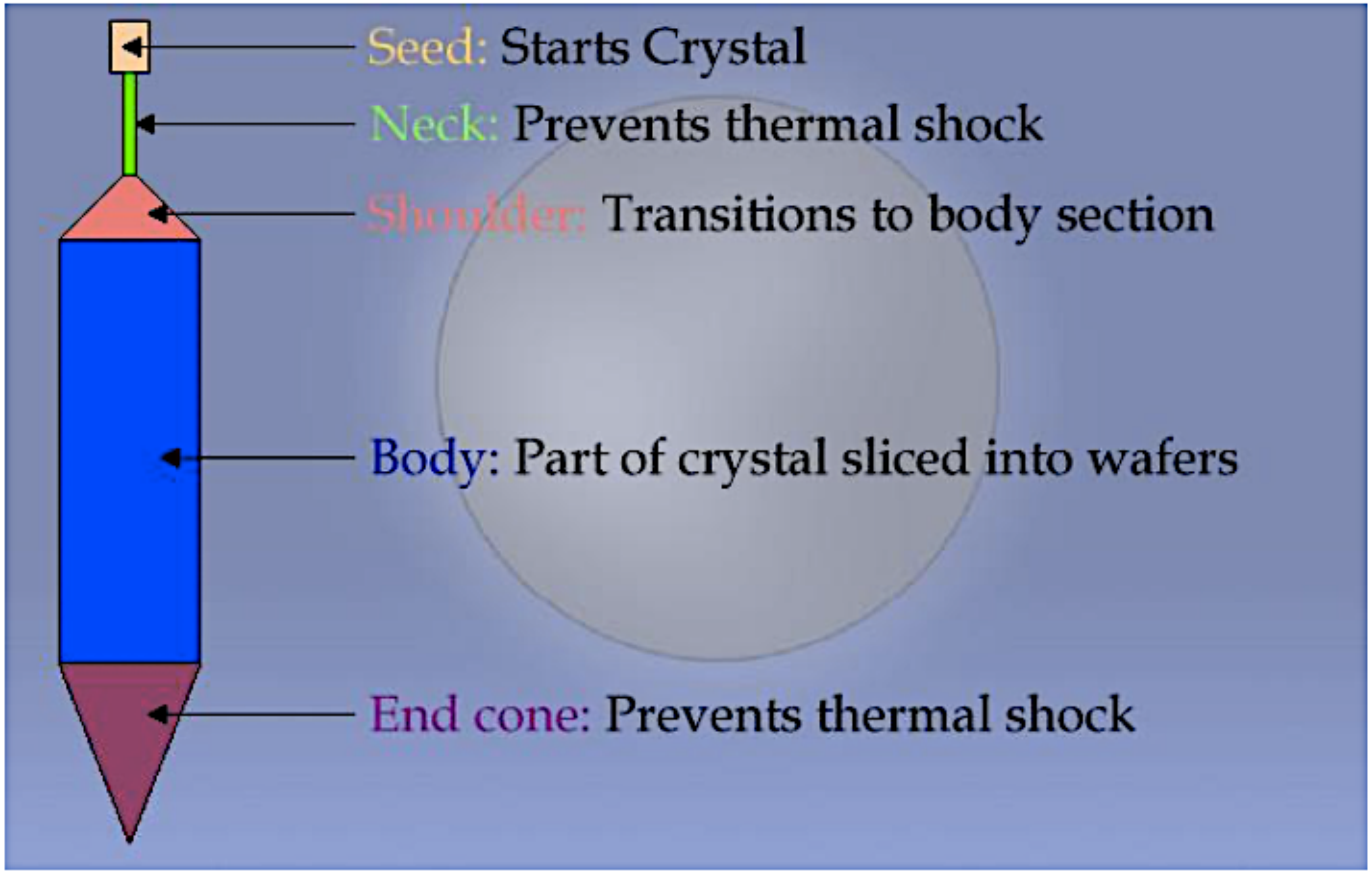



final stage
silicon crystal
bottom end cone

- Take care to keep impurities out - do it in a clean room - and use hyperpure silica for your crucible.
- Make sure that the inside of the machine is very clean too and that the gas flow
- the gas you introduce but also the SiO coming from the molten **Si** because parts of the crucible dissolve
- Dissolve the Si in the crucible and keep its temperature close to the melting point.

- Since you cannot avoid temperature gradients in the crucible, there will be some *convection* in the liquid **Si**. You may want to suppress this by big magnetic fields.
- Insert your *seed crystal*, adjust the temperature to "just right", and start withdrawing the seed crystal.
- For homogeneity, *rotate* the seed crystal and the crucible.
- First pull *rather fast* - the diameter of the growing crystal will decrease to a few mm.
- Now decrease the growth rate - the crystal diameter will increase

The Finished Crystal Parts…



Single Crystal Ingots…

- This Technique is widely used in Growing Si, Ge and some compound semiconductor.
- In pulling compounds like GaAs from the melt, vaporization of volatile elements (e.g. As) is prevented.
- In one method, known as *Liquid Encapsulated Czochralski **(LEC)*** growth, the same can be done by using B_2O_3 (Boron Trioxide) , which floats on the surface of the molten GaAs.