4. CMOS

AIM: To study the CMOS and plot the DC/transient curves using simulation

Tool used: Some study about CMOS and Cogenda Visual TCAD tool

Theory: CMOS uses complementary and symmetrical pairs of p-type and n-type of (MOSFETs) for logic functions. CMOS-based transistors only use one charge at a time, they run efficiently, using up very little power, the devide figure is given below

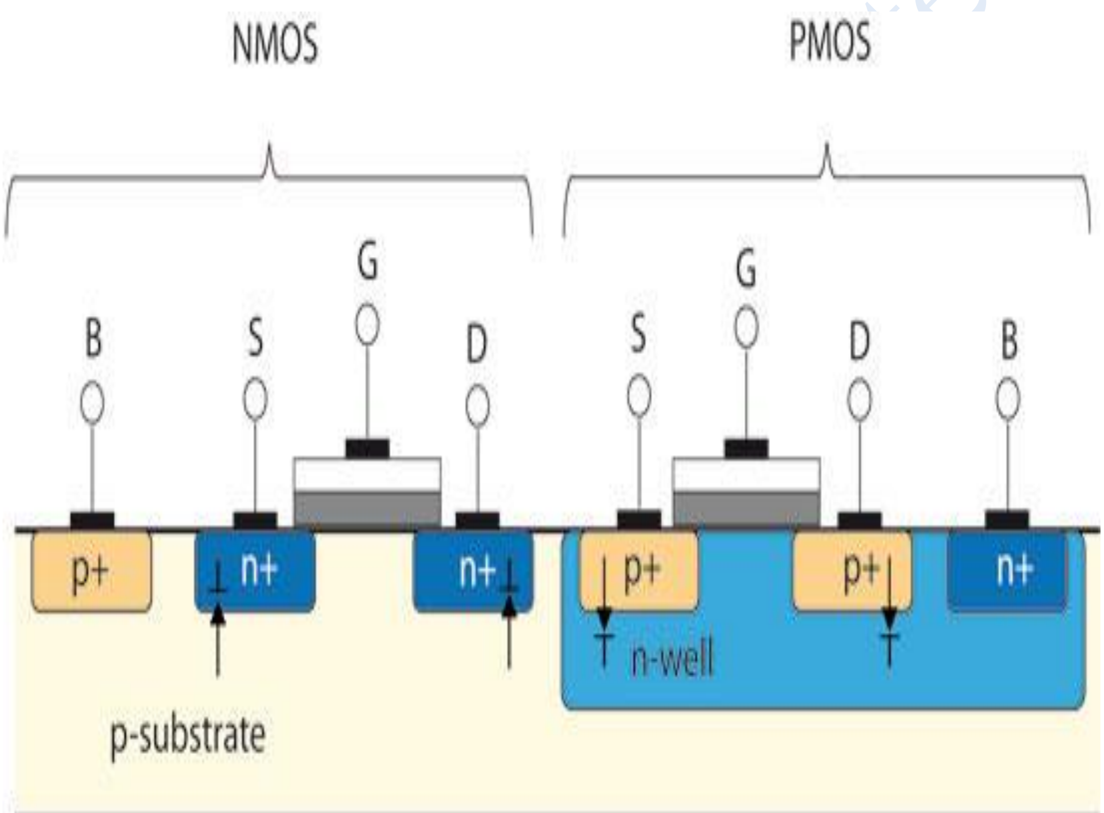


Fig 4(a) CMOS

<u>**OPERATIONS**</u>

<u>**For VTC**</u>

- when we apply the constant voltage at the **VDD**(from the interconnection of **Source** and **Substrate** of **PMOS**), **Ground** (from the interconnection of **Source** and **Substrate** of **NMOS**),**OUTPUT** (from the interconnection of both the **Drains** of **NMOS** and **PMOS**), & **INPUT** (from the interconnection of both the **Gates** of **NMOS** and **PMOS**) by giving a Constant or a DC voltage as a source of Supply Voltage
- Below in figure are the **CMOS** standard **DC analysis** or **VTC[Voltage transfer characteristics]** characteristics

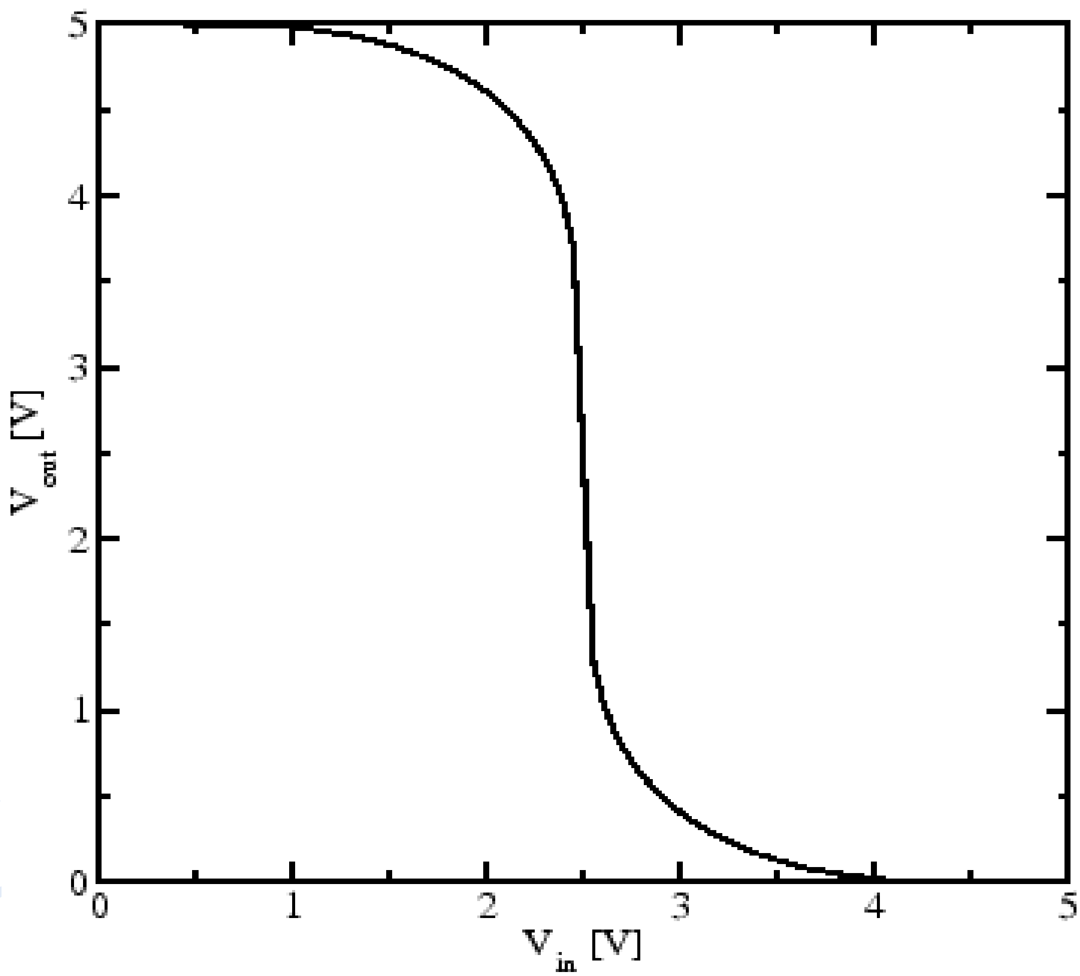


Fig 4(b) DC analysis or Voltage transfer characteristics [VTC]

For Transient Analysis

- when we apply the constant voltage at the **VDD**(from the interconnection of **Source** and **Substrate** of **PMOS**), **Ground** (from the interconnection of **Source** and **Substrate** of **NMOS**),**OUTPUT** (from the interconnection of both the **Drains** of **NMOS** and **PMOS**), & **INPUT** (from the interconnection of both the **Gates** of **NMOS** and **PMOS**) by giving a varying power source or a Pulsated voltage as a source of Supply Voltage
- Below in figure are the **CMOS** standard **Transient** characteristics

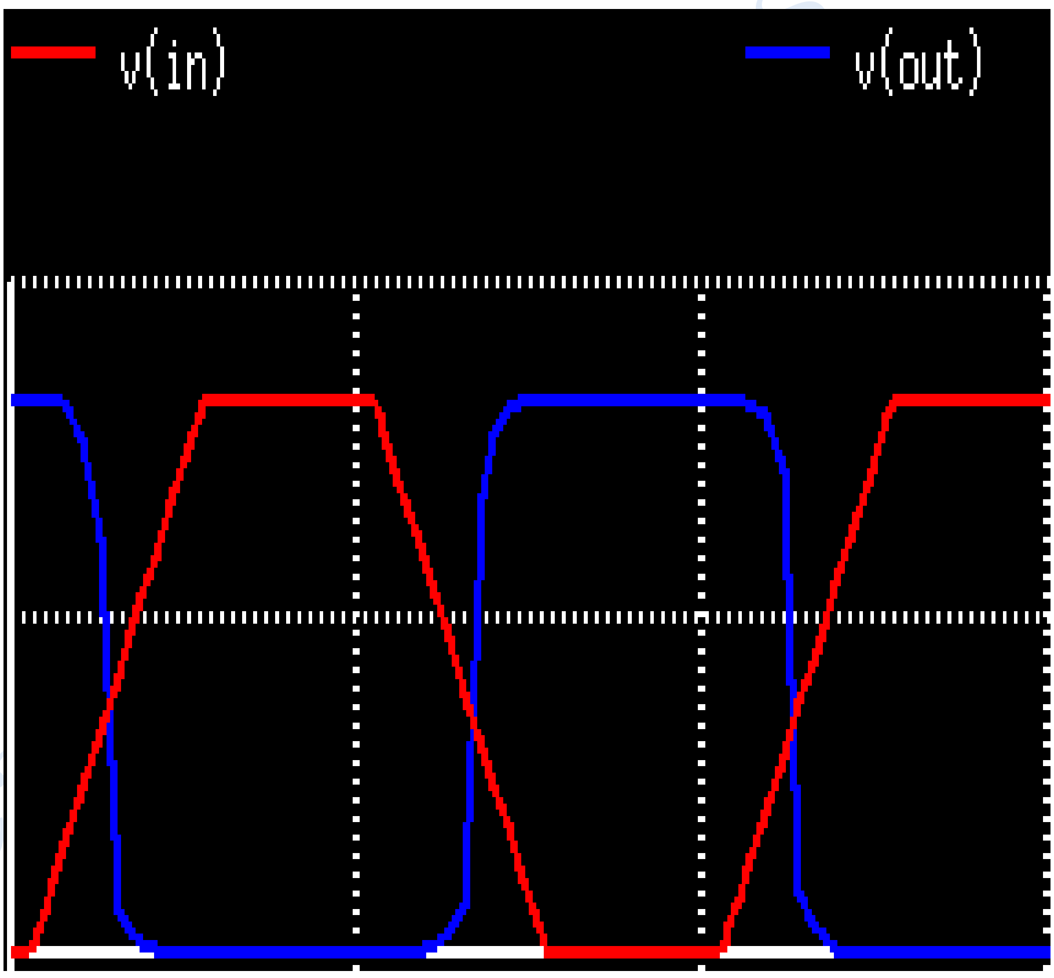
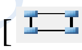


Fig 4(c) Transient Output

Procedure:

1. Open the Visual TCAD tool by clicking on the icon in start menu for windows user and for Linux(ubuntu or rhel) open the terminal [ctrl+alt+t]
2. Go to the new file and choose the Device Drawing as an option
3. A window with black background will open up with default grid spacing width of 0.01um
4. We are preparing a P-MOSFET alongside N-MOSFET of both having same dimensions as (L=0.5um x H=0.6um) with the **Source(s)** region and the **Drain(s)** region **(L=0.1um x H=0.03um)** and **Substrate(s) (L=0.6um x H=0.5um)** along with **Gate(s) (L=0.2um x H=0.03um)** and oxide **(L=0.2um x H=0.01um)**.
5. With the help of the shapes given on the left top use rectangular []shape to design the device
6. The actual shape is designed below using the rectangular shape

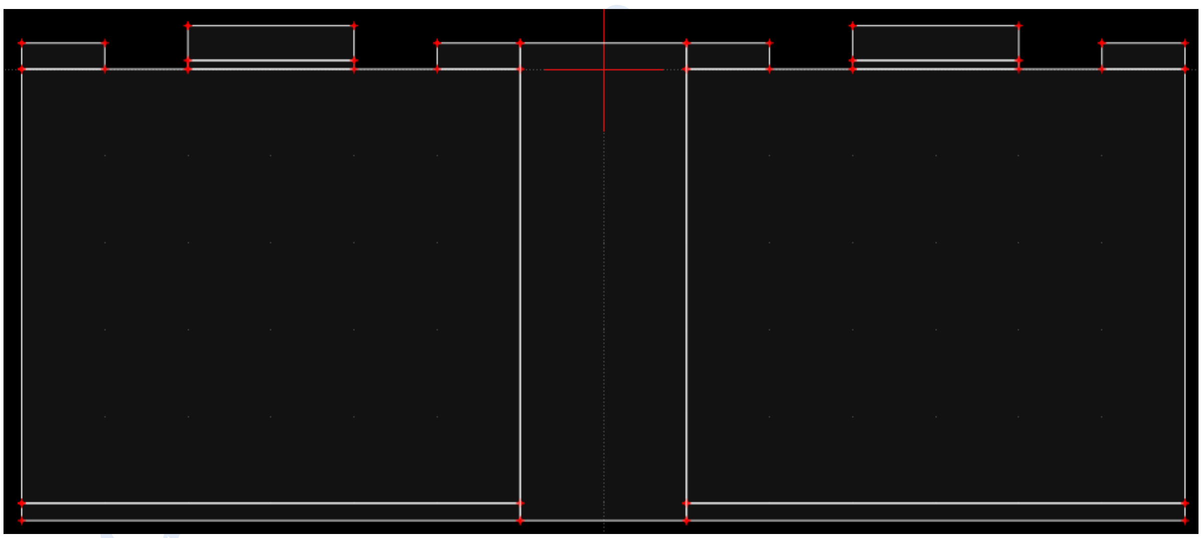


Fig 4(d) Structure of a MOSFET

7. Add the region label from the option in the left palette in Device Drawing **[**  **]** with named as **P.BODY** for **PMOS** and **N.BODY** for **NMOS (0.5um x 0.6um)** of the silicon material with the mesh size assumed as 1/10th of the block size e.g. as it is of 5um block length so max. meshing size will be 0.05um
8. Add the region label of the another three blocks that are **P.Source & N.Source (L=0.03um x H=0.1um)**, **P.Drain & N.Drain (L=0.1um x H=0.03um)**, **P.Substrate** & **N.Substrate (0.02um x 0.6um)** with the Aluminum (Al) region and keep the max mesh

size same as given by default as we don't require to calculate on the metal-semiconductor junctions. Another two regions are **P.Gate** & **N.Gate** with material (P Poly Silicon) & (N Poly Silicon) respectively along with the **P.oxide** & **N.Oxide** regions below Gate of both region with material (silicon dioxide) having the mesh size of **0.05 &** it is isolated with the **Oxide** material in between **PMOS** and **NMOS** as a Spacer with by default mesh size .

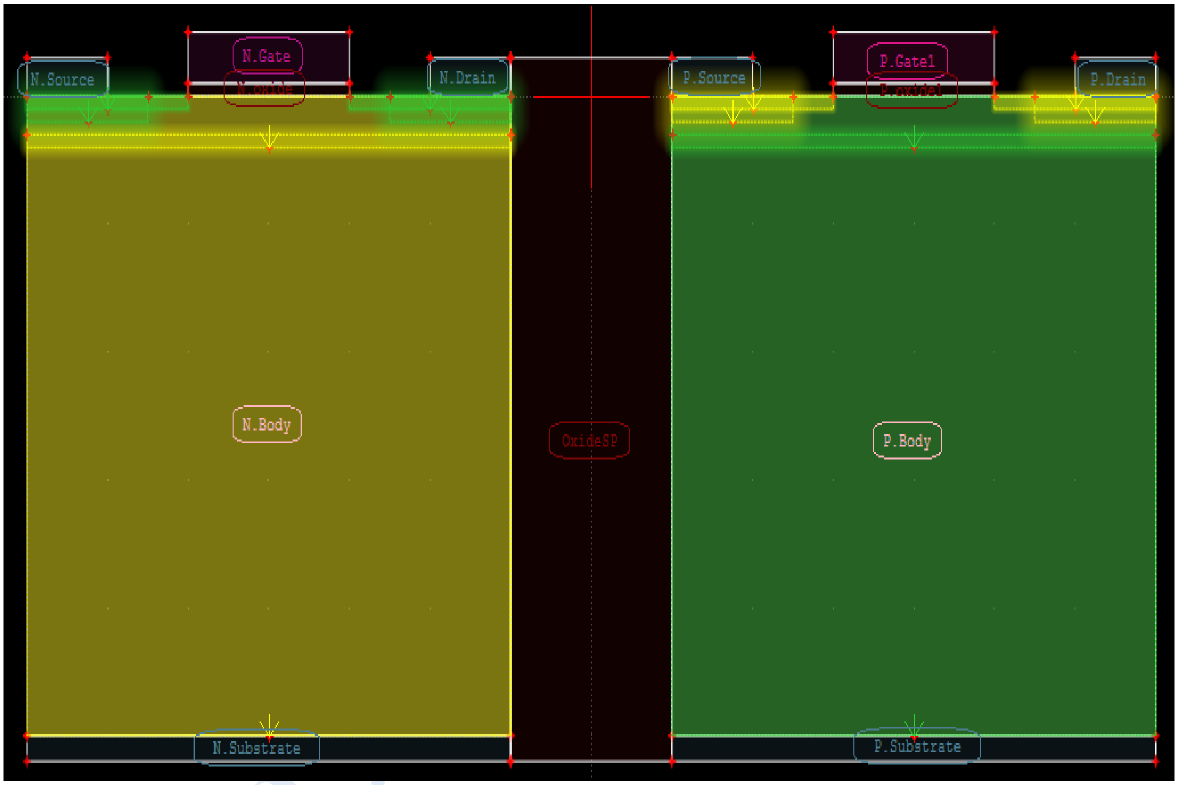


Fig 4(e) Structure of a CMOS with all regions with materials

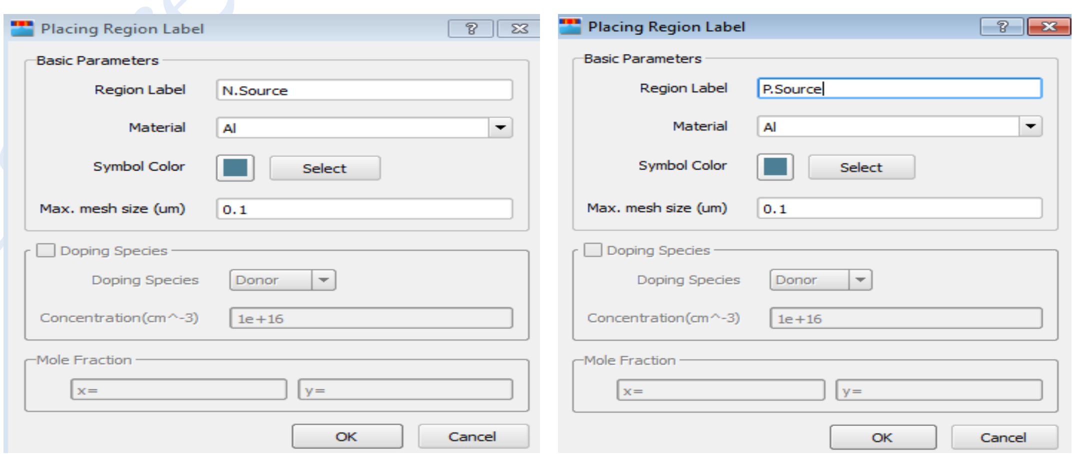


Fig 4(f) Source regions with material meshing and details

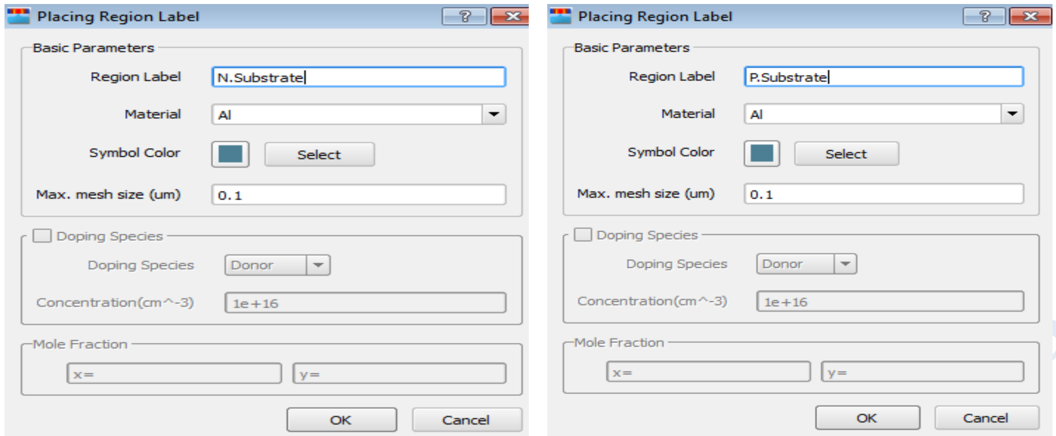


Fig 4(g) Substrate region with material meshing and details

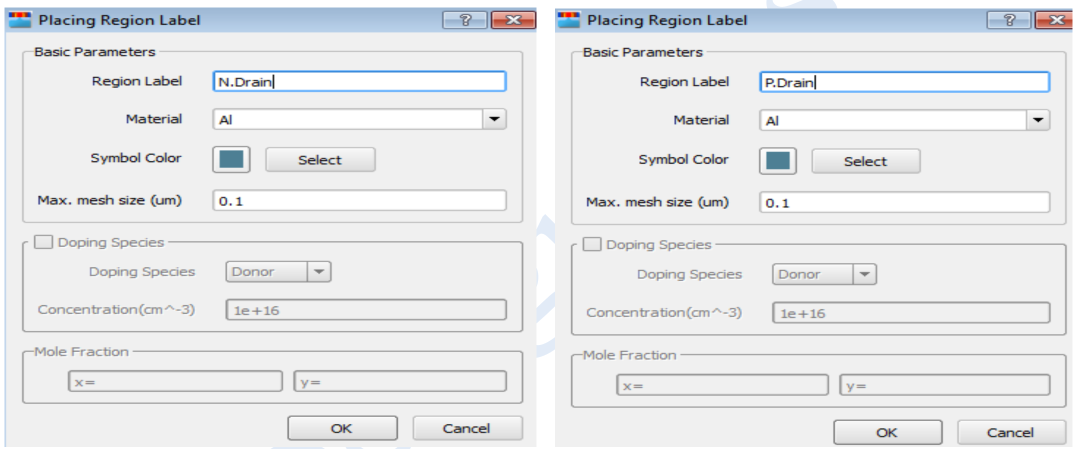


Fig 4(h) Drain region with material meshing and details

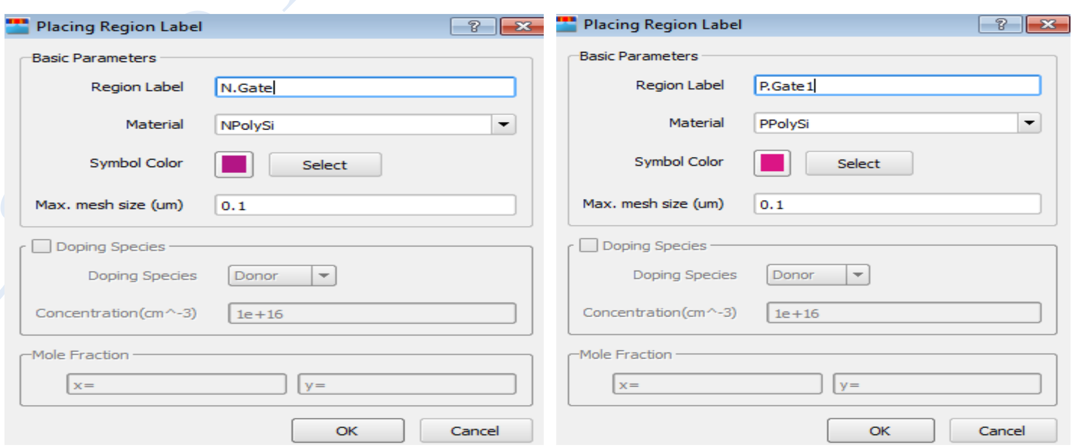


Fig 4(i) Gate region with material meshing and details

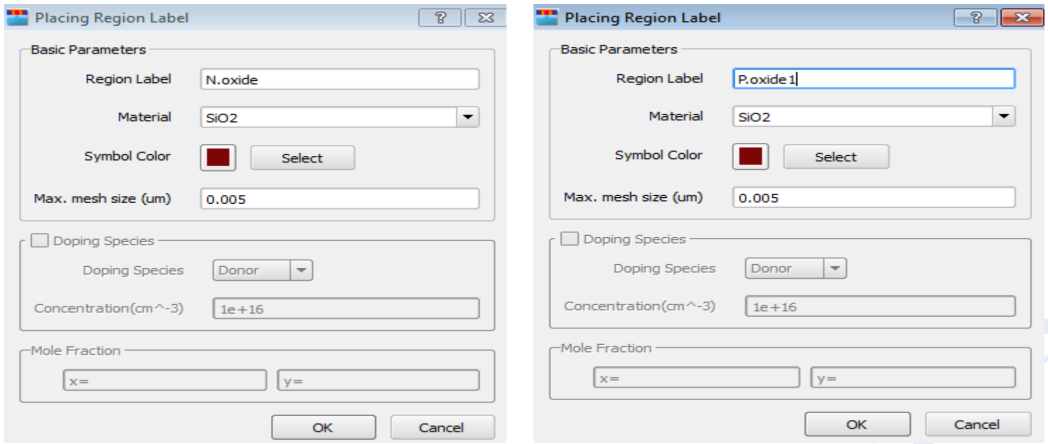


Fig 4(j) Oxide region with material meshing and details

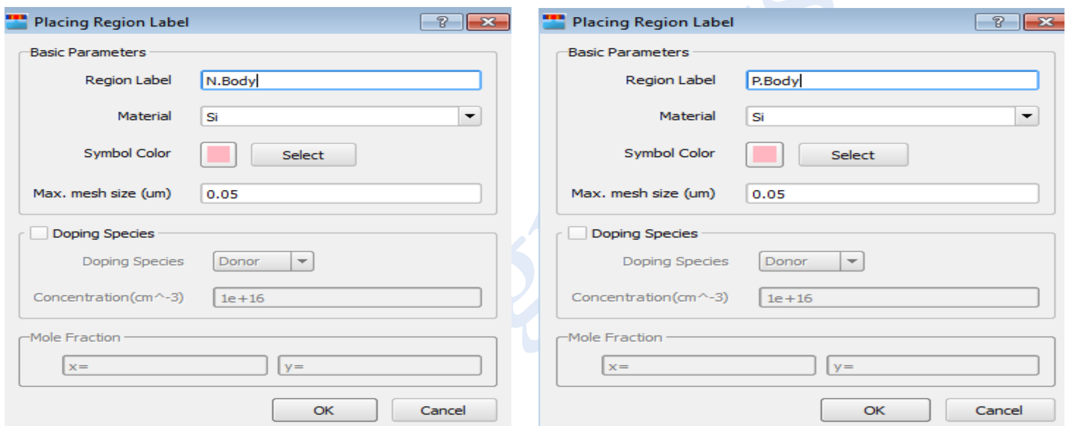


Fig 4(k) Body with material and meshing Details

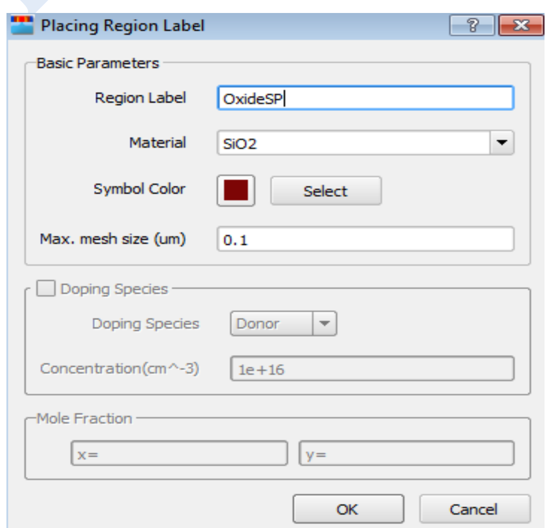
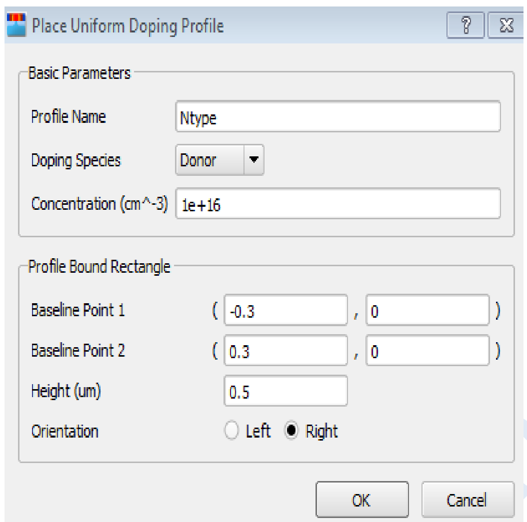
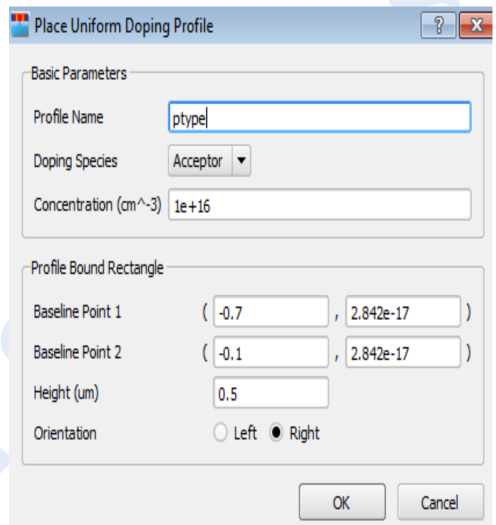


Fig 4(l) Oxide Spacer with material and meshing Details

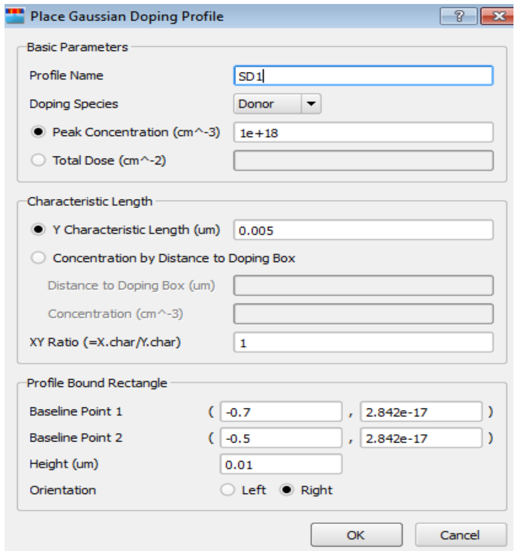
9. Now with the option of Add Doping Profile we will make the two regions **NMOS** & two regions for **PMOS**

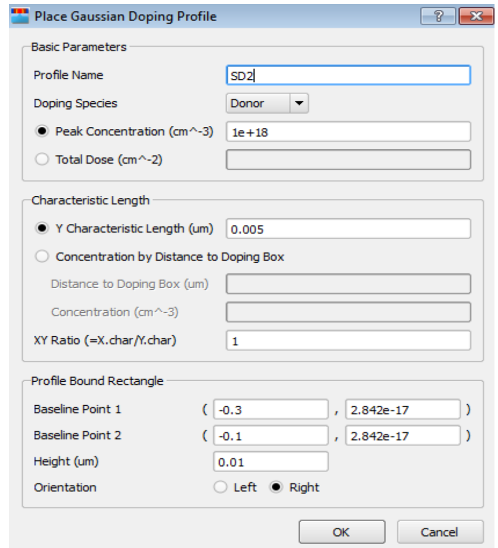
- First is **uniform doping profile** of **N type** /**Donor** in **PMOS** & **P type**/**Acceptor** in **NMOS** with the doping concentration of **(1e+16)/cm^3** across the whole region from top to bottom uniformly or we can say **(0.5um x 0.6um)** above the **Body** region of both **PMOS** & **NMOS** from top to bottom.

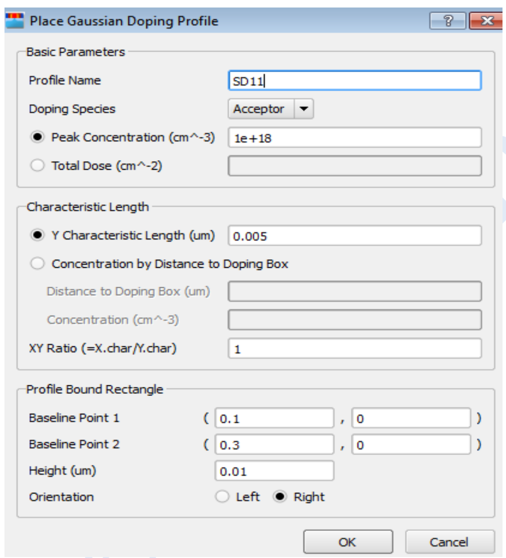


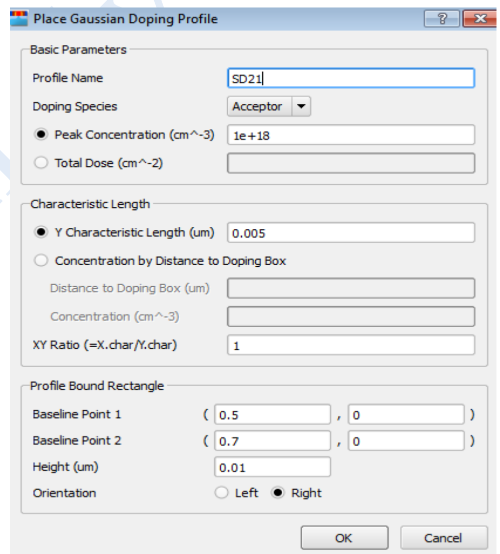


- Second is Gaussian doping profile is of **P type / Acceptor** in **PMOS** & **N type /Donor in NMOS** starts below the **Oxide** layer and from **top to bottom** towards both extreme left to the **Source** as well as extreme right to the **Drain with** the dimensions **(L=0.01um x H=0.2um)** along with the **doping conc.(1e+18) /cm^3** and the **Y-characteristics** length will be **0.005um** with **X-Y ratio** of **1.**

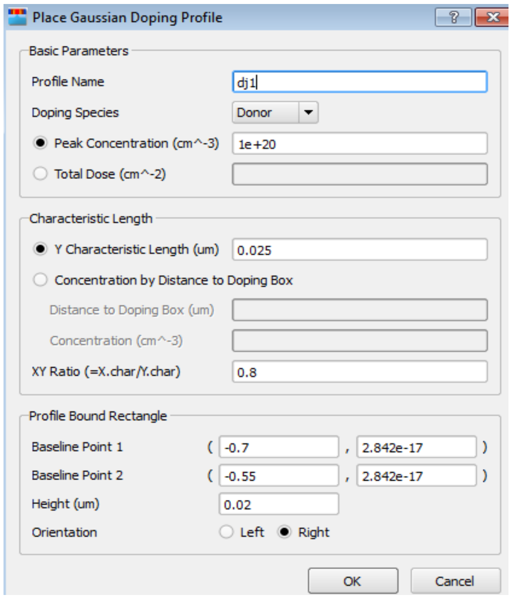


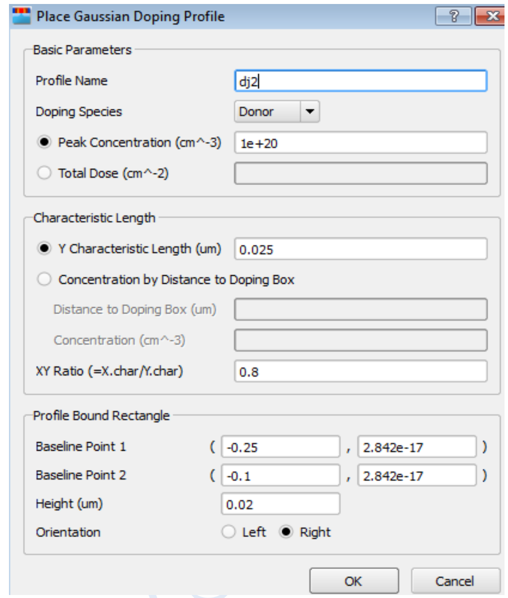


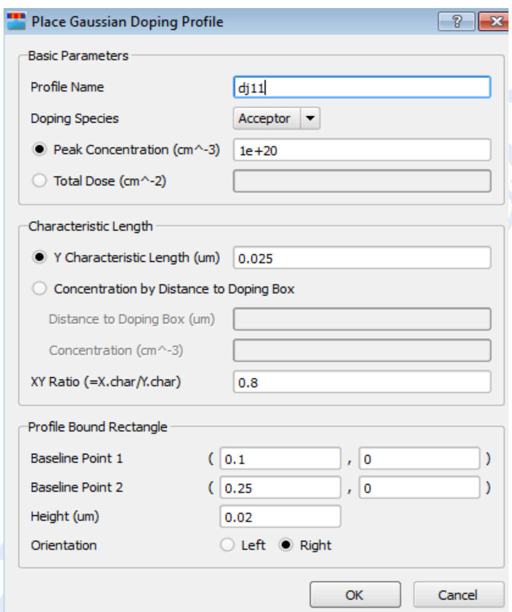


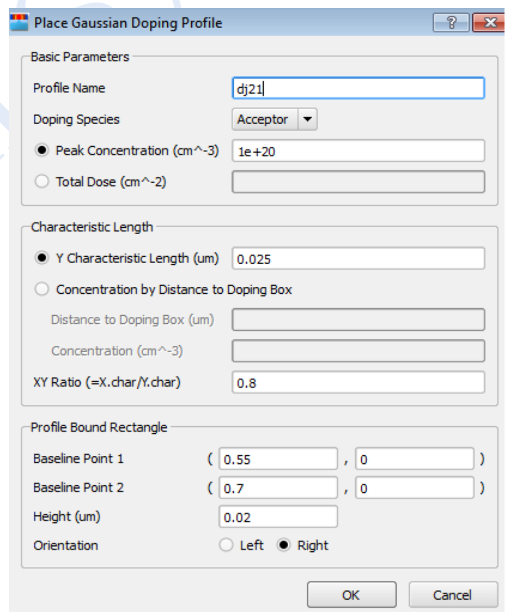


- Third is again Gaussian doping profile is of **P type / Acceptor** in **PMOS** & **N type /Donor in NMOS** starts below the **Oxide** layer and from **top to bottom** towards both extreme left to the **Source** as well as extreme right to the **Drain with** the dimensions **(L=0.02um x H=0.15um)** along with the **doping conc. (1e+20) /cm^3** and the **Y-characteristics** length will be **0.025um** with **X-Y ratio** of **0.8.**









- Fourth doping profile is of **N type /Donor** in **PMOS** & **P type / Acceptor in NMOS** for the **threshold voltage implant** doping with the doping concentration **(1e+18) /cm^3** along with the characteristics length of **0.01um** and **X-Y ratio** is **1**.

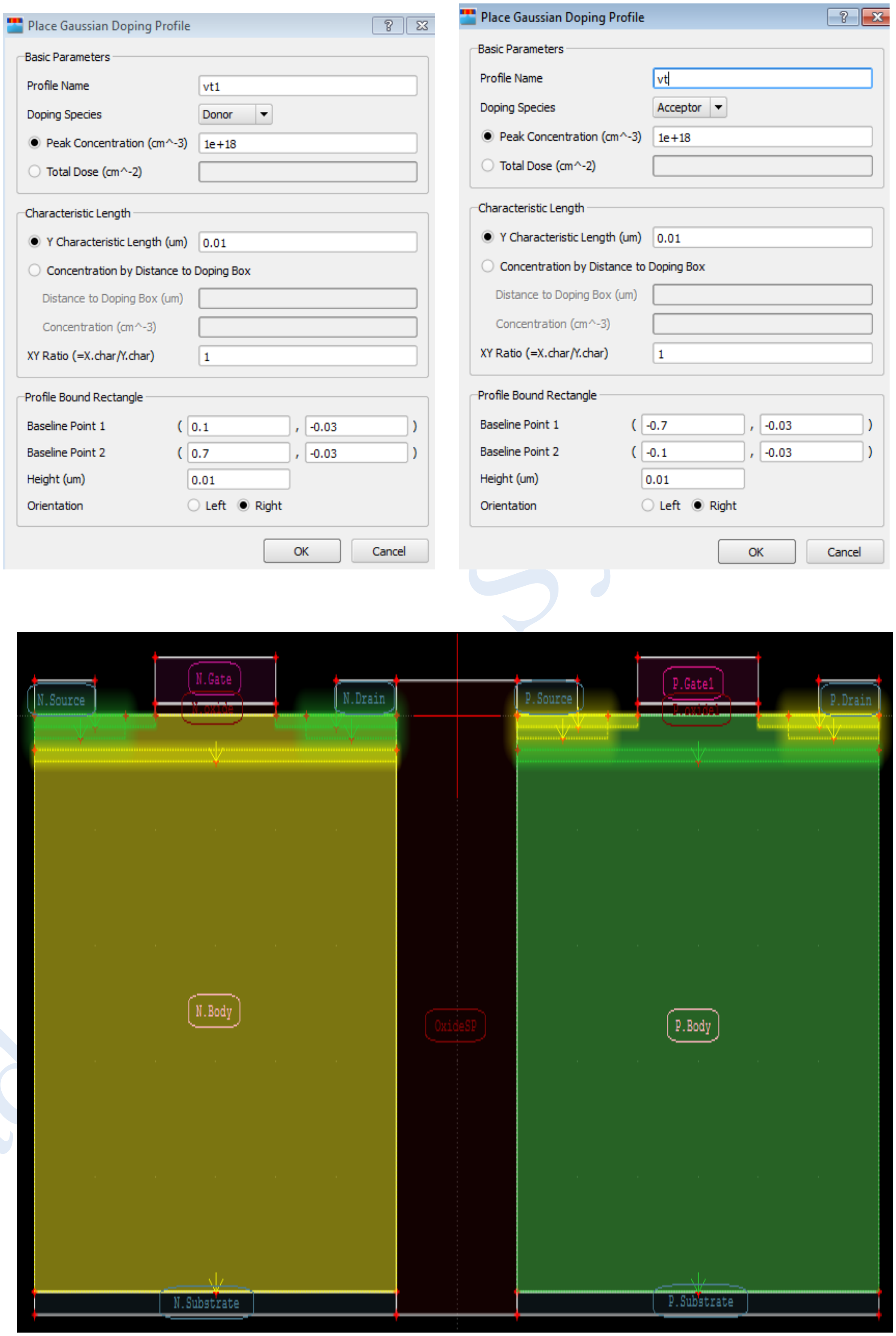


Fig 4(m) Doping Profile structure view

10. Now with the option **Do Mesh [**]we can meshed the device and refine the mesh with the option **Refine Existing Mesh [ ]** and we can also do the mesh by **spring method** ,the area of junction will be so denser after refining it 2-3 times ,the tool automatically detect the Junction of material and used to do the denser mesh at junctions automatically

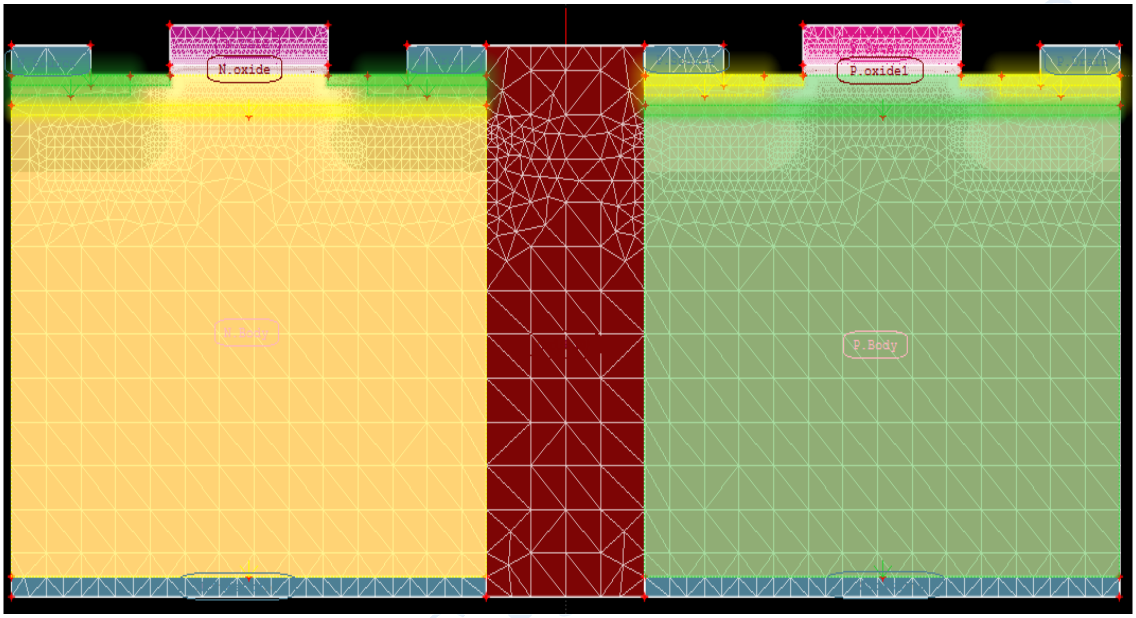


Fig 4(n) Meshing of CMOS

11. After the meshing being done we will save this file to **.tif** file using **Device** option in menu bar above we will get an option below "**Save mesh to file**"
12. After the mesh file saved to .tif file **go to the file option above** and open the **Device simulation**
13. From the **folder** below **Setup** on the left hand pellet with the location we can open the .tif file and it will take some time or earlier in loading the structure from .tif .After loading the file, In the middle electrodes are shown also e.g. **GATE, SOURCE, DRAIN** and **SUBSTRATE** of **NMOS** and **PMOS**

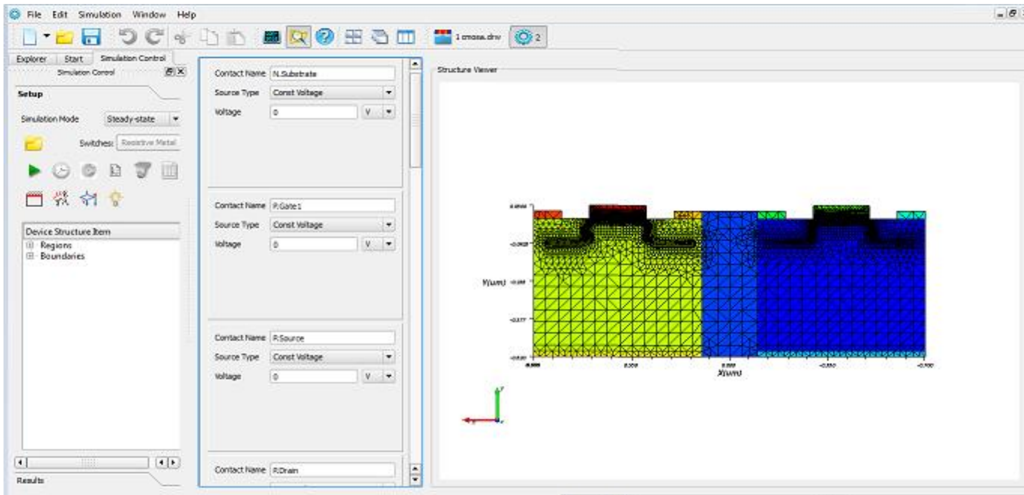


Fig 4(o) CMOS Simulation without interconnect

14. We will interconnect the **Gates**, **Drains** of **PMOS** & **NMOS** together along with **VDD**(from the interconnection of **Source** and **Substrate** of **PMOS**) and **GND**(from the interconnection of **Source** and **Substrate** of **NMOS**) then we will apply biasing as shown in fig below
15. For interconnections go Boundary condition[ ] and click on to interconnect [Interconnect] then connect Both the **Gates**, **Drains**, **Source** & **Substrate** of **NMOS** & **PMOS** as shown below

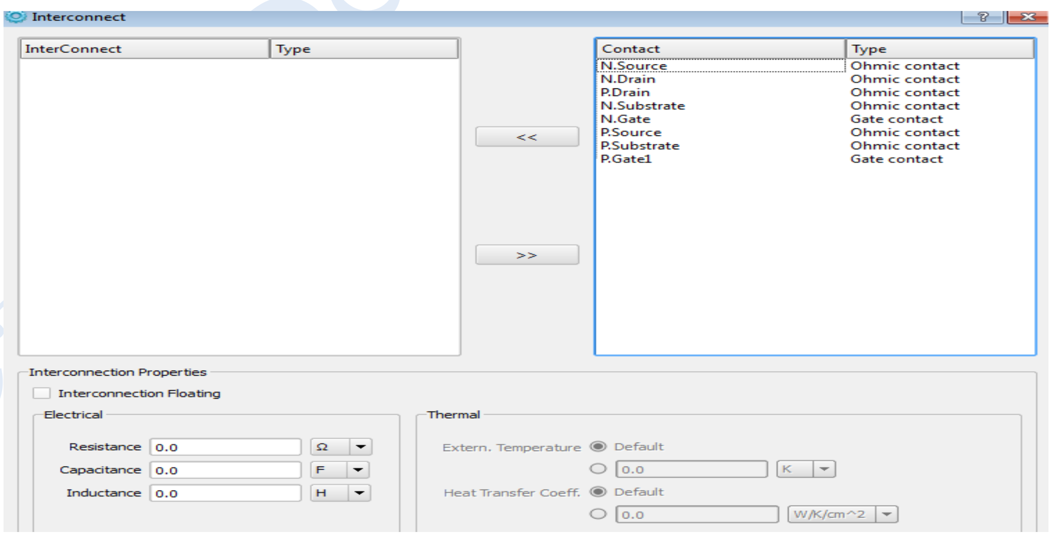


Fig 4(p) Simulation without interconnects

We will select two electrodes together and with the help of the [<<] we will interconnect the two electrodes and the electrodes will be shorted and stored into the left hand side table as shown below

If there will be wrong selection of the electrodes connected together then we can reverse the steps by using the option [>>] and we will use some resistance in parallel with output voltage (e.g. 5Kohm here)

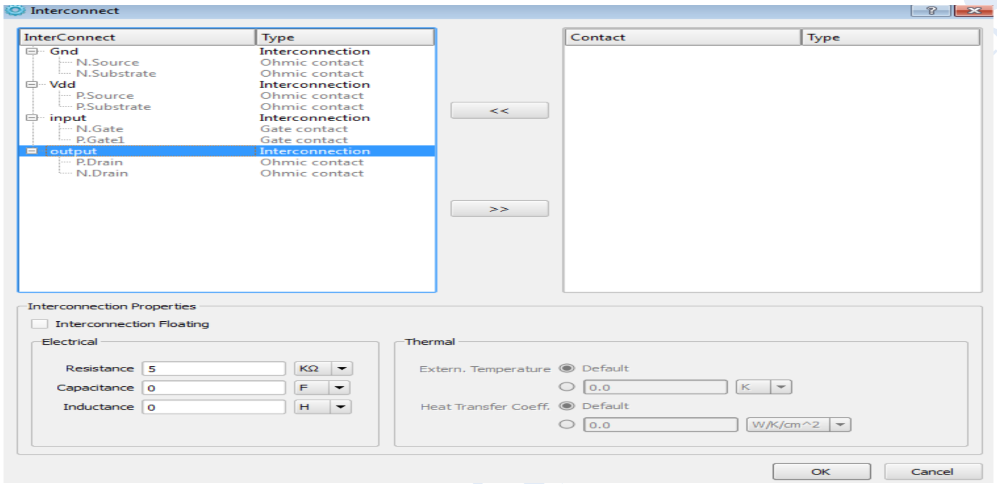


Fig 4(q) Simulation interconnects

16. Now after these steps the device will have four electrodes i.e. **INPUT, OUTPUT, VDD** & **GROUND** as shown below in the figure**.**

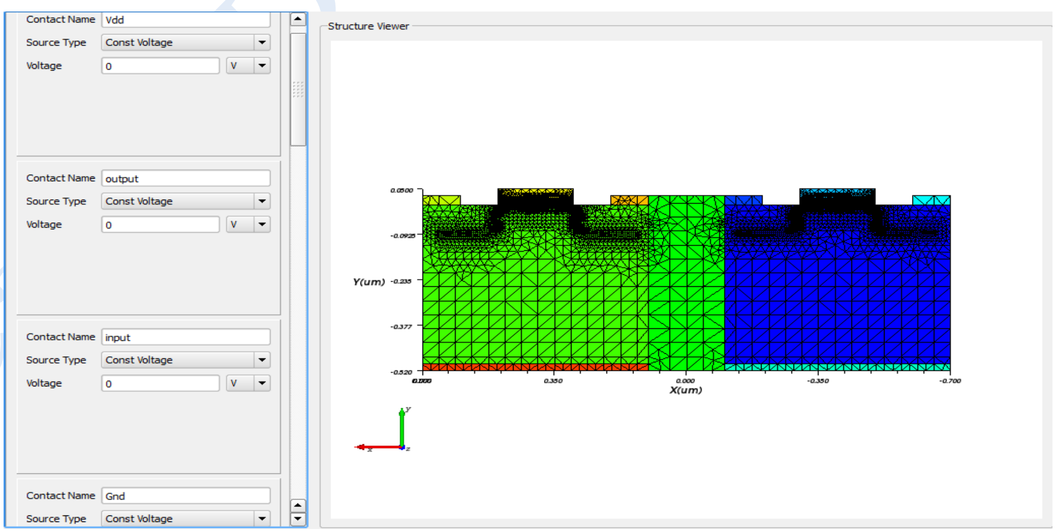


Fig 4(r) CMOS Simulation with interconnect

For VTC

17. Now Provide some Voltage Sweep biasing to the **input** (2v) and **output** with voltage (left unchanged) and some constant supply to the **VDD** (1v) along with **GND** (left unchanged) then with the help of **Run** [ ] button we can simulate our device by firstly save as a **.sim** file and then **create a folder** named as results or run or as per user wants to give name to it, after choosing the folder for simulation our simulation will be submitted and will give the results or we can open the file **result.dat** from the folder we have selected to simulate in.
18. Results with Spreadsheet and Plot are given below:

Vapp(Vdd) [V]	P(Vdd) [V]	I(Vdd) [A]	Vapp(input) [V]	P(input) [V]	I(input) [A]	Vapp(output) [V]	P(output) [V]	I(output) [A]	Power [W]
1	1	4.88498130835069e...	0.15	0.15	0	0	0.99999972602322	-1.11022302462515...	4.88498130835069e...
1	1	1.3988810110277e-11	0.2	0.2	0	0	0.999998074512227	0	1.3988810110277e-11
1	1	4.01900734914307e...	0.25	0.25	0	0	0.999984948850352	1.1102230246251e-13	4.01900734914307e...
1	1	1.16906484493029e...	0.3	0.3	0	0	0.999875135004563	0	1.16906484493029e...
1	1	3.43058914609173e...	0.35	0.35	0	0	0.998917451038858	0	3.43058914609173e...
1	1	1.01052499701382e...	0.4	0.4	0	0	0.988891824283214	0	1.01052499701382e...
1	1	1.83819626187187e...	0.45	0.45	0	0	0.133091052824982	0	1.83819626187187e...
1	1	1.15785159238158e...	0.475	0.475	0	0	0.0131061551905109	-1.7347234759736e-...	1.15785159238158e...
1	1	6.72017996805607e...	0.5	0.5	0	0	0.00378343554513436	0	6.72017996805607e...
1	1	2.25486296301369e...	0.55	0.55	0	0	0.000409794343297...	5.42101086198324e...	2.25486296301369e...
1	1	7.63833440942108e...	0.6	0.6	0	0	4.77755892729926e...	-6.77626357747905...	7.63833440942108e...
1	1	2.62012633811537e...	0.65	0.65	0	0	5.83362916187655e...	-8.47032945013527...	2.62012633811537e...
1	1	9.10382880192628e...	0.7	0.7	0	0	7.71511824700647e...	1.05879118669529e...	9.10382880192628e...
1	1	3.21964677141295e...	0.75	0.75	0	0	1.17270425050235e...	1.32348895622719e...	3.21964677141295e...
1	1	1.11022302462516e...	0.8	0.8	0	0	2.16617195041213e...	-6.61744491684559...	1.11022302462516e...
1	1	4.44089209850063e...	0.85	0.85	0	0	4.94978329277125e...	-8.27180563714589...	4.44089209850063e...
1	1	2.22044604925031e...	0.9	0.9	0	0	1.39403822135236e...	2.06795140928647e...	2.22044604925031e...
1	1	1.11022302462516e...	0.95	0.95	0	0	4.92456750846369e...	0	1.11022302462516e...
1	1	0	1	1	0	0	2.2639486473708e-10	0	0

Fig 4(s) CMOS Simulation VTC Results

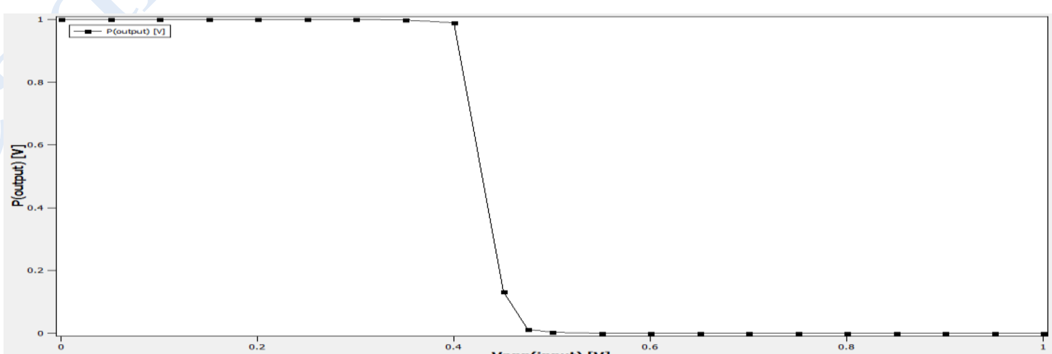


Fig 4(t) CMOS Simulation VTC Plots

For Transient Analysis

19. Firstly change the simulation mode to transient and Provide some Voltage Pulsated source to **input** and **output** will be (left unchanged) and some constant supply to the **VDD**(1v) along with **GND** (left unchanged) then with the help of **Run** [ ] button we can simulate our device by firstly save as a **.sim** file and then **create a folder** named as results or run or as per user wants to give name to it, after choosing the folder for simulation our simulation will be submitted and will give the results or we can open the file **result.dat** from the folder we have selected to simulate in.
20. For transient analysis simulation settings first change the source as if we want voltage Pulse/sin/DC. we will select **Pulse** source for the **INPUT** and constant source for the **VDD** and for the **INPUT** source below are the simulation settings shown in the figures Go to input and click edit [Edit] then a window will be open as below

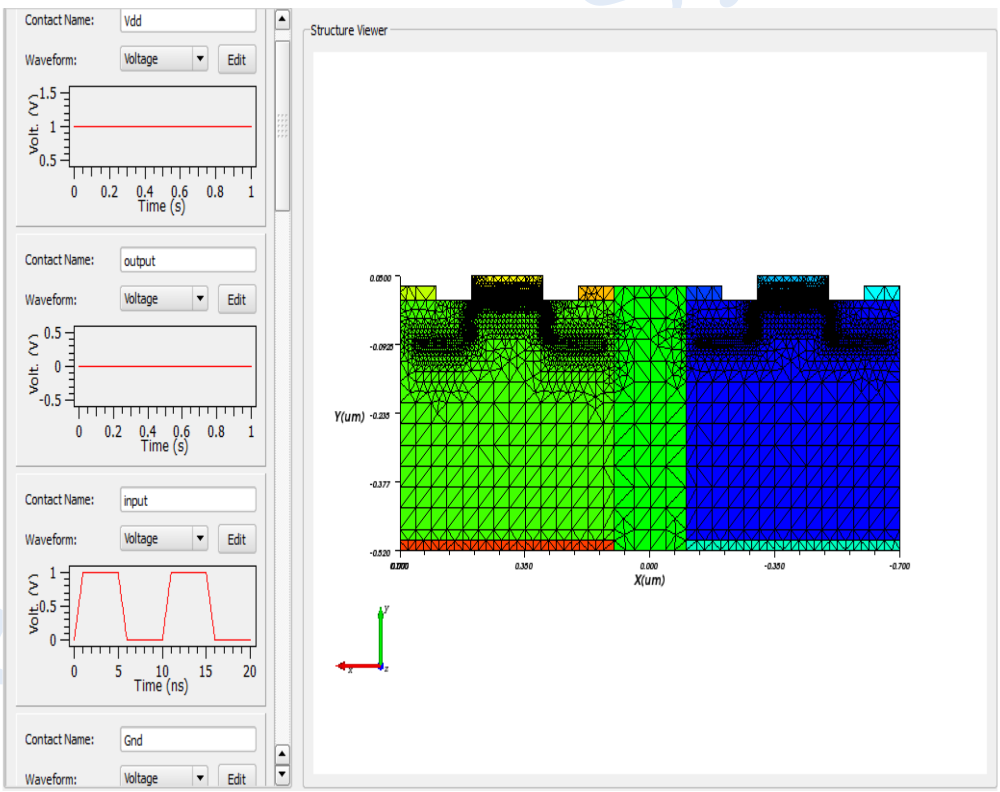


Fig 4(u) CMOS Transient Simulation Mode

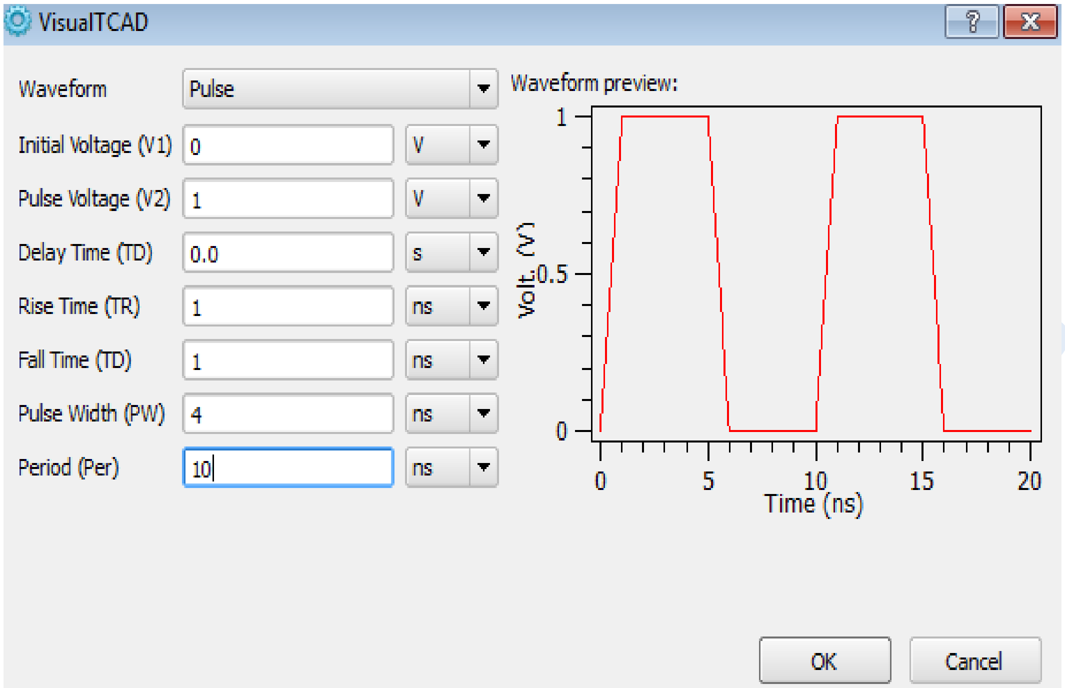


Fig 4(v) CMOS Transient Voltage source settings

21. After this we will save the file and submit the simulation with the help of Run button[ ]
22. A popup window will generate for time steps and for what maximum time we want to simulate the device, put the relevant values and press ok

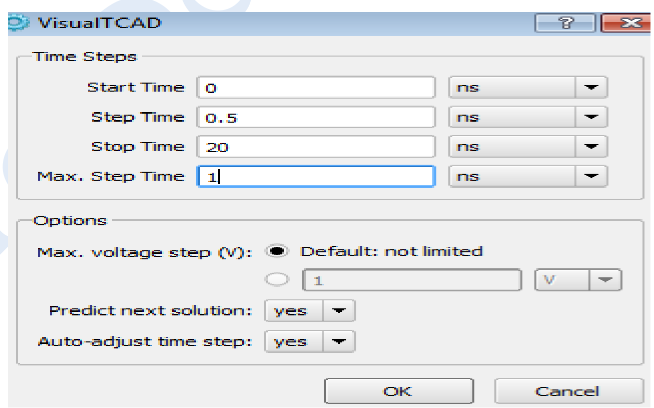


Fig 4(w) CMOS Transient Mode time settings

23. Our simulations has been submitted get the results and plot the transient response of **CMOS**

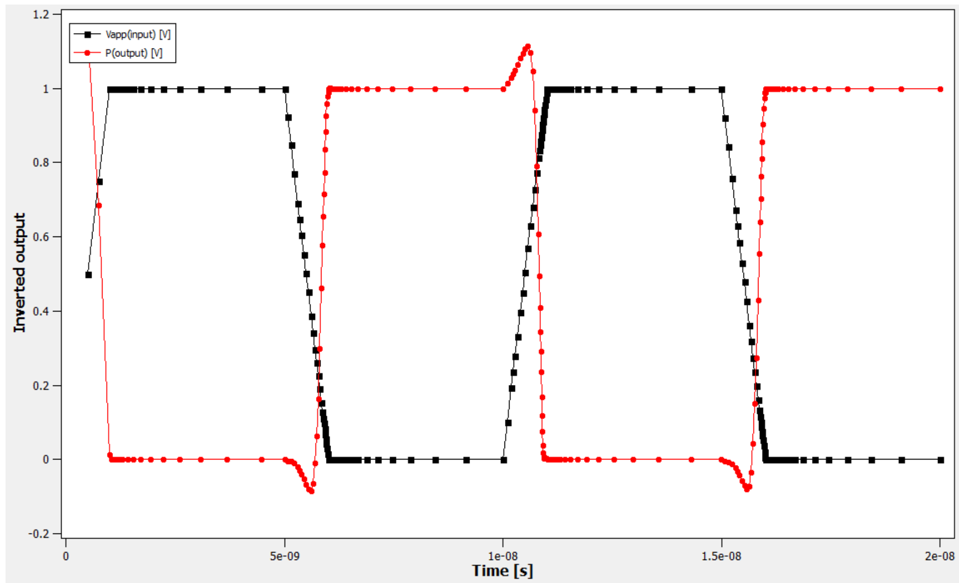


Fig 4(x) CMOS Transient plot