2. NMOS

AIM: To study the N-MOSFET and plot the I-V characteristics curves using simulation

Tool used: Some study about N-MOSFET and Cogenda Visual TCAD tool

Theory: N-MOSFET is a type of transistor and basically a four terminal voltage controlled device used in the electronic circuits with the terminal names are **GATE, SOURCE, DRAIN, and SUBSTRATE**

- There are two types of N-MOS (i) **Depletion Type** (ii) **Enhancement Type**
- **Depletion Type :** There is the presence of impurity in the substrate during the fabrication process that makes near the channel region that makes easy the flow of current even when there is no biasing due to the presence of a channel already
- **Enhancement Type :** There is the mobility is blocked of those minority charge particles in the substrate by using **Voltage threshold doping** to enhance the device
- **Voltage threshold doping :** During the fabrication process a doping with is done below the gate region to enhance the threshold voltage of the device so that device will not start very sooner due to the presence of minority charge particles , with the help of this doping the holes and the electron recombination takes place and the area left below gate is remain neutral until the biasing with suitable work function of the gate material is applied on the device

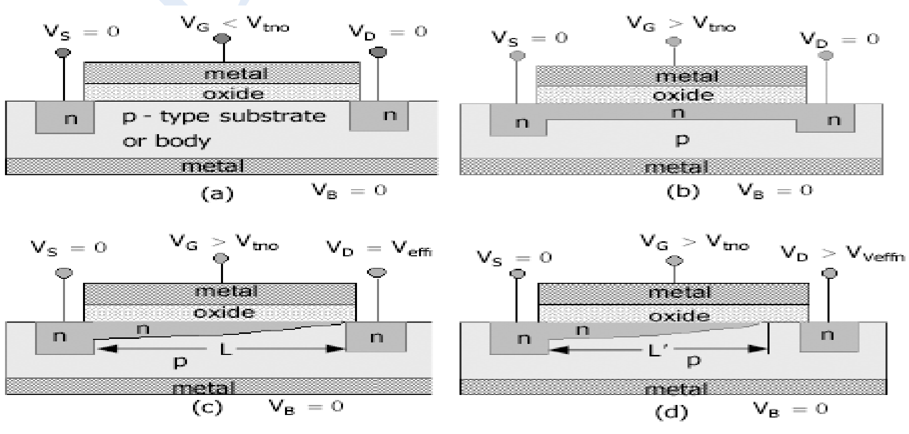


Fig. 2(a) Types of MOSFET

OPERATIONS

- when we apply the constant biasing for **DRAIN** and voltage sweep biasing on **GATE** to have the characteristics plot between the Voltage (applied on gate) Vs current from **DRAIN** this is known as **TRANSFER** characteristics
- when we apply the voltage sweep biasing on **DRAIN** and fix biasing on **GATE** to have the characteristics plot between the Voltage (applied on drain) Vs current from **DRAIN** this is known as **OUTPUT** characteristics
- Below in figure are the diode standard characteristics

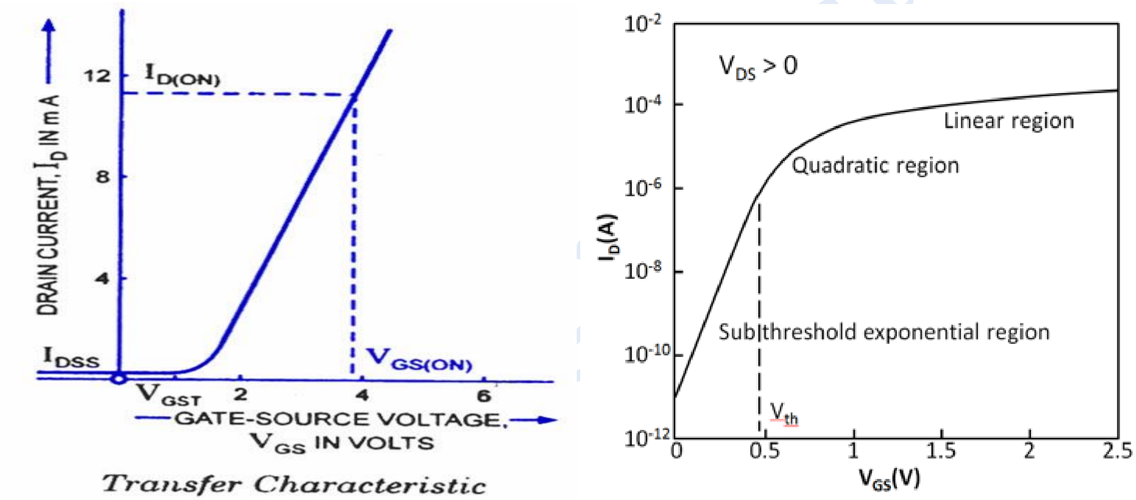


Fig 2(b) Transfer characteristics Curve

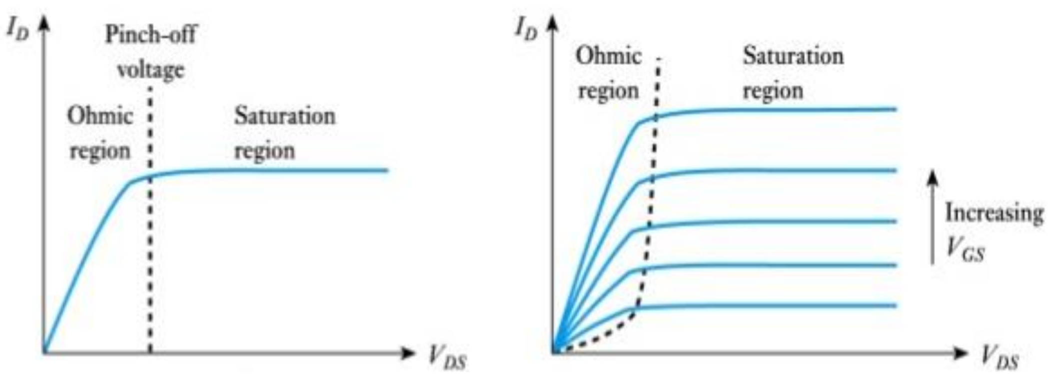


Fig 2(c) Output characteristics Curve

Procedure:

1. Open the Visual TCAD tool by clicking on the icon in start menu for windows user and for Linux(ubuntu or rhel) open the terminal [ctrl+alt+t]
2. Go to the new file and choose the Device Drawing as an option
3. A window with black background will open up with default grid spacing width of 0.01um
4. He are preparing a N-MOSFET of (L=0.6um x H=0.5um) with the Source region and the Drain region (L=0.03um x H=0.1um) and Substrate (L=0.6um x H=0.5um) along with Gate (L=0.2um x H=0.03um) and oxide (L=0.2um x H=0.01um).
5. With the help of the shapes given on the left top use rectangular shape to design the device
6. The actual shape is designed below using the rectangular shape

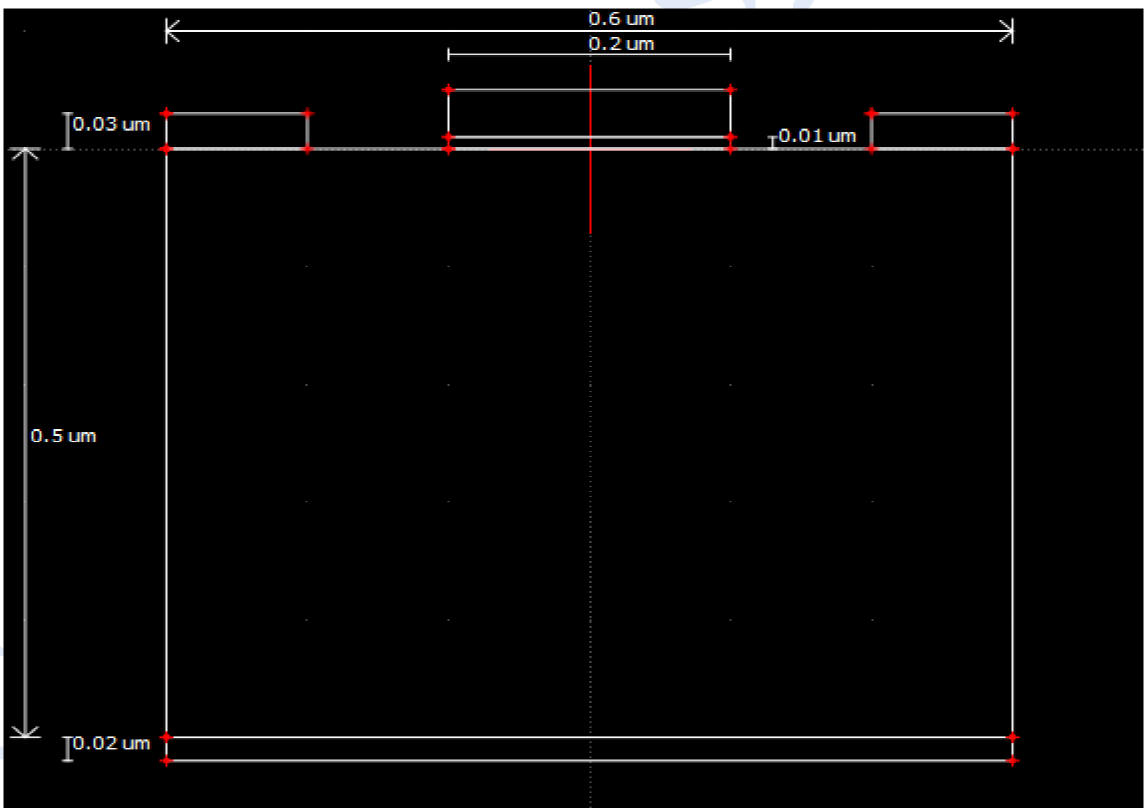


Fig 2(d) Structure of a MOSFET

7. Add the region label substrate (0.6um x 0.5um) from the silicon material with the mesh size assumed as 1/10th of the block size e.g. as it is of 4um block length so max. meshing size will be 0.05um

8. Add the region label of the another three blocks that are Source(L=0.1um x H=0.03um), Drain(L=0.1um x H=0.03um), Substrate (0.6um x 0.02um) with the aluminum (Al) region and keep the max mesh size same as given by default as we don't require to calculate on the metal-semiconductor junctions. Another two regions are Gate with material (N Poly Silicon) along with the oxide region below Gate region with material (silicon oxide) having the mesh size of **0.05**.

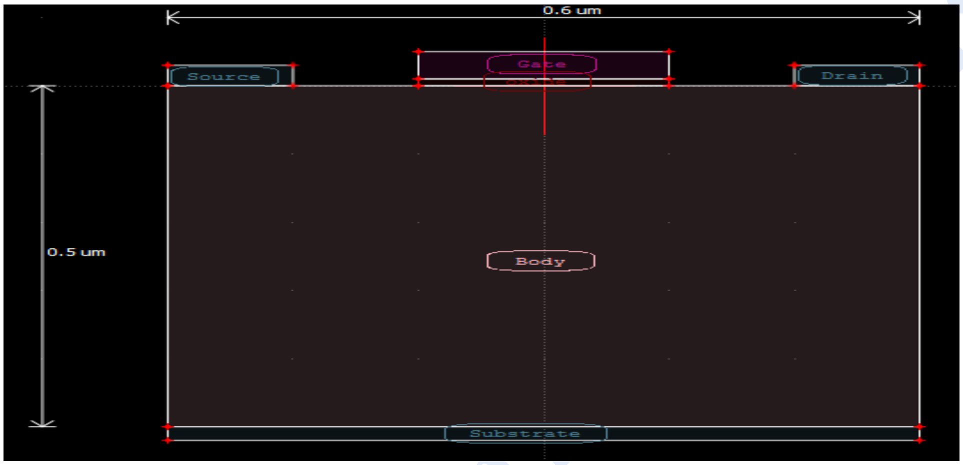


Fig 2(e) Structure of a MOSFET with all regions with material

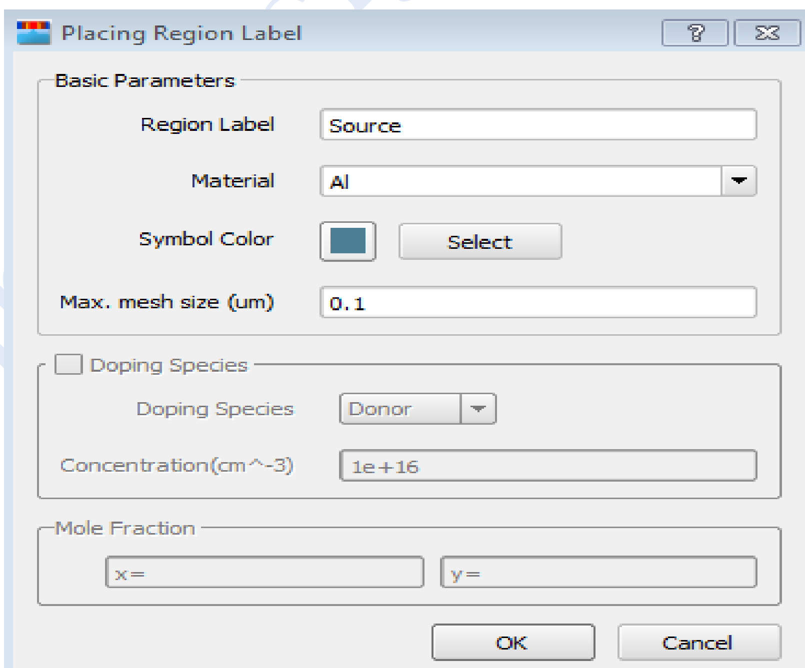


Fig 2(f) Source region with material meshing and details

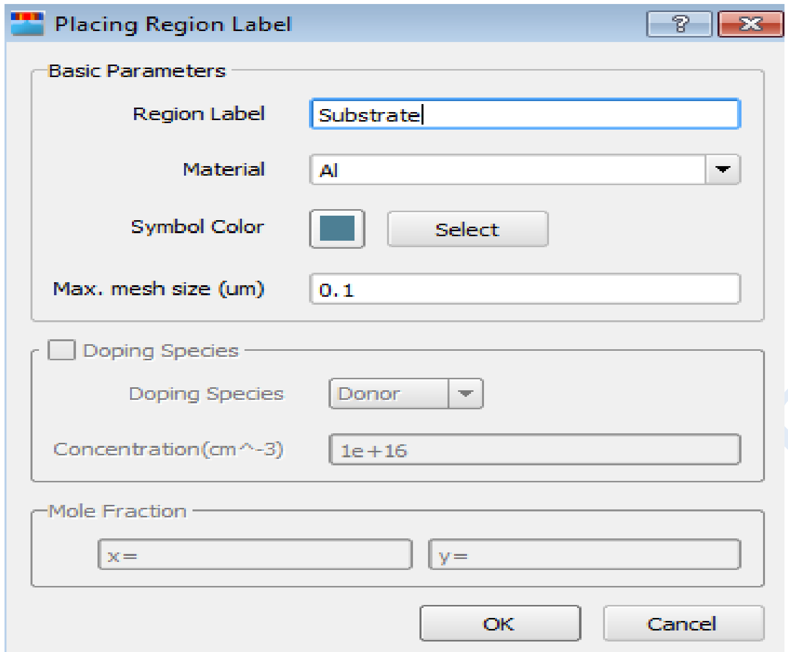


Fig 2(g) Substrate region with material meshing and details

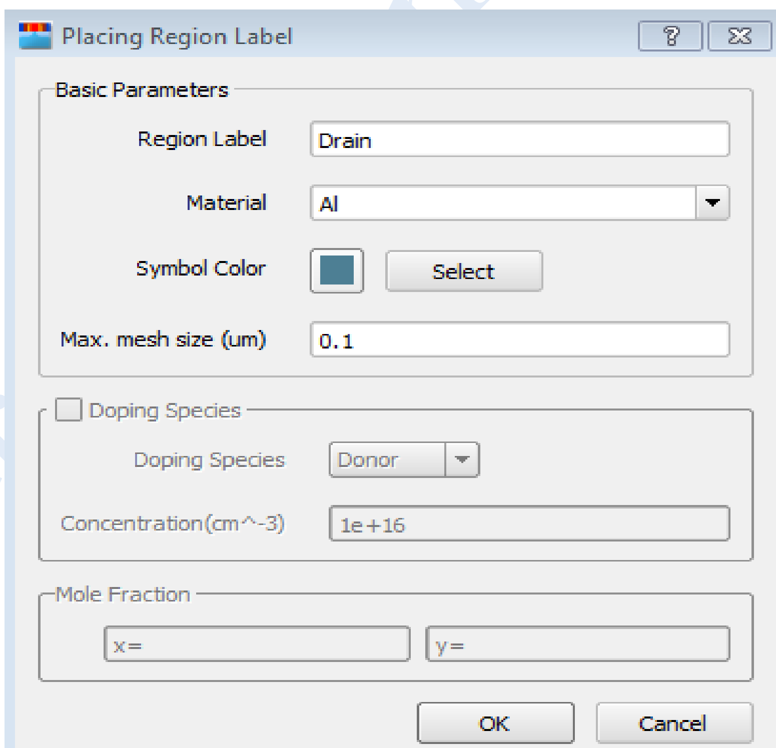


Fig 2(h) Drain region with material meshing and details

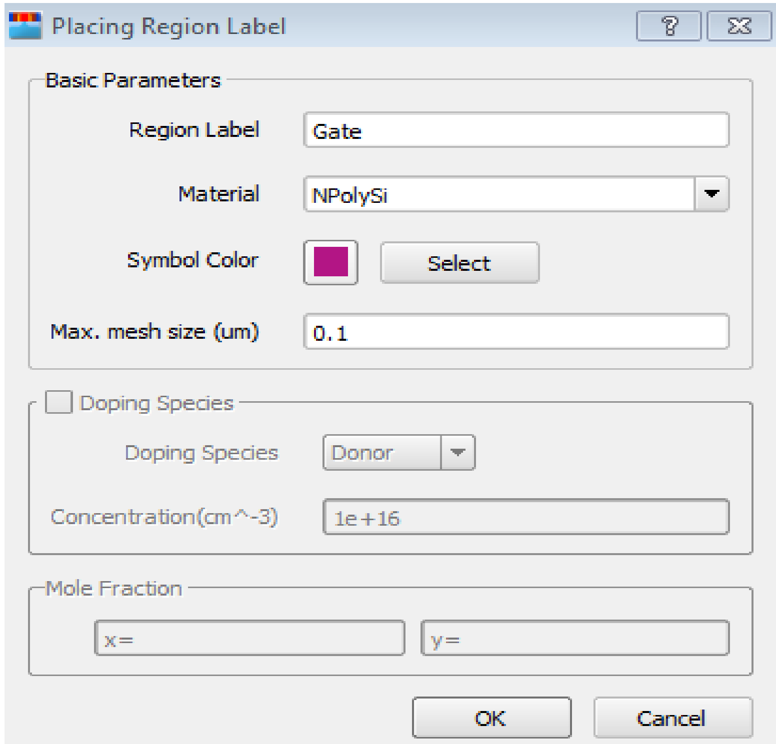


Fig 2(i) Gate region with material meshing and details

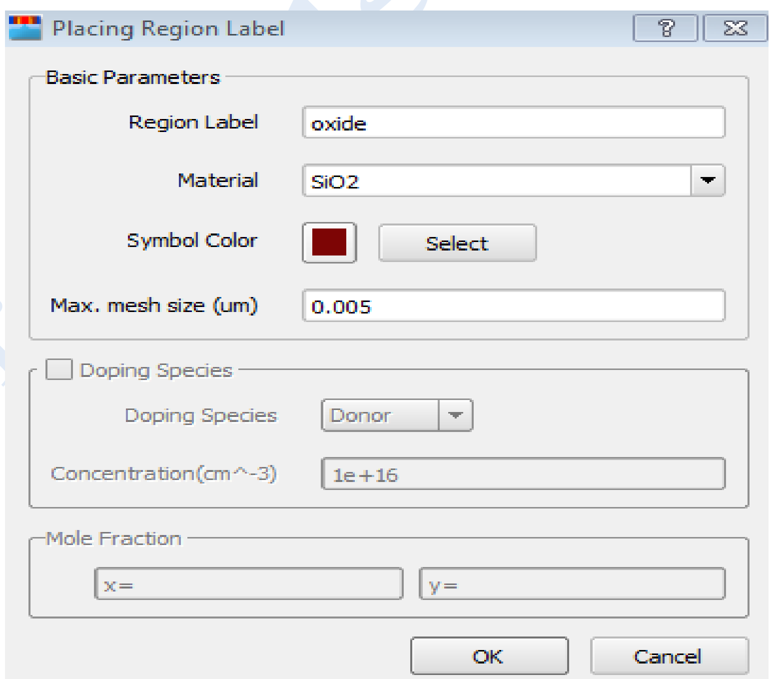


Fig 2(j) Oxide region with material meshing and details

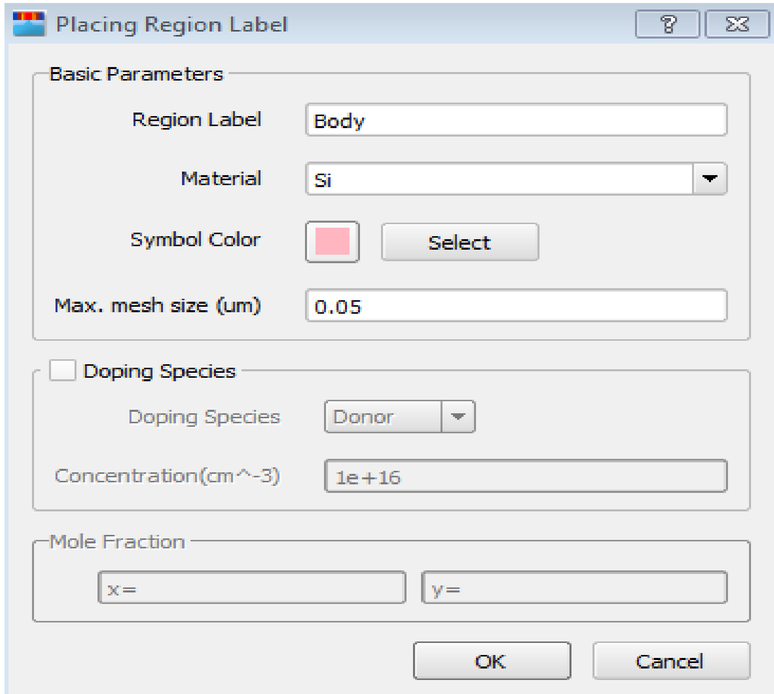
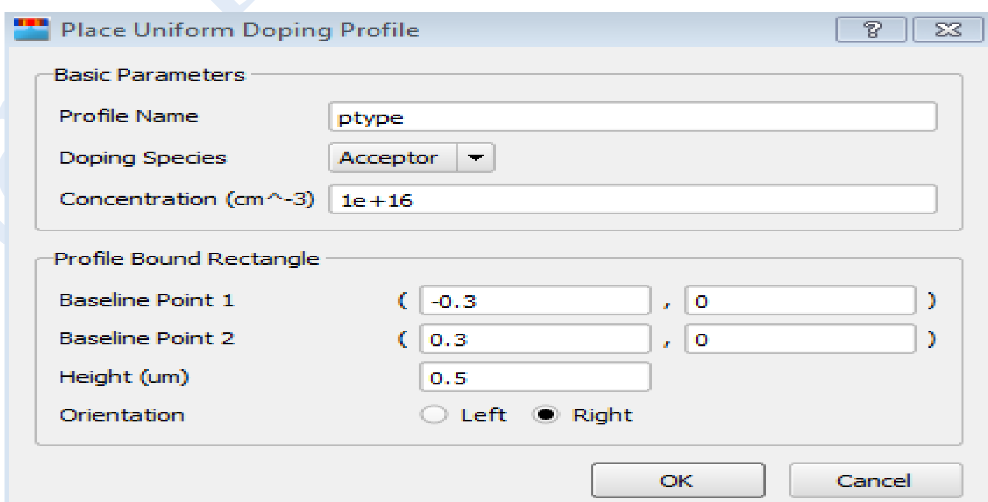


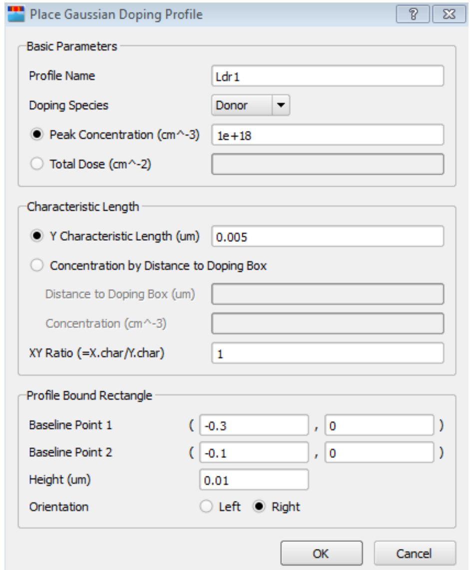
Fig 2(k) Body with material and meshing Details

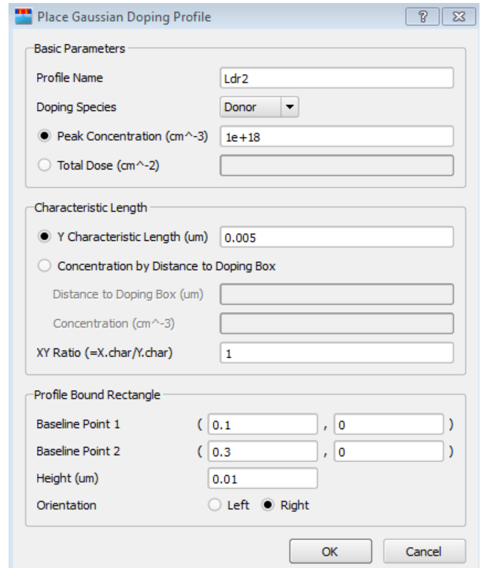
9. Now with the option of Add Doping Profile we will make the two regions

- First doping profile **is uniform doping profile** of **P type** /**Acceptor** with the doping concentration of **(1e+16)/cm^3** across the whole region from top to bottom uniformly or we can say (0.5um x 0.6um) above the **Body** region from top to bottom

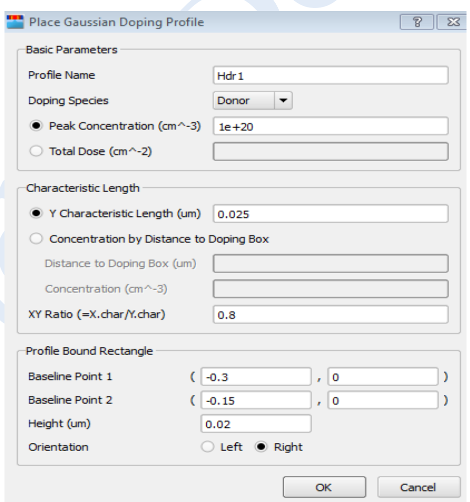


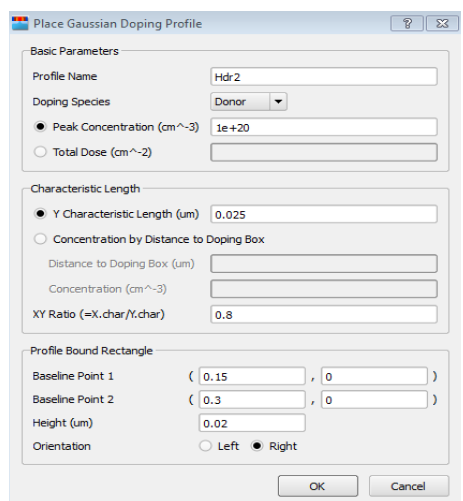
- Second doping profile is of **N type / Donor** starts below the **Oxide** layer and from **top to bottom** towards both extreme left to the **Source** as well as extreme right to the **Drain** with the dimensions (0.01um x 0.2um) along with the **doping conc.(1e+18) /cm^3** and the **Y-characteristics** length will be **0.005um** with **X-Y ratio** of **1.**



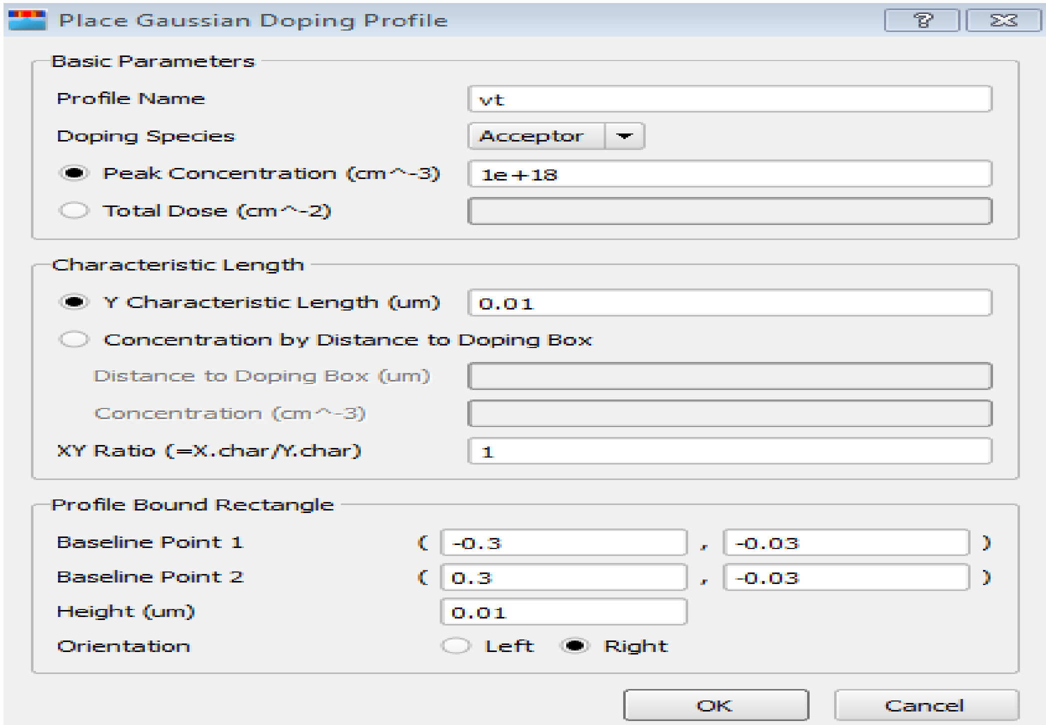


- Third doping profile is also of **N type / Donor** starts below the mid of the **Source** and **Drain** with **Oxide** as common, from **top to bottom** towards both extreme left to the **Source** as well as extreme right to the **Drain with** the dimensions (0.15um x 0.02um) along with the **doping conc. (1e+20) /cm^3** and the **Y-characteristics** length will be **0.025um** with **X-Y ratio** of **0.8.**





- Fourth doping profile is of **P type** /**Acceptor** for the **threshold voltage doping implant** with the doping concentration **(1e+18) /cm^3** along with the characteristics length of **0.01um** and **X-Y ratio** is **1**.



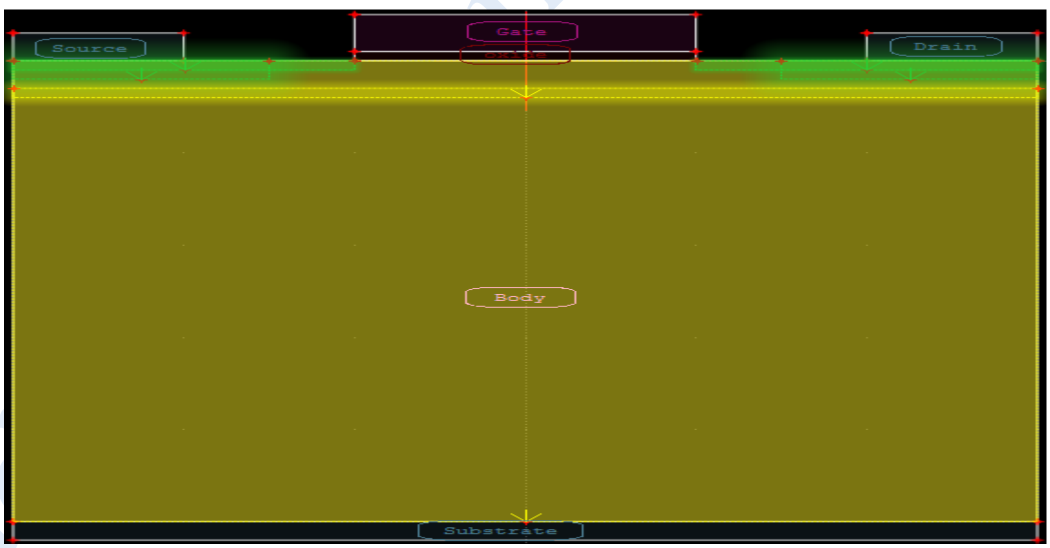


Fig 2(l) Doping Profile structure view

10. Now with the option **Do Mesh [**]we can meshed the device and refine the mesh with the option **Refine Existing Mesh [** **]** and we can also do the mesh by **spring method** ,the area of junction will be so denser after refining it 2-3 times ,the tool

automatically detect the Junction of material and used to do the denser mesh at junctions automatically

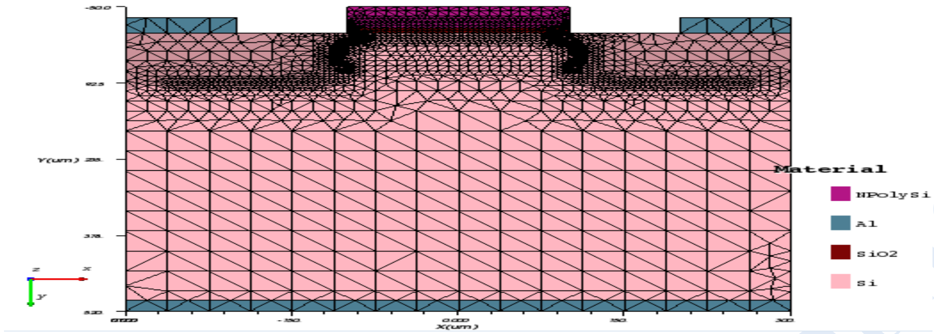


Fig 2(m) Meshing of NMOS

11. After the meshing being done we will save this file to **.tif** file using **Device** option in menu bar above we will get an option below “**Save mesh to file**”
12. After the mesh file saved to .tif file **go to the file option above** and open the **Device simulation**
13. From the **folder below Setup** with the location we can open the .tif file and it will take some time or earlier load the structure from .tif file along with the contacts shown on the middle electrode work area e.g. **GATE, SOURCE, DRAIN, and SUBSTRATE**
14. He will apply biasing as shown in fig below

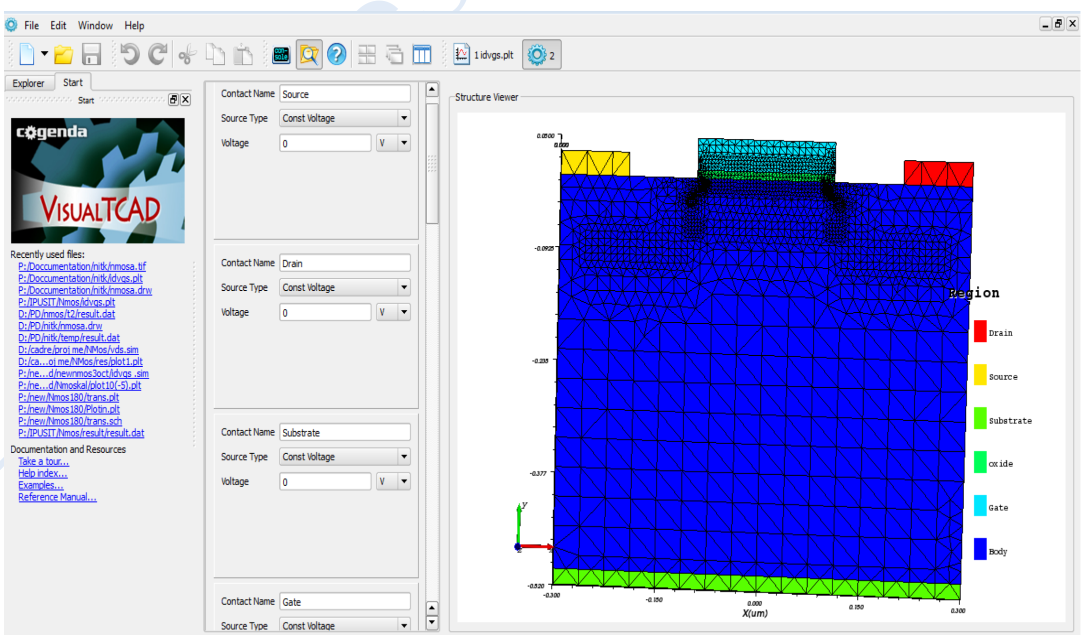
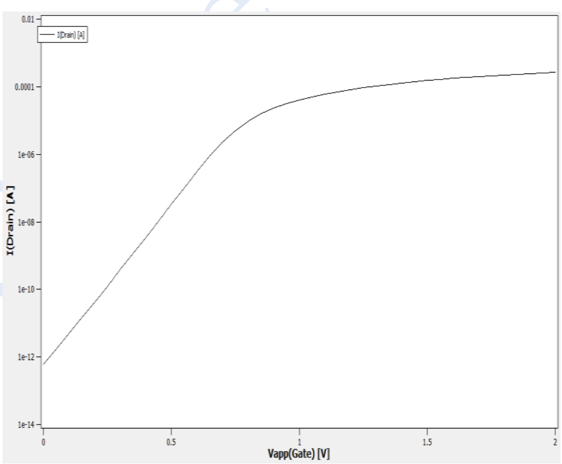


Fig 2(n) NMOS Simulation

15. Now Provide some Voltage Sweep biasing to the **GATE** (2v with step size 0.05) and **Drain** with Constant voltage and save with some name then with the help of **Run** button we can simulate our device by firstly save as a **.sim** file and then **create a folder** named as results or run or as per user wants to give name to it, after choosing the folder for simulation our simulation will be submitted and will give the results or we can open the file **result.dat** from the folder we have selected to simulate in.
16. Now we can **Plot the data** with the help of results or spreadsheets **between I(Drain)** and **V app(GATE)**
17. **Results with Spreadsheet and Plot are given below:**

	Ih(Source) [A]	Body_to_oxide) [A	Vapp(Drain) [V]	P(Drain) [V]	I(Drain) [A]	Ie(Drain) [A]	Ih(Drain) [A]	Vapp(Gate) [V]	P(Gate) [V]	I(Gate) [A]
1	-6.89990456897896...	0	1	1	6.15965699815153e...	6.15965699723089e...	9.20639985185704e...	0	0	0
2	-7.22698551757879...	0	1	1	1.7372975166195e-12	1.73729751652744e...	9.20638126766156e...	0.05	0.05	0
3	-7.57769492913987...	0	1	1	4.99115009356451e...	4.99115009347245e...	9.20636232671431e...	0.1	0.1	0
4	-7.9670746375647e-...	0	1	1	1.45176460259955e...	1.45176460259034e...	9.20634301653472e...	0.15	0.15	0
5	-8.43663333118416...	0	1	1	4.26566505493103e...	4.26566505492182e...	9.20632332300886e...	0.2	0.2	0
6	-9.02538214908178...	0	1	1	1.2652093627698e-10	1.26520936276888e...	9.20630324427478e...	0.25	0.25	0
7	-9.8364125941951e-...	0	1	1	3.78767863651263e...	3.78767863651171e...	9.20628282712358e...	0.3	0.3	0
8	-1.11136438208156...	0	1	0.999999999999999	1.14454985897038e...	1.14454985897029e...	9.20626226731337e...	0.35	0.35	0
9	-1.37750701187085...	0	1	0.999999999999997	3.49050386863315e...	3.49050386863305e...	9.20624221764749e...	0.4	0.4	0
10	-2.06722268000933...	0	1	0.999999999999989	1.07343047824373e...	1.07343047824372e...	9.20622474823229e...	0.45	0.45	0
11	-4.06394852953436...	0	1	0.999999999999967	3.32026694307062e...	3.32026694307061e...	9.20621633055171e...	0.5	0.5	0
12	-1.00748919880783...	0	1	0.999999999999897	1.02606187033119e...	1.02606187033119e...	9.2062367988733e-23	0.55	0.55	0
13	-2.8014886632669e-...	0	1	0.999999999999688	3.11733001332088e...	3.11733001332088e...	9.20634429292382e...	0.6	0.6	0
14	-7.82786296542709...	0	1	0.9999999999991	8.99717014451445e...	8.99717014451445e...	9.20668869440067e...	0.65	0.65	0
15	-2.00739941382778...	0	1	0.999999999997666	2.3340923545391e-06	2.3340923545391e-06	9.20756304972598e...	0.7	0.7	0
16	-4.42892065785615...	0	1	0.999999999994828	5.17162993564003e...	5.17162993564003e...	9.2093165454868e-23	0.75	0.75	0
17	-8.28549810283526...	0	1	0.999999999990309	9.69112229034722e...	9.69112229034722e...	9.21212463095065e...	0.8	0.8	0
18	-1.34886441784299...	0	1	0.999999999984212	1.57879951385534e...	1.57879951385534e...	9.21592276611793e...	0.85	0.85	0
19	-1.98004978539092...	0	1	0.999999999976818	2.31823967722485e...	2.31823967722485e...	9.22053658173671e...	0.9	0.9	0

Fig 2(o) NMOS Simulation Input Results



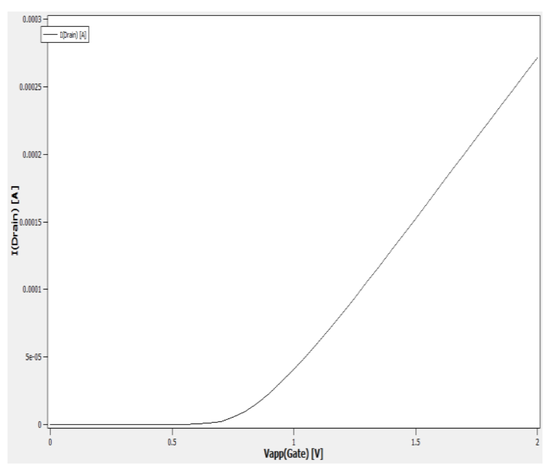


Fig 2(p) NMOS Simulation transfer characteristics Plots

19. He will also do the simulation to plot output characteristics by sweeping the voltage of **DRAIN** and making the contestant voltage supply at **GATE** shown in the figure below with results and also multiple results plot with different **GATE** voltage with the help of the option [ ] after the graph will be plotted

	x (Vapp(Drain) [V])	y (I(Drain) [A])@(gate=2v)	y (I(Drain) [A])@(gate=1v)	y (I(Drain) [A])@(gate=1.5v)	y (I(Drain) [A])@(gate=0.5v)
1	0	-3.73394811566893e-17	-3.98946e-17	-3.01911e-17	-1.87999e-16
2	0.05	3.82574042147394e-05	1.36015e-05	2.9468e-05	1.42184e-08
3	0.1	7.4528754848841e-05	2.29169e-05	5.63624e-05	1.69483e-08
4	0.15	0.000107996509518287	2.79641e-05	7.9774e-05	1.79224e-08
5	0.2	0.000138074410991677	3.02553e-05	9.9022e-05	1.86333e-08
6	0.25	0.000164431067555866	3.14186e-05	0.000113755	1.93129e-08
7	0.3	0.000186965131326279	3.22153e-05	0.000124076	2.00008e-08
8	0.35	0.000205762794874904	3.28859e-05	0.000130657	2.07067e-08
9	0.4	0.000221039390349455	3.35054e-05	0.000134649	2.14352e-08
10	0.45	0.000233086463694545	3.41016e-05	0.00013721	2.219e-08
11	0.5	0.000242265017376517	3.46867e-05	0.000139097	2.29743e-08
12	0.55	0.00024902523746555	3.52665e-05	0.000140679	2.37916e-08
13	0.6	0.000253907209407	3.58456e-05	0.000142116	2.46449e-08
14	0.65	0.00025748181615618	3.64281e-05	0.000143479	2.55378e-08
15	0.7	0.000260240501189021	3.70171e-05	0.000144801	2.64735e-08
16	0.75	0.000262523152224531	3.76151e-05	0.000146094	2.74557e-08
17	0.8	0.000264528981329749	3.8224e-05	0.000147372	2.8488e-08
18	0.85	0.000266362709461086	3.88454e-05	0.000148643	2.95745e-08
19	0.9	0.00026807764285724	3.94804e-05	0.000149911	3.07193e-08
20	0.95	0.000269705055246049	4.01295e-05	0.00015118	3.19271e-08

Fig 2(q) NMOS Simulation Output Results

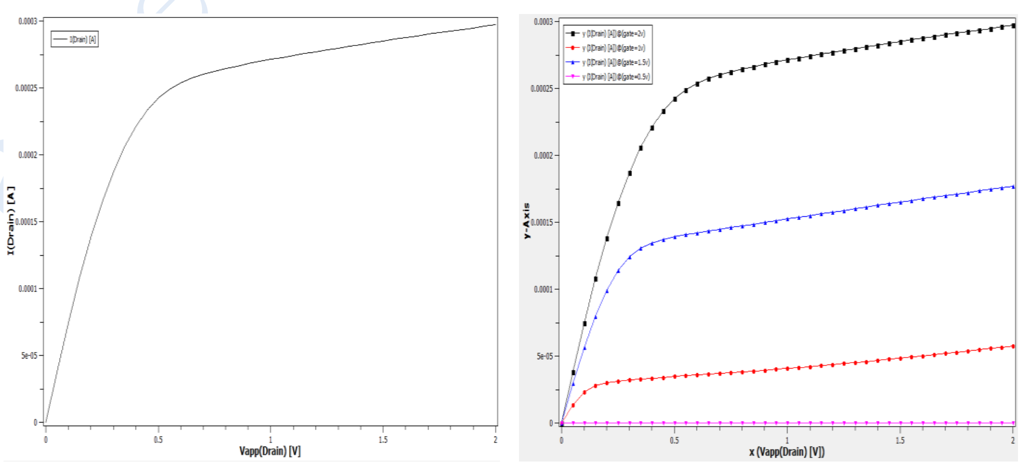


Fig 2(r) NMOS Simulation transfer characteristics Plots

20. We will also make circuit symbol and do the simulation of the NMOS as Circuit-Mixed Mode simulation
21. Now again load the .sim file into the device simulation option and select the **Circuit element** in **Simulation Mode** option as shown

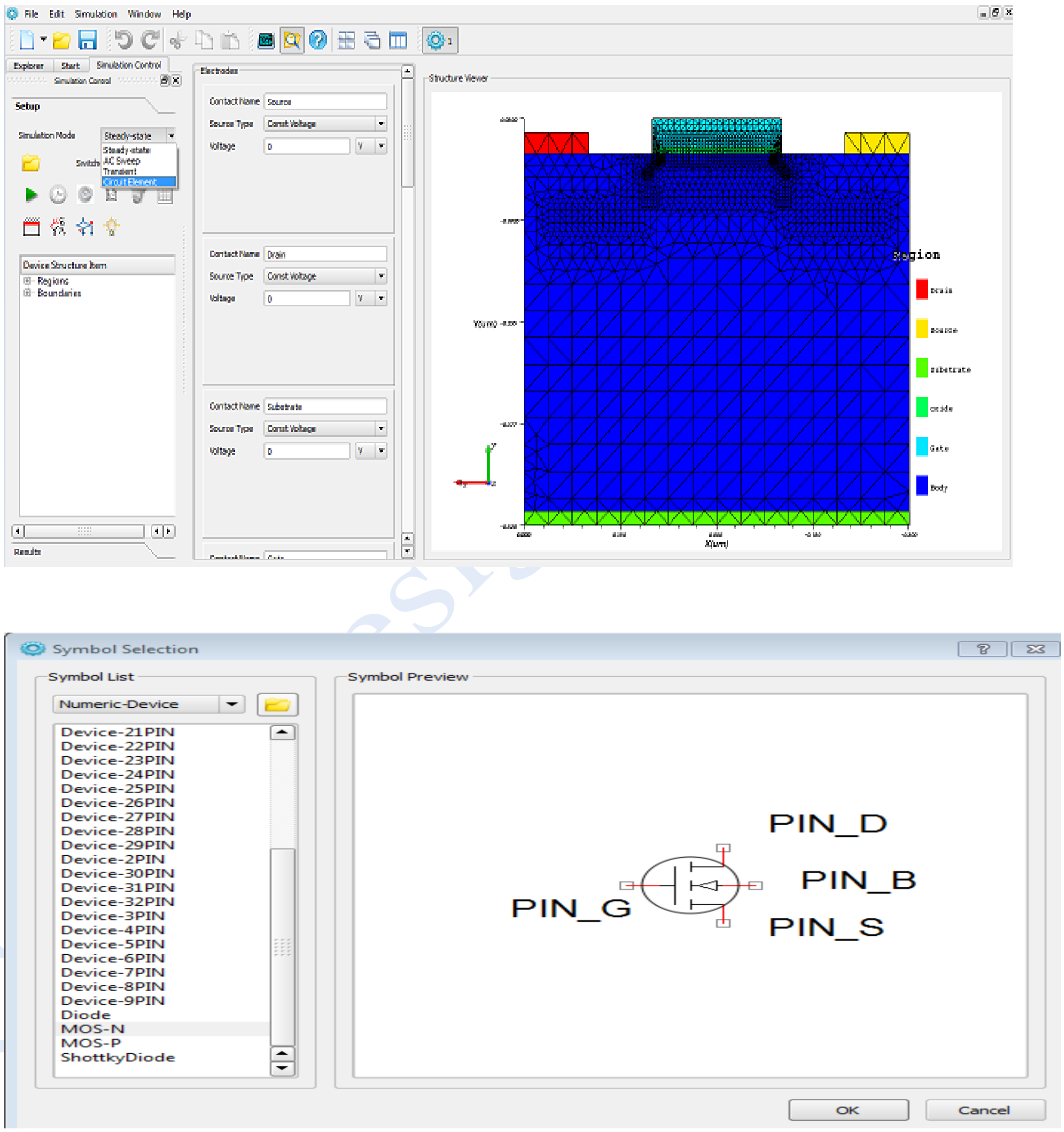


Fig 2(s) Circuit element conversion

22. Now go to the file > Circuit Schematic and load the **.sim** file and from the option Numerical device and make a mixed mode circuit by choosing the 180 nm technology of PMOS from the library for mixed mode simulation as shown in the figure

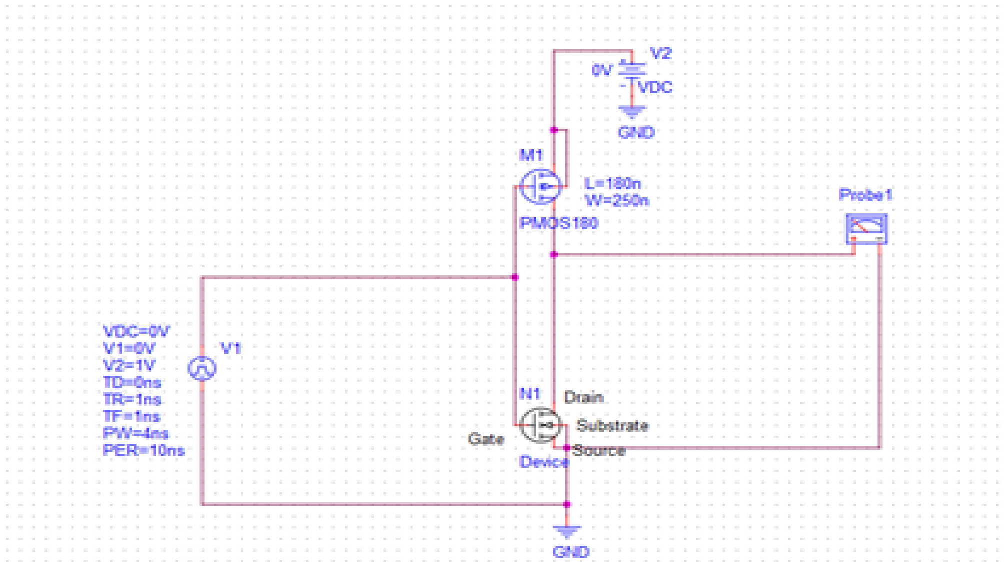


Fig 2 (t) Mixed mode simulation circuits

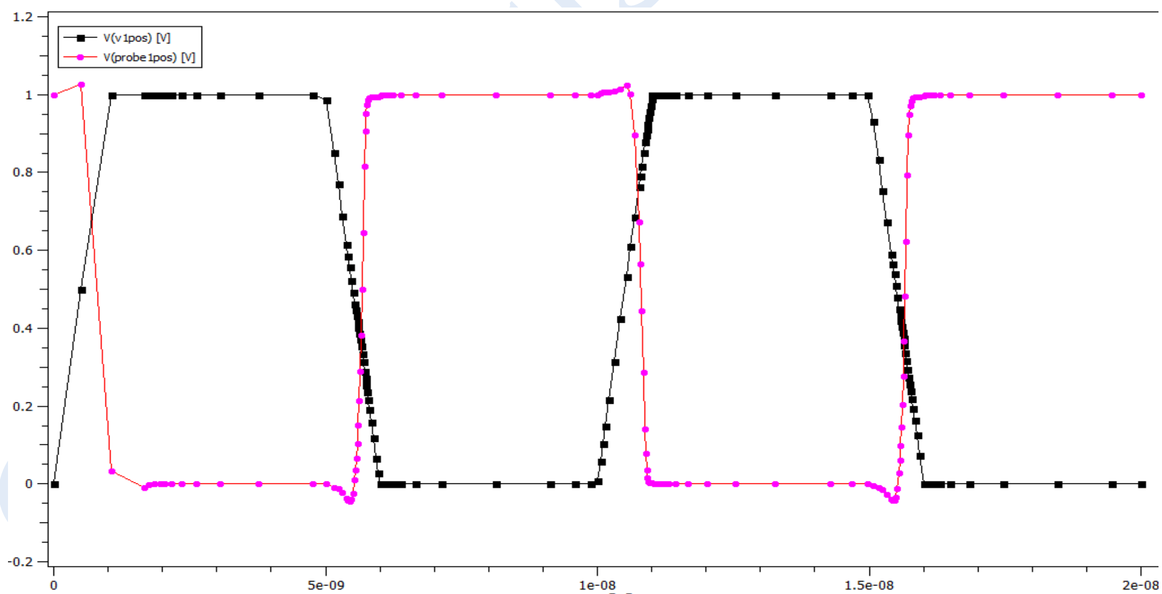


Fig 2(u) Transient characteristics