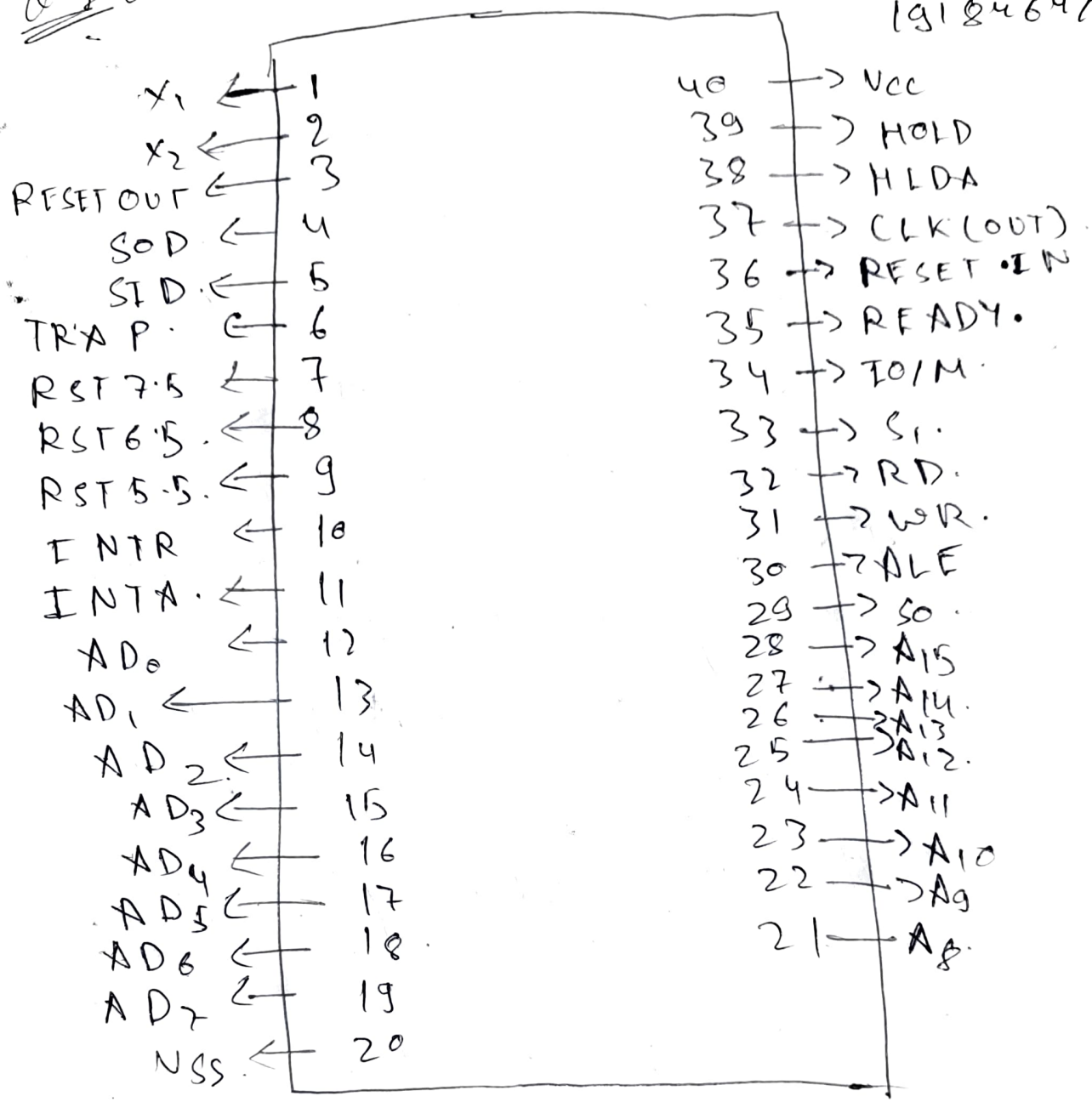
Q-1 a.

Mayank Kumar
19184641/34/K



Pin diagram of 8085 Microprocessor

ALE → Address latch Enable is at number 30 in the configuration we know that lower order bits of the 16-bit address bus are multiplexed with 8 bit data bus.

RD → Number at 32 in configuration & a low signal in this configuration pin shows the read operation. either of from I/O dev

or / from the memory write. Thereby indicating that the data bus is now in a state or position to accept the data / from the memory or I/O devices.

WR → It is the 37st pin in the pin diagram. & a low signal in this pin represents the write operation at the memory or I/O devices. This indicates that the data present in the data bus is be written into the desired Memory address or I/O device by the processor.

I/O/M → Pin number 34. & indicates the selection of a memory address or I/O device. This shows whether the read / write operation is to be carried out at the memory location or at the I/O device.

S_1 & S_0 → at 2982 33 in configuration: They are status signals. Show the type of recent operation of microprocessor

I/O/M	S_1	S_2	Data Bus · STATUS.
0	0	0	HALT.
0	0	1	Memory write.
0	1	0	Memory read.
1	0	1	IO write
1	1	0	IO Read
0	1	1	Opcode fetch.
1	1	1	Interrupt acknowledge.

When microprocessor receives any interrupts signal from peripheral which are requesting its services, it stops its current execution and program control is transferred to sub-routine by generating CALL signal and after executing sub-routine control gets returned to main program.

Software interrupts

In this type of interrupt, the programmer has to add the instructions into the program to execute the interrupts. There are 8 software interrupts in 8085, ie RST0, RST1, RST3, RST4, RST5, RST6 and RST 7.

Hardware interrupts

When microprocessors receive interrupts signals through pins (hardware) of microprocessor, they are known as Hardware interrupts. There are 5 hardware interrupts in 8085 microprocessor. They are INTR, RST 7.5, RST 6.5, RST 5.5, TRAP.

Address

(I) RST 4.5 = 24H

(II) RST 5.5 = 2CH

(III) RST 6.5 = 34H

(IV) RST 7.5 = 3CH

{ vector address = 8 * Type of interrupt }

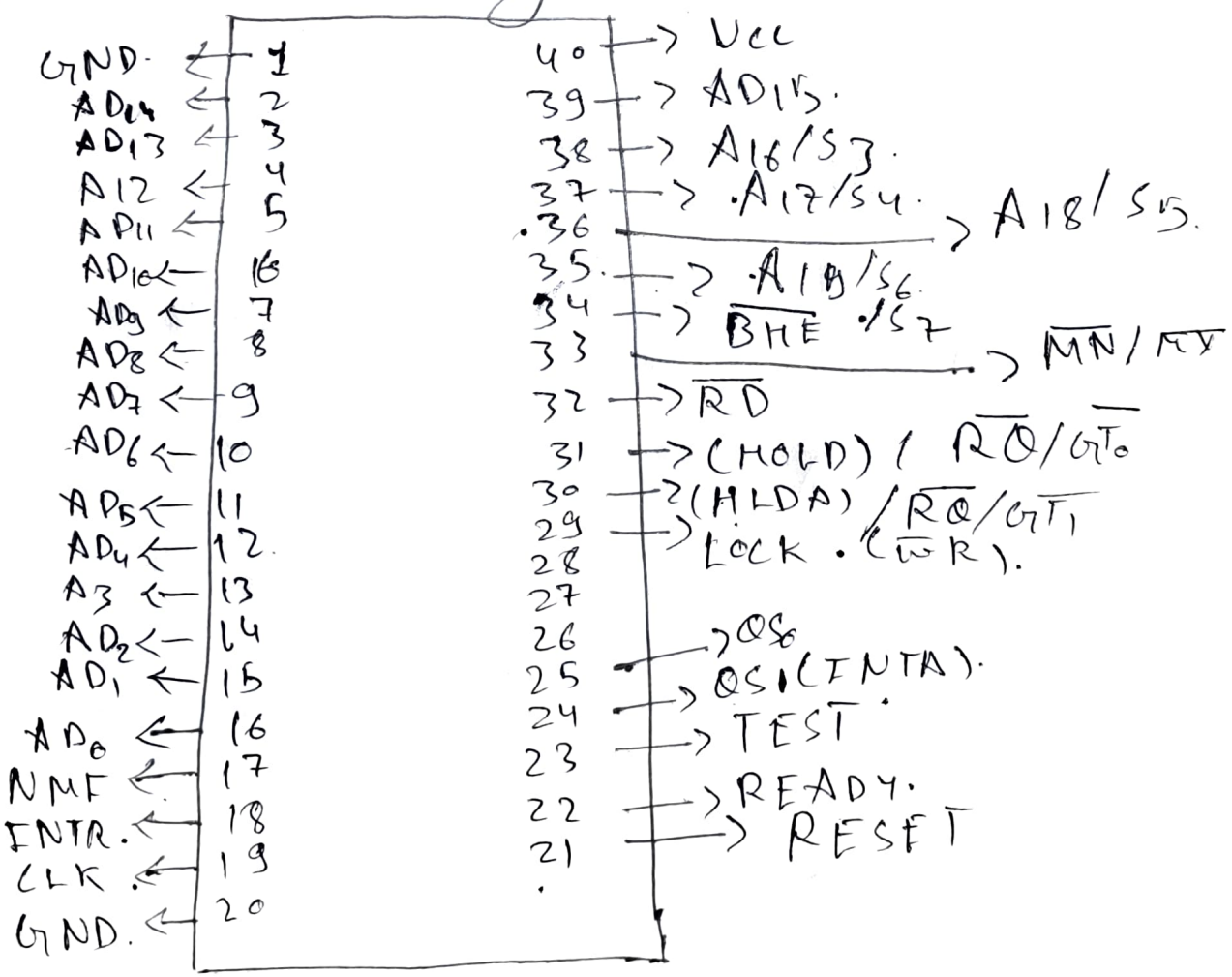
Q 3 a

Mayank Kumar
19184064/34/K

It is a 16-bit µp
8086 has a 20 bit address bus can access upto 220 Memory locations (1MB).
It can support upto 64K I/O Ports.
It provides 14, 16-bit registers
It has multiplexed address & data bus.
AD0 - AD15 & A16 - A19.
It requires Single Phase clock 33% duty cycle to provide internal timing
8086 is designed to operate in two modes Min & Max.
It can pregetches upto 6 instruction bytes from memory & queues them in order to speed up instruction execution.
It requires +5V power supply.
A 40 pin dual in line package.
8086 has two blocks BIU & EU.
The BIU performs all bus operations. The instruction bytes are transferred to inst. queue
EU executes instructions from the instruction byte queue.

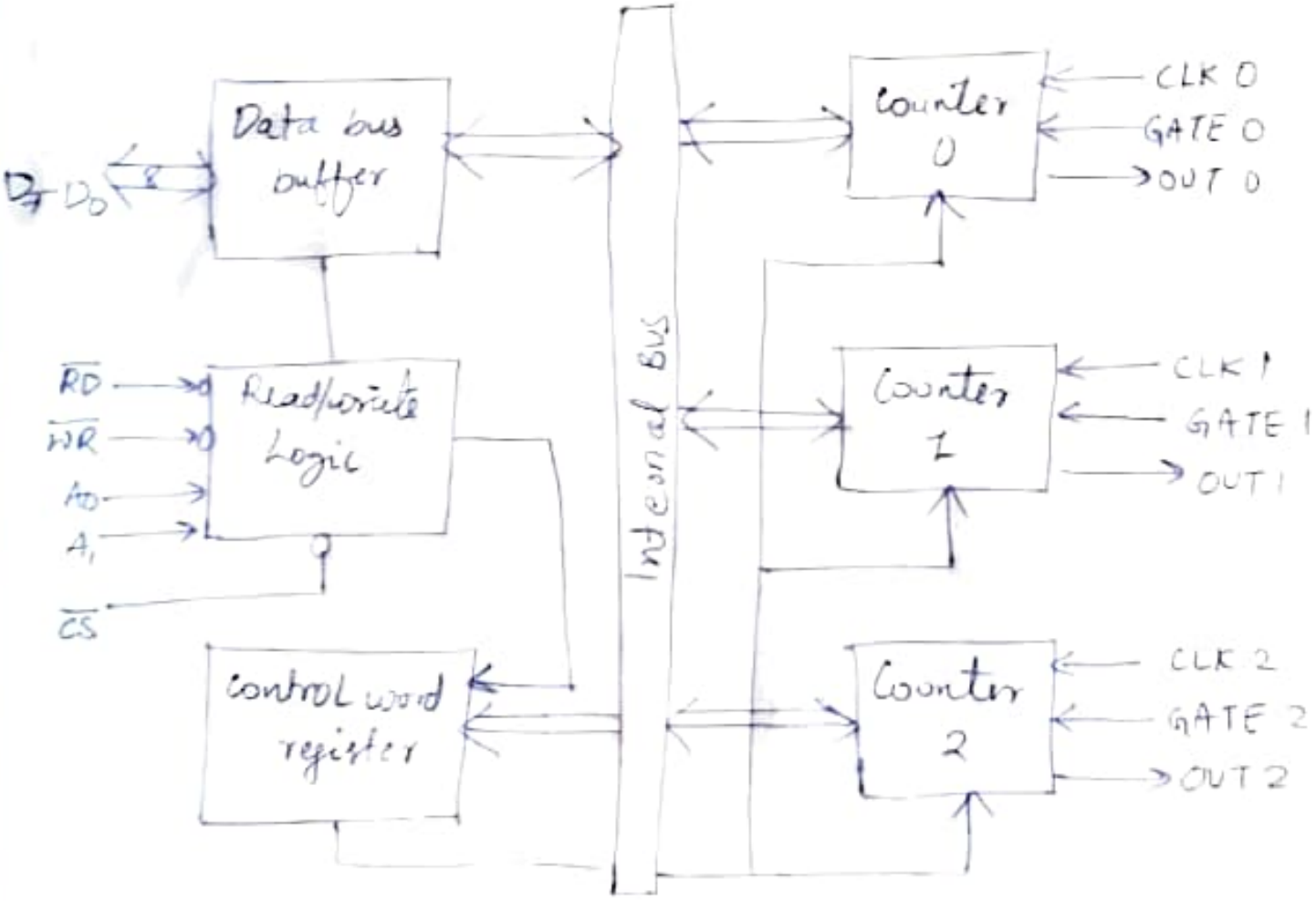
Both the units operate asynchronously to give the 8086 an overlapping instruction fetch & execution mechanism which is called as pipeling. This result in efficient use of the system bus & performance

BIU contains Instruction queue segment. register, Instruction pointer. Address adder. Fr control circuitry.



A4(b) Features of 8254:

1. 8254 is the device designed to solve the timing control problems in a microprocessor.
2. It has 3 independent counters, each capable of handling clock inputs up to 10MHz and size of each counter is 16 bit.
3. It operates in +5V regulated power supply and has 24 pin signals.
4. It has 3 counters each with two inputs (Clock and Gate) and one output.
5. The 8254 is an advanced version of 8253.



The architecture of 8254

Data Bus Buffer : It is a tri-state, bidirectional 8-bit buffer, which is used to interface the 8253/54 to the system data bus. It has 3 basic functions

- programming the modes of 8253/54
- loading the count registers
- Reading the count values

Read/Write Logic : It includes 5 signals, i.e RD, WR, CS, and the address lines A_0 & A_1. In the peripheral I/O mode, the RD and WR signals are connected to IOR and IOW, respectively.

Control Word Register : this register is accessed when lines A_0 & A_1 are at logic 1. It is used to write a command word, which specifies the counter to be used, its mode, and either a read or write operation

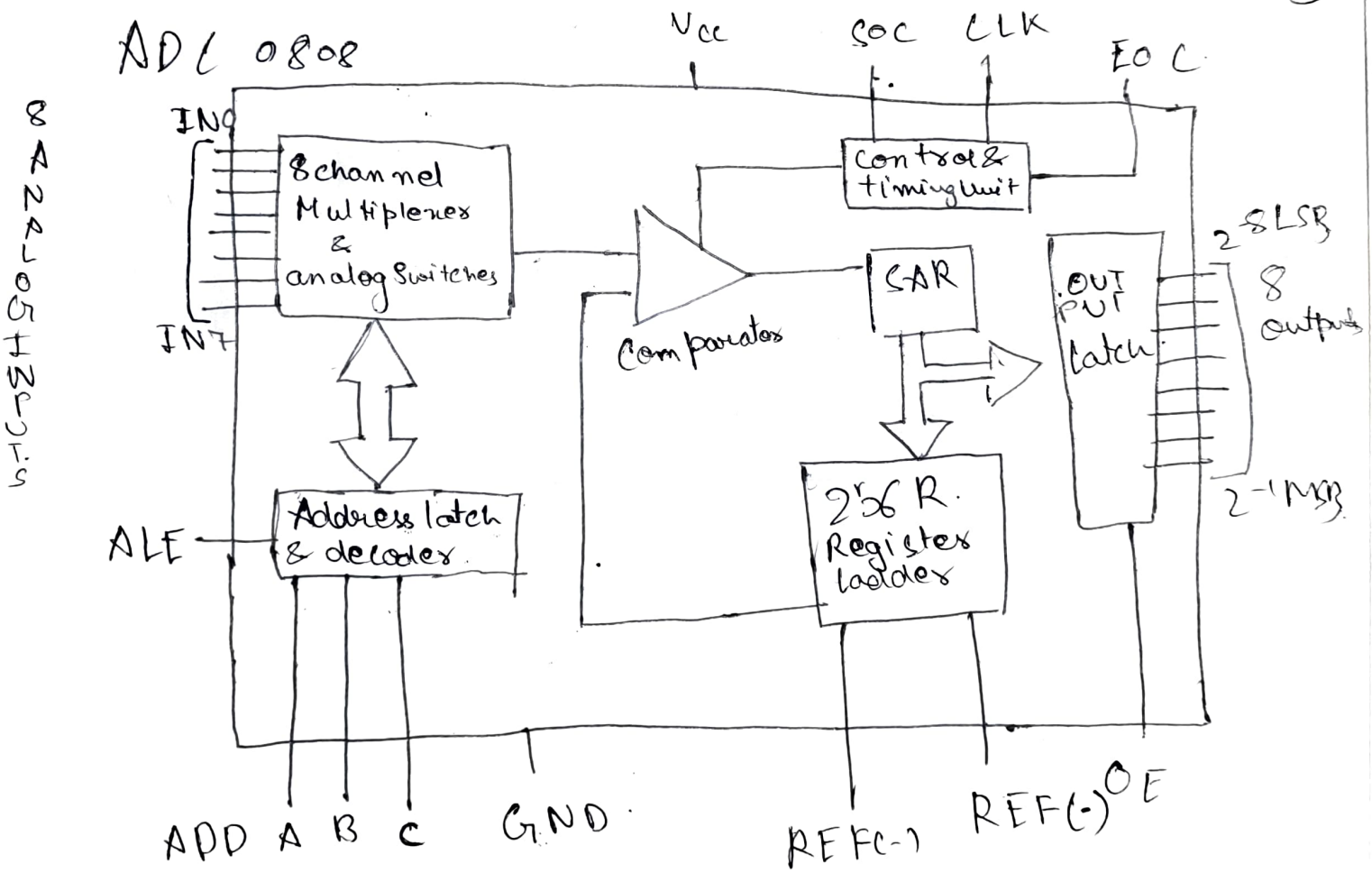
Counters : Each counter consists of a signal, 16 bit-down counter, which can be operated in either binary or BCD. Its input and output is configured by the selection of modes stored in the control word register.

The programmer can read the contents of any of the three counters without disturbing the actual count in the process.

Mayank Kumar
19184641K134
B.Tech. IV-Sem.

Name- Mayank Kumar
19164641341K.

Q.5 a An analog to digital converter is an electronic Device. As the name predicts, the supplied analog Signal is converted into a digital Signal which is produced at output. Analog Signal such as. Voice recorded into a digital Signal using an analog to digital converter.



Functional block diagram.

There are 7 pins for receiving analog inputs (1 to 5, 27, 28). Then there is START (6th pin) which is set to high to start the conversion. Then there is End of conversion (7th pin) which turns itself high once the conversion is done. Many output (2^{-1} to 2^{-7}) these give result of the ADC conversion. Vcc (11th pin) typically powers the IC.

ADD A, B, C. These 3 are used to select channel.

ALE → Temporarily made high to select channel.

Ground → to connect to ground, Vref(-) & Vref(+).

clock & OUTEN

features.

Easy to interface with all microprocessors or works stand alone.

Eight channel 8 bit ADC module.

Can measure up to 8 Analog values seamlessly.

Digital output. Varians from 0 to 255 operating

Power in 15 mW. Conversion 100 us.

Explaination

The functional blocks ADC are

8 channel multiplexer,

Comparator, 256 R. Register ladder

Switch tree.

Mayank Kumar
19181164134/K.

The 8-channel multiplexer can accept eight analog signal as input with the range of 0 to 5V and allow one by one for conversion depending on the 3-bit address input.

The successive approximation register performs eight iterations to determine the digital code for input value.

The End of Conversion (EOC) will go low b/w 0 and 8 clock pulses after the positive edge of Start Pulse.

The 256R ladder has been provided instead of conventional R/2R ladder because of its inherent monotonic, which guarantee no missing digital codes.

The comparator is a chopper-stabilized comparator. It converts the DC input signal into an AC signal, and amplifies the AC sign using high gain AC amplifier. Then converts AC to DC signal.

In ADC conversion process the input analog value is quantized analog value will have a unique binary equivalent.

Quantization Step →

$$\text{Q step} = \frac{V_{REF}}{2^8} = \frac{V_{REF}(+) - V_{REF}(-)}{256_{10}}.$$

The digital data corresponding to an analog input (V_{in}) is

$$\text{Digital data} = \left(\frac{V_{in}}{\text{Q step}} - 1\right)$$