ACHD Final Project – Phase 3

Implementation of a 32-bit processor with assembly codes (auto clock)

Deliverables:

- **1.** Assembly code for encryption.
- 2. FPGA DEMO: https://youtu.be/FaERPXxH3Xk

Team 11 | Version 3

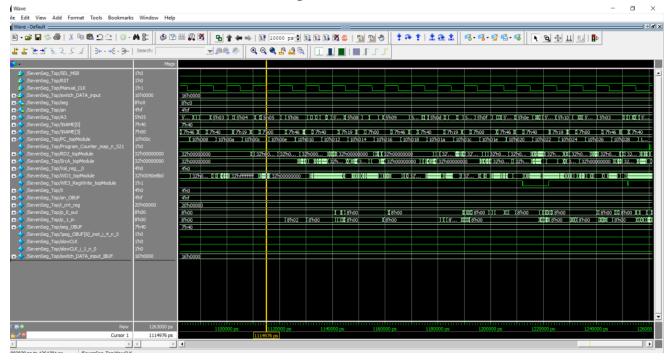
Byte Addressable 32 Bit NYU6463processor Processor

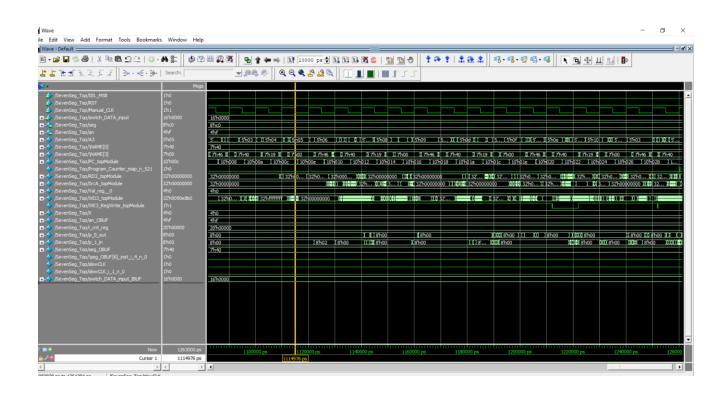
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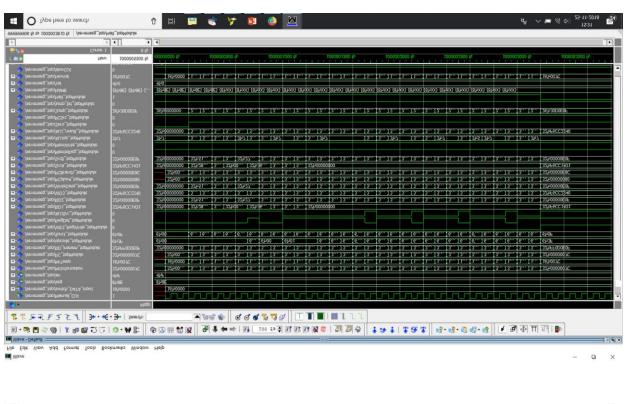
Phase III: RC5 Code Instruction explanation: please find the codes in the respective text files attached.

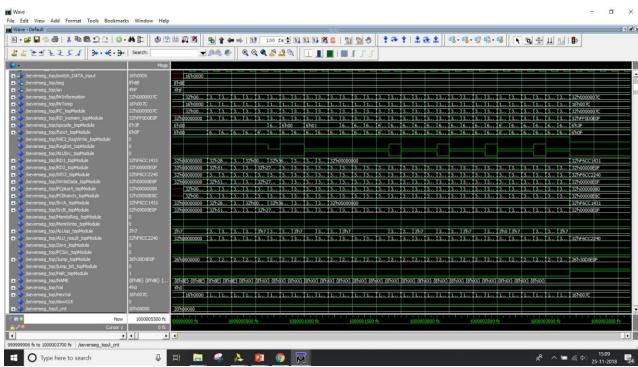
Timing Simulation





Behavioral Simulation





€ 1 •		Msgs																			
	seg_top/SEL_MS8	0																			
		0																			
	seg_top/switch_DATA_input	16h0000	16°h0000																		
■- /sevens		8"h8E	8'h8E																		
□- / /sevens		4hF	4hF																		
□-4 /sevens		16'h0000	16'h0000																		
/sevens	eg_top/Manual_CLK	1				$\overline{\Box}$											\overline{n}	$\overline{\Box}$	\overline{n}	\overline{n}	
- /sevens	ieg_top/RF_ARRAY	{32h00000000}	[{32h0] {32	H000000	{32h0	I (32h0	{) {32	110000000	[(32h0000	0] {32h	000000	I (32h0000	0) (32)	000000	{32h0	{ } {32	HO 1 (32)	0 1{	[(32h0000	00) (32	H00000
	teg top/DMEM ARRAY	{32h00000000}	(32h00000000)	(32h000000	000) (32h4	6F8E8C5	(32h460C6)	085) (32h70	F8388A) (3)	h28488303) (32h513	E1454) (32)	F621ED22	(32h31250	65D) (32h	1A83A5D)	32hD4276	368) (32h7	13AD82D}		
♦ /sevense	seg_top/branch_Out_debug_topModule	0																			
□- /sevens	seg_top/branch1_BLT_BEQ_BNE_debug	5'h02	15 15 15	I 5 I 5	5) 5	I 5 X 5	I 5 I 5	I 5 X 5	I 5 I 5	5 1 5	5 15	5 15	5 Y 5	5 X 5	5 X 5	5 I 5	15 15	5 [5	15 15h0	2 Y 5	5h05
- /sevens	eg_top/Fetched_instruction	32hFFFFFFFF	13 13 13																		3 X
□- /sevens	eg_top/RD_topModule	32h00000000	3 3 3	3 3	3 3	3 ¥3	3 3	13 X32h	00000000	3 3	3 \ 32h	00000000									3
□- /sevens	ieg_top/readAddress_out_topModule	7h00		7 7									7 \ 7	7h02	7 X 7	7 77	7 17h0	17	7 17h0	0 Y7	7Y
	eg_top/MrInformation	32h0000014C	13 13 13		3 3	3 3	3 (3		3 13					З ХЗ	З ХЗ	3 13	13 13	3 [3	3 13	3)3	3
- /sevens	eg_top/MrTemp	16'h014C	1100 (100 (100	1 (1)	1 1	11 X1	1 (1	11 (1	1 1	1 (1)	1 1	1 11	1 1	1 11	1 (1	1 11	1 11	1 1	1 11	1 11	1
- /sevens	seg_top/PC_topModule	32h0000014C	13 13 13	3 13	3 3	3 \ 3	3 (3	. (3	3 [3	3 3	3 [3	3 13	3 3	З ХЗ	з Хз	3 [3	3 13	3 [3	3 13	3)3	3
- /sevens	eg_top/RD_insmem_topModule	32hFFFFFFF	3 13 13	3 (3	3 / 3	3 \ 3	3 (3	3 (3	3 (3	3 3	3 [3	3 / 3	3 \ 3	3 (3	3 (3	3 [3	3 (3	3 (3	3 (3	3)3	3)
	seg_top/opcode_topModule	6'h3F	16 16 16																		67h00
□- /sevens	seg_top/funct_topModule	6'h3F	16 16 16		6 16				16 16h0			16 16h0			6 (6h0		16 16		16 16h0		16 X
	ieg_top/WE3_RegWrite_topModule	0																			
	eg_top/RegDst_topModule	0																			_
/sevense	ieg_top/ALUSrc_topModule	0																			
	seg_top/RD1_topModule	32h00000000	13 13 13	32h00	3 3	3 321	100 X 3	I 3 I 3	3 [32h	0 13	3 13	13 132h	0 (3	3 X 3	3 X 32h	00 I 3	13 13	32h00	32h00	3) 32h	00000
- /sevens	seg_top/RD2_topModule	32h00000000	13 13 13	3 13	3 / 3	3 X3	. I 3 I 3	I3 X3	13 13	3 [3	3 13	3 13	3 \ 3	3 X3	З ХЗ	3 13	13 13	3 [3	З ТЗ	3 X3	32h0
□- /sevens	seg_top/WD3_topModule	32h00000000	3 3 13	3 3	3 3	3 ¥3	3 3	3 X3	3 (3	3 3	3 3	3 /3	3 3	32h00	з (з	3 13	13 \ 32h	0 [3	3) 32h	00) 3	3Y
	eg_top/WriteData_topModule	32h00000000	13 13 13																		32h0
	ieg_top/PCplus4_topModule	32h00000150	3 3 3		3 3	3 73	3 (3		3 13					3 13	З ХЗ	3 13	3 13	3 13	3 13	3) 3	3 Y
	seg_top/PCBranch_topModule	32h0000014C	[3 [3 [3	3 13	3 3	3 3	3 (3	13 (3	13 13	3 13	3 13	3 13	3 3	3 13	З ХЗ	3 13	13 13	3 13	3 13	3)3	3 X
□- /sevens	ieg_top/SrcA_topModule	32h00000000	3 3 3											З УЗ	3) 32h	00 13	3 13	32h00	32h00	3) 32h	00000
□- /sevens	ieg_top/SrcB_topModule	32h00000000	13 13 13																	3 /3	
	ieg_top/MemtoReg_topModule	0																			
	ieg_top/MemWrite_topModule	0																			
	seg_top/ALUop_topModule	3'h0	[3 [3 [3	3 (3	3 (3	3 (3	3 (3h) (3	3 (3	3 [3ħ0	[3	3 (3	3 (3h0	(3	3 (3	3 (3	3 (3	3 (3	3h0	3)(3	3 (
E-100	Now	0.4802 ns	75.00	0.29	1 1		0.2985 ns		0.25			0.2995 ns			ns .	1111	0.3005 ns		0.30	1	
0.10	Cursor 1	0.00000 ns	7316	0.29	10 115		0.2985 R		0.2	9119		0.2995 NS		0	7119		0.5005 hs		0.30	V 1 110	

\$1 •		Msgs												
4	/sevenseg_top/SEL_MS8	0												
- 4	/sevenseg_top/RST	0												
B -4	/sevenseg_top/switch_DATA_input	16'h0000	16)h0000											
□ ◆		8"h8E	8'h8E											
D - 4		4hF	4hF											
		16"h0000	16h0000											
4		1												
□ -♦	/sevenseg_top/RF_ARRAY	{32h00000000}	{32h000	{32h000000000}	32h00000017} {	{32h000000000}	{32h00000017} {	. [{32h00000000	{32h000000000}	(32h0000000B) {3	2h03F6BCBF} {32	(32h00000000)	{32'h000000008} {	32H03F6BCBF}-{
	/sevenseg_top/DMEM_ARRAY	{32h00000000}	(32h00000	000) (32h0000000) (32h46F8E8C5)	(32h460C6085) (32h70F8388A) (321	128488303} (32h5	13E1454) (32hF621	D22) (32h312506	SD) (32h11A83A50) (32hD427686B)	(32h713AD82D) (32h48792F99} {
4	/sevenseg_top/branch_Out_debug_topModule	0												
0 -4	/sevenseg_top/branch1_BLT_BEQ_BNE_debug	5'h02	5h02	5h12	[5h02	5h1D	5h01	5h02	5h15	5h01	5h02	[5h1D	5h01	5h02
□ -♦		32'hFFFFFFFF	32h142	32h280F0004	32h08A\$0001	32h2C05FFE8	32h0C2F0001	32h14210001	32h280F0004	32h00310801	32h08A50001	32h2C05FFE8	32h0C2F0001	32h1421000
D-		32h00000000	32h035	32h00000000	32h00000046	32h00000046	32h00000000	32hC5460C60	32h00000000	32hC5460C60	32h00000000			32h0000004
D -4		7h00	7h17	7h00	7h05	7h05	7h01	7h08	7h01	7h08	7h04	7h04	7h01	7h05
□ -♦	/sevenseg_top/MrInformation	32h0000014C	32h000	32h00000108	32h00000110	32h00000114	32h00000100	32h00000104	32h00000108	32h0000010C	32h00000110	32h00000114	32h00000100	32h0000010
D -4	/sevenseg_top/MrTemp	16°h014C	16h0104	16h0108	16h0110	16h0114	16h0100	16h0104	16'h0108	16h0100	16h0110	16'h0114	16h0100	16h0104
□ -♦	/sevenseg_top/PC_topModule	32h0000014C	32h000	32h00000108	32h00000110	32h00000114	32h00000100	32h00000104	32h00000108	32h0000010C	32h00000110	32h00000114	32h00000100	32h0000010
0 -4	/sevenseg_top/RD_insmem_topModule	32hFFFFFFFF	32h142	32h280F0004	32h08A\$0001	32h2C05FFE8	32h0C2F0001	32h14210001	32h280F0004	32h00310801	32h08A50001	32h2C05FFE8	32h0C2F0001	32h1421000
□ -♦		6°h3F	6'h05	6h0A	6h02	6'h08	6h03	6h05	6h0A	6h00	6h02	6'h08	6h03	6h05
□ ◆	/sevenseg_top/funct_topModule	6°h3F	6h01	6h04	6h01	6h28	6h01		6h04	6h01		6h28	6h01	
- 4	/sevenseg_top/WE3_RegWrite_topModule	0												
- 4	/sevenseg_top/RegDst_topModule	0												
- 4		0												
	/sevenseg_top/RD1_topModule	32h00000000	32h000	32h00000000	32h00000006	32h00000000	32h00000017			32h00000008	32h00000005	32h00000000	32h00000008	
□ -◆	/sevenseg_top/RD2_topModule	32h00000000	32h000	32h00000000	32h00000006	32h00000005	32h00000000	32h00000017	32h00000001	32h00000000	32h00000005	32h00000004	32h00000001	32h0000000
	/sevenseg_top/WD3_topModule	32h00000000	32h000	32h00000000	32h00000005	32h00000005	32h00000001	32h00000008	32h00000001	32h00000008	32h00000004	32h00000004	32h00000001	32h0000000
□ -◆	/sevenseg_top/WriteData_topModule	32h00000000	32h000	32h00000000	32h00000006	32h00000005	32h00000000	32h00000017	32h00000001	32h00000000	32h00000005	32h00000004	32h00000001	32h0000000
	/sevenseg_top/PCplus4_topModule	32h00000150	32h000	32h0000010C	32h00000114	32h00000118	32h00000104	32h00000108	32h0000010C	32h00000110	32h00000114	32h00000118	32h00000104	32h0000010
	/sevenseg_top/PCBranch_topModule	32h0000014C	32h000	32h00000110	32h00000114	32h00000100	32h00000104	32h00000108	32h00000110	32h00000910	32h00000114	32h00000100	32h00000104	32h0000010
□ -◆		32h00000000		32h00000000		32h00000000	32h00000017		32h00000000	32h00000008	32h00000005	32h00000000	32h00000008	
		32h00000000	32h000	32h00000000	32h00000001	32h00000005	32h00000001			32h00000000	32h00000001	32h00000004	32h00000001	
-		0												
4	/sevenseg_top/MemWrite_topModule	0												
		3'h0	3h1	3h0	3h2	3h0	3h4	3h1	3h0		3h2	3'h0	3h4	3h1
E 18 4	Now	0,4802 ns	100	98 ns		982 ns		984 ns	0.2			988 ns		.299 ns