Pulse Width Modulation Generator

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***Abstract*—This document is a model and analysis of a PWM generatorwith variable duty cycle.The verilog PWM generator generates a 10MHZ PWM signal with variable duty cycle.Two buttons which are debounced are used to control the duty cycle of the PWM signal.The first push button is to increse the duty cycle by 10% and the other button is to decrease the duty cycle by 10%. It is simulated using verilog.**

***Index Terms*—Pulse code modulation(PWM),Register Transfer Level(RTL),Field Programmable Gate Array(FPGA)**

I. Introduction

In last two decades, the Pulse width modulation (PWM) techniques are extensively used for controlling the analog circuitry. In particular, it is more commonly used for controlling the power converters employed in various industrial/domestic applications. In power converters it is used for firing of power electronic devices like thyristors, InsulatedGate Bipolar Transistors (IGBTS), Metal Oxide Semiconductor Field Effect Transistors (MOSFET) etc.[1-[3]. Inverter fed AC motor drives has wide area ofdomestic/industrial application. Controlled Inverter can control both the magnitude as well as frequency of voltage and current applied to the motor. The Pulse Width Modulation(PWM) has made possible for three phase voltage levelinverter to convert DC link voltage into three phase voltages by controlling the on and off time of power electronic devices. The main parameter of PWM signal is duty cycle which is a part of PWM period [4]-[5]. The electric motors usually run at duty cycle less than 100 per-cents. Duty cycle (D) can be defined as ratio of ON time over to total ON and OFF time and is shown in Fig. 1.

$$D = \frac{Ton}{Ton + Toff} * 100 \tag{1}$$

Frequency dividers can be designed in 2 ways: analog and digital. Analog frequency dividers are rare and used only in very high frequency applications. One of the most important application of analog frequency divider was used in the development of televisions, the device was called injection-locked frequency divider. Digital frequency dividers are the most widely used frequency dividers. For the power of 2 integer division, a simple binary counter can be used, clocked by the input signal. In this case the LSB becomes 1/2 of the input signal, the next bit becomes 1/4 of the input signal, the third bit becomes 1/8 of the input signal and so on. Other division ratios can be obtained by adding logic gates to the chains of flipflops. Whereas Time period (T) is defined as sum of Ton and Toff Ton- time for which switch is on Toff – time for which witch is off

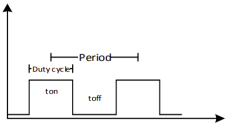

Fig. 1. Duty Cycle

The main advantage of Pulse width modulation is that it has very low power loss in switching devices and higher frequency that affects the devices which uses power. Only digital circuits can produce PWM signals. In this paper counters are used to generate PWM signals which will be in the form of square wave. The conventional method of generating the PWM pulses using analog circuitry have disadvantages of complex circuitry, limited function and low flexibility in circuit modification. Due to limitations offered by analog circuit designing, the digital methods of generating the pulses are getting more popularity.

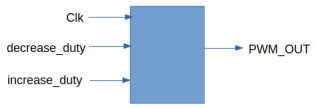

Fig. 2. Basic Block Diagram

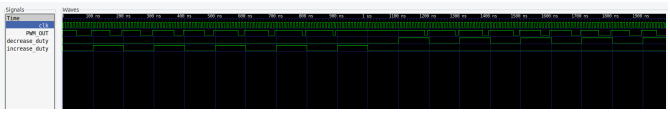

Fig. 3. Verilog simulation result

References

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