

**Repeaters Number and Size Optimization of Copper  
Interconnects with Machine Learning Techniques**

**M.Tech Thesis**

By

**Himanshu Pandey**

**2018IMT-038**



**ABV-INDIAN INSTITUTE OF INFORMATION TECHNOLOGY  
AND MANAGEMENT GWALIOR MADHYA PRADESH  
GWALIOR-474015(INDIA)**

**MAY, 2023**

**Repeaters Number and Size Optimization of Copper  
Interconnects with Machine Learning Techniques**

*A*

*thesis submitted in fulfillment for the award of the degree of*

*Integrated Post Graduate*

in

Information Technology

By

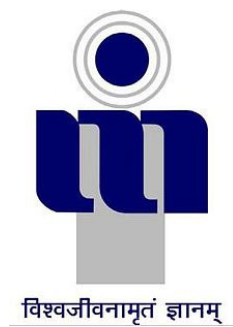
**Himanshu Pandey : 2018IMT-038**

Under the Supervision of

**Dr. Somesh Kumar**

and

**Dr. Pinku Ranjan**



ABV-INDIAN INSTITUTE OF INFORMATION TECHNOLOGY  
AND MANAGEMENT GWALIOR  
GWALIOR, INDIA



©ABV-Indian Institute of Information Technology and Management

Gwalior

All rights are reserved



# DECLARATION

I hereby certify that the work, which is being presented in the thesis, entitled **Repeaters Number and Size Optimization of Copper Interconnects with Machine Learning Techniques**, in fulfillment of the requirement for the award of the degree of Integrated Post Graduate - Master of Technology in Information Technology and submitted to the institution is an authentic record of my/our own work carried out during the period July-2022 to May-2023 under the supervision of Dr. Somesh Kumar and Dr. Pinku Ranjan. I also cited the reference about the text(s)/figure(s)/table(s) from where they have been taken.

Dated:

**Signature of the candidate**

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

Dated:

**Signature of supervisor**

Dated:

**Signature of supervisor**



# ACKNOWLEDGEMENTS

I would like to express my sincere thanks to all those people who made this thesis possible. First and foremost, I would like to express my profound respect and gratitude to my supervisor, Dr. Somesh Kumar and Dr. Pinku Ranjan, who has been guiding force behind this work. I am greatly indebted for their invaluable guidance, constant encouragement, and their valuable comments on my work. I am fortunate enough to have such advisors who gave me the freedom to think independently and explore new ideas. More importantly, I would like to thank for the patience they have shown in carefully reading and commenting on the manuscripts, and countless revisions of this dissertation. Their commitments and dedication to research have been and will continue to be a constant source of inspiration for me. I have no doubts that finishing my degree in proper and timely manner was impossible without their help. I am highly privileged to have got an opportunity to work with such wonderful persons.

I am thankful to ABV-IIITM for providing the resources to undertake my research work. Lastly, I would like to thank the Almighty God for granting me this opportunity and showering me with his blessings so that I could overcome all odds and succeed.

***Himanshu Pandey***



## Abstract

The main goal of this work is to verify the optimal number of repeaters and repeater size computed theoretically with the optimization algorithms including Particle Swarm Optimization(PSO), Random Search(RS), Ant-Lion Optimization(ALO), Bat Algorithm(BA) and Artificial Neural Networks(ANN). We have considered the global and intermediate copper interconnects for 7nm and 13nm technology nodes. In our work, we have developed models for various parameters like effective resistivity, mean free path, resistance per unit length, repeater size and optimal number of repeaters in copper interconnects.

In case of Particle Swarm Optimization algorithm we will use a time delay function. The time delay function will be a function of optimal number of repeaters( $k$ ) and repeater size ( $h$ ) and the length of the interconnect( $l$ ). In case of ANN the relation between the length, specular parameter and technology node which are taken as inputs and optimal number of repeaters and repeater size which are the outputs will be learnt using back propagation and hidden layers. In ANN the value of weight is updated using sigmoid and relu function which gives value between 0 and 1. We will see that the theoretical values well match with values obtained from PSO and ANN thereby showing that the theoretical formula is valid. The repeater size will remain constant for a given technology node even with variation of length only the optimal number of repeaters change. The insertion of repeaters in interconnects is employed to reduce the time delay and power dissipation. The figure of merit(FoM) is also calculated in our work and matched with the theoretical values. In our work, the optimal repeater designs that goal at minimum power-delay product (PDP) are performed by studying the delay and power optimal algorithms. In future, we are planning to extend our studies to the Borophene as an interconnect by deploying similar models for that and various hybrid interconnects like Cu-GNR, Cu-CNT and Cu-Graphene.

*Keywords:* Copper, Interconnect, Effective Resistivity, mean free path, optimal repeater size, Power-Delay Product(PDP), Random Search(RS), Bat Algorithm(BA), Ant Lion Optimization(ALO), repeater insertion, Time-delay, , Artificial Neural Network(ANN), Particle Swarm Optimization(PSO).



# Contents

<b>List of Figures</b>	<b>xiii</b>
<b>List of Tables</b>	<b>xv</b>
<b>List of Acronyms</b>	<b>xvi</b>
<b>1 Introduction</b>	<b>1</b>
1.1 Content . . . . .	2
1.2 Copper(Cu) Interconnects . . . . .	4
1.3 Repeaters in Interconnects . . . . .	6
1.4 Thesis Statement and Objectives . . . . .	8
1.5 Approach . . . . .	8
1.6 Thesis Outline . . . . .	10
<b>2 Background Work</b>	<b>13</b>
2.1 Literature Survey . . . . .	14
2.2 Key Related Research . . . . .	15
2.3 Review of the Key Related Research . . . . .	18
2.4 Identified Research Gaps . . . . .	23
2.5 Summary . . . . .	23
<b>3 Delay and Power Delay Product optimized number of repeaters and     repeater size for Copper Interconnects using various optimization algo-     rithms</b>	<b>25</b>
3.1 Analytical Models . . . . .	26
3.1.1 Resistivity . . . . .	26
3.1.2 Mean Free Path . . . . .	28

## Contents

---

3.1.3	Figure of Merit . . . . .	28
3.1.4	Repeaters in copper Interconnects . . . . .	29
3.2	Machine Learning Optimization Algorithms . . . . .	30
3.2.1	PSO Algorithm . . . . .	30
3.2.2	Random Search . . . . .	33
3.2.3	Bat Algorithm . . . . .	34
3.2.4	Ant Lion Optimization . . . . .	36
3.3	Results and Discussions . . . . .	38
3.3.1	Copper Interconnects . . . . .	38
3.3.2	Delay Optimized Repeaters Number and Size Dependency upon Length in Copper Interconnects . . . . .	39
3.3.3	Delay Optimized Repeaters Number and Size Dependency upon Specularity Parameter in Copper Interconnects . . . . .	40
3.3.4	Power Delay Product(PDP) Optimized Repeaters Number Depen- dency upon Length in Copper Interconnects . . . . .	43
3.3.5	Power Delay Product(PDP) Optimized Repeaters Number and Size Dependency upon Specularity Parameter in Copper Interconnects . . . . .	44
3.3.6	Analysis of the Figure of Merit and Processing Time for various Optimization Algorithms . . . . .	46
3.4	Summary . . . . .	49
<b>4</b>	<b>Artificial Neural Networks for the repeater size and number of repeaters for Cu Interconnects</b>	<b>50</b>
4.1	Artificial Neural Network . . . . .	51
4.2	Analysis of the Artificial Neural Network . . . . .	53
4.3	Summary . . . . .	55
<b>5</b>	<b>Conclusions and Future Scope</b>	<b>56</b>
5.1	Conclusion . . . . .	57
	<b>Bibliography</b>	<b>58</b>

# List of Figures

1.1	Copper Interconnects . . . . .	5
1.2	An interconnect divided into subsections using the repeaters . . . . .	7
1.3	Flowchart of the Approach . . . . .	9
3.1	Vectorial Representation of Particle Swarm Optimisation . . . . .	31
3.2	Flowchart-for-basic-PSO-algorithm . . . . .	32
3.3	Flowchart of Bat Algorithm . . . . .	35
3.4	Flowchart for Ant Lion Optimization . . . . .	37
3.5	Effective Resistivity vs Width of Interconnect . . . . .	38
3.6	Effective mean free path vs Technology node . . . . .	39
3.7	Optimal Number of Repeaters vs Length of Interconnect . . . . .	40
3.8	Optimal Number of Repeaters vs Specularity Parameter . . . . .	41
3.9	Repeaters Size vs Specularity Parameter at 7nm Technology Node . . . . .	42
3.10	Repeaters Size vs Specularity Parameter at 13nm Technology Node . . . . .	42
3.11	Optimal Number of Repeaters vs Length of Interconnect . . . . .	44
3.12	Repeaters Size vs Specularity Parameter . . . . .	45
3.13	Repeaters Number vs Specularity Parameter . . . . .	45
3.14	Figure of Merit Dependency upon Number of Iterations for various Algorithms . . . . .	47
3.15	Processing Time for various Algorithms for given Number of Iterations . . . . .	47
3.16	Figure of Merit Dependency upon Specularity Parameter for various Algorithms . . . . .	48

## List of Figures

---

3.17 Figure of Merit Dependency upon Length of Interconnect for various Algorithms . . . . .	48
4.1 Artificial Neural Network . . . . .	52
4.2 Variation in the Processing Time on increasing Number of Epochs . . . . .	54
4.3 Variation in the Mean Squared Error on increasing Number of Epoches . . . . .	54

# List of Tables

2.1	Research Review . . . . .	18
3.1	Typical Interconnect Parameters . . . . .	26
4.1	Comparative Analysis of the Results at 1000 $\mu$ m length and 13nm technology node. . . . .	55

# List of Acronyms

VLSI	Very Large Scale Integration
IC	Integrated Circuits
Cu	Copper
MFP	Mean Free Path
EMFP	Effective Mean Free Path
PSO	Particle Swarm Optimization
ANN	Artificial Neural Networks
$R_Q$	Quantum Resistance
$R_S$	Scattering Resistance
$R_C$	Contact Resistance
$E_n$	Minimum Subband Energy
$E_f$	Fermi Energy
RC	Resistive-Capacitive
FoM	Figure of Merit
BA	Bat Algorithm
RS	Random Search
ALO	Ant Lion Optimization



# 1

## Introduction

---

### 1.1 Content

Interconnections are essential to the success of VLSI (Very Large-Scale Integration) systems. The electronic paths that link various parts of a chip together are known as interconnects. These interconnections may be on- or off-chip. Off-chip interconnects are made to join together various chips, whereas on-chip interconnects are made to link components on the same chip. Transistor speeds have grown as a result of smaller device dimensions and higher component densities on the chip. However, this has resulted in an increase in connection delay and losses [1]. Conventional copper (Cu) based planar interconnects suffer from lower data-rates [2] and greater delay than is necessary to keep up with ongoing transistor scaling. Unlike scaling of transistors, scaling of interconnects results in a significant rise in time delay, which has become the major performance bottleneck in modern very large scale integration (VLSI) chip designs. Moreover, the ITRS forecasts that the current density will soon surpass the maximum ampacity of typical copper (Cu) interconnects in the near future [3].

The interconnects next to the transistors must be tiny since the transistors themselves are very small and frequently tightly packed. These lines, known as local interconnects, are typically narrow and brief in length. The global interconnects are located higher up in the structure, and they connect the various circuit blocks. Consequently, they are often long and thick. Vias provide the transmission of signals and electricity from one interconnection level to the next.

Interconnects play an essential part in the technological reduction of device size, as the smaller device size indicates a shorter transit time delay. Consequently, the entire chip performance is dependent on the link performance [4]. Currently, far-end time delay is one of the most important design criteria; therefore, it is necessary to lower the total time delays at intermediate stages. In order to eliminate temporal delays, which can lead to malfunctions and logical failures, it is best to include repeaters at intermediate stages. In the study [5], the appropriate number of repeaters and repeater size are precisely

determined and implanted in copper and graphene interconnects to eliminate time delays. The repeaters are assumed to be nonlinear CMOS inverters that are viable in the real world.

We employ an artificial neural network to automate the estimation of the ideal number and size of repeaters. In today's VLSI (very large scale integration) interconnects, artificial neural networks (ANNs) play a significant role. They are used to connect and regulate various VLSI system components, including capacitors, transistors, and resistors, and others. ANNs are used to create complicated networks and circuits that can be utilised to tackle complex issues, including optimization and learning. ANNs are made up of numerous artificial neurons, often referred to as nodes, that are connected to one another. Each neuron takes information from other neurons as input and processes it to produce an output. One neuron then transmits its output to the following one, and a signal is sent from one neuron to every other neuron in the network, an example of a feed-forward network. A supervised learning approach used to train ANNs is the backpropagation algorithm. It is a technique for reducing network error by utilising gradient descent to train the weights between neurons. The backpropagation process in an artificial neural network functions by propagating the mistake from the output layer to the input layer. A neural network's weights are changed using the backpropagation technique so that the network's neurons learn to provide the desired output. The error function's gradient with regard to the network weights is calculated to achieve this. Adjusting the weights to minimise the error function is the objective. In order for the backpropagation process to function, the mistake must first be propagated from the input layer to the output layer. Following that, the chain rule of calculus is used to propagate the error across the concealed levels.

In this study, we have used the sigmoid function and relu function. In artificial neural networks, the sigmoid function is utilised as an activation function. It is a nonlinear function that can be used to simulate complex input-output relationships. The sigmoid function "squashes" a real-valued number into the interval between 0 and 1. The sigmoid

## 1. Introduction

---

function is also known as the logistic function and can be defined as:

$$h_{\theta}(x) = \frac{1}{1 + e^{-\theta^T x}} \quad (1.1)$$

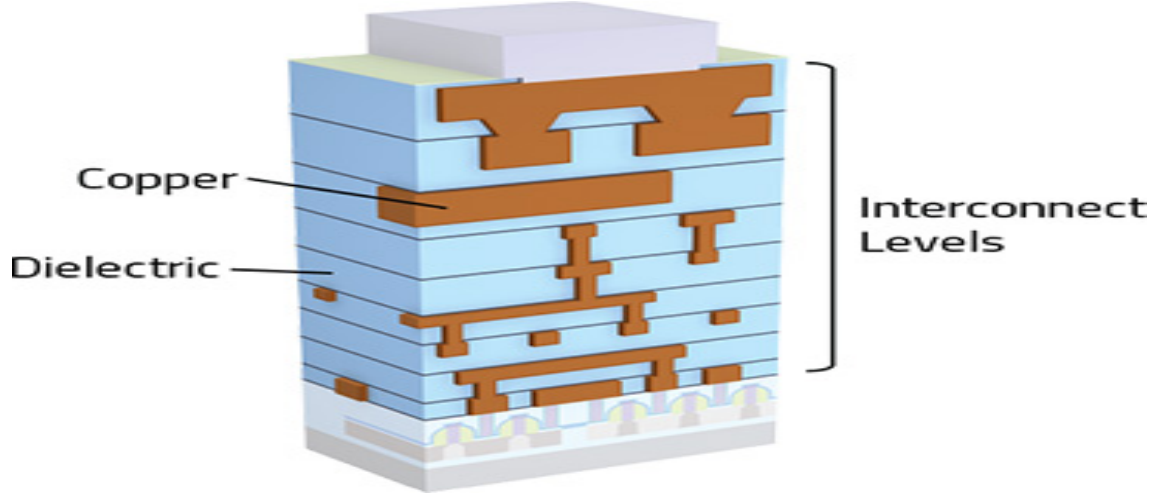
Its S-shaped form makes the sigmoid function handy for classification applications. The function accepts  $x$  as input and returns a number between 0 and 1. The output value is close to 0, and it is close to 1, depending on whether the input is positive or negative. Most frequently, the activation layer of a neural network has the sigmoid function as one of its elements. In this instance, the weighted total of the inputs from the preceding layer serves as the input to the sigmoid function. Due of these nonlinear correlations between inputs and outputs, the neural network can learn them.

## 1.2 Copper(Cu) Interconnects

One of the most often utilised materials in IC interconnects is copper. It is utilised in every facet of IC design, from transistor connections to external connections on chips and packages. Copper is an ideal material for interconnects due to its superior electrical and thermal qualities, low cost, and ease of processing. Copper's electrical characteristics make it a good connection material. Due to its low resistivity, it offers a high current carrying capacity with minimal power loss. Also, copper's resistance doesn't change much with temperature, therefore it has a low thermal coefficient of resistance. Copper is also an excellent heat conductor, which is significant in very large scale integrated circuits (VLSI) because heat dissipation is a primary concern in these circuits.

Copper interconnects were the industrial norm for decades after aluminium, which conducts electricity more efficiently. However, constructing copper interconnects is significantly more complicated, necessitating the development of an entirely new production strategy for this technological shift. The method of copper interconnection begins with the deposition of an insulating (dielectric) substance, such as silicon dioxide, followed by the formation of trenches. The copper is then added to the trenches (using electroplating and chemical processes), and the excess is scraped away to leave a flat surface for pro-

cessing.



**Figure 1.1:** Copper Interconnects [6]

The figure 1.1 represents the copper interconnects levels like intermediate interconnect and global interconnect and its schematic diagram consisting of copper and dielectric. The semiconductor industry has long relied on copper interconnects, and now they are by far the most used interconnect technology for VLSI (very large-scale integration). Copper has several advantages over other connecting materials, including improved electrical performance and cheaper production costs. Copper's resistance and capacitance are both lower than those of aluminum's, which helps boost its signal-to-noise ratio.

In recent decades, copper interconnects have become increasingly common in very large scale integration (VLSI) circuits. Due to its exceptional electrical characteristics, copper is the material of choice for many applications. Copper interconnects provide a signal route with low resistance, enabling faster and more effective communication between components. Copper interconnects are more dependable than aluminium ones due to the former material's resistance to oxidation and the latter's lower melting point. This makes them appropriate for applications requiring high speeds.

Copper interconnects are not only superior in electrical qualities, but also cheaper to produce than alternative interconnect materials. Copper interconnects are easier to

## 1. Introduction

---

work with and require less processing than other interconnect materials. This means they can be made with fewer steps and for less money. Copper interconnects are therefore an excellent option for businesses seeking a cost-effective material.

Cu is a great electrical conductor and is utilised in a variety of interconnections. However, because Cu's thickness and width have the same order of mean free path when the technology node is smaller than a few nanometers, the resistivity rises significantly. Due to the presence of a layer with high diffusivity and electron scattering, the current density is quite high, resulting in a transmission power delay. When discussing VLSI, the connector width ranges from 7nm to 45nm. When the diameters of the Cu Interconnect become smaller than the bulk mean free path of the electrons, surface scattering increases. As an alternative to copper, materials such as tungsten, silicides, carbon nanotubes, and hybrid interconnects could be used to address this issue. Despite the fact that the bulk resistivity of W and silicide films is significantly greater than that of Cu films, the shorter mean free path of the electrons will reduce the surface scattering effect. Copper's Inductance per unit length, Capacitance per unit length, and Resistance per unit length are our primary parameters. Here, we have taken into consideration technology nodes of 7nm and 13nm.

### 1.3 Repeaters in Interconnects

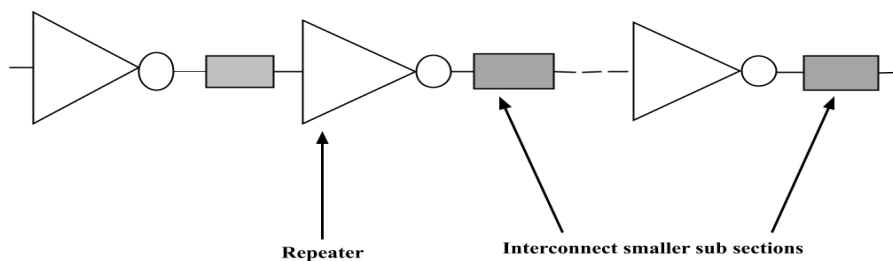
One chip can contain tens of thousands of transistors in creating a process called very large scale integration (VLSI). As the size and complexity of VLSI circuits rise, so does the importance of interconnects between the various components. Interconnects are the channels that allow communication between various circuit components. To attain optimum performance and efficiency, the connection system must be meticulously planned and enhanced.

In VLSI circuits, there are two primary types of interconnects: global and local. While local interconnects link parts inside a single logic block, global interconnects enable communication between various parts of the same device. The circuit's overall performance depends on the interconnect system's architecture, which also determines how quickly and

reliably data is transferred and how much power is used.

Several things must be considered while creating interconnections for a VLSI circuit. Distinct types of interconnects have different qualities, such as speed, power consumption, and signal integrity. The interconnects' topology, which controls the routing of signals and how they communicate with one another, is the second factor.

Very large scale integration (VLSI) circuits have two key design constraints: delay and power dissipation. These develop as a result of the chip's million of active devices and the interconnections between these components. In the past three decades, a significant technique for inserting repeaters in lengthy linkages to reduce delay in VLSI circuits has indeed been disclosed. In high performance VLSI circuits, it is necessary to reduce propagation latency and power dissipation. Since the load on VLSI circuits has increased, especially because of huge fanouts and extensive interconnects, efficient driver circuits are essential for discharging capacitances quickly enough to aid in delay minimization. Repeaters are utilised to reduce connection response time by reducing the effects of resistance and capacitance. The number of metal layers has increased due to an increase



**Figure 1.2:** An interconnect divided into subsections using the repeaters

in chip complexity. Due to this, power and clock lines in particular have become significantly longer. As the length of a connection increases, so does its parasitic resistance and capacitance, which results in significant delays in signal propagation. Consequently, the

overall latency of the VLSI circuit increases. Repeaters are ideal for driving capacitive and resistive loads with high resistance. Figure 3 depicts  $m$  repeaters installed into an interconnect that has been subdivided. Dividing the connection into smaller and smaller pieces decreases the total RC constant. To be considered, however, is the added latency caused by repeaters.

In contrast, repeater insertion was typically applied in long interconnects to reduce time delay [7], [8]. However, the delay-optimal repeater insertion method would overestimate the number of repeaters, leading to excessive power loss. To this purpose, approaches for repeater insertion that account for power dissipation have been devised [9], [10]. The figure 1.2 shows the number of repeaters inserted in an interconnect dividing it into various subsections.

### 1.4 Thesis Statement and Objectives

In our thesis, we have worked upon the Particle Swarm Optimization(PSO), Ant Lion Optimization(ALO), Random Search(RS) and Bat algorithms for the optimal repeater size and optimal number of repeaters. We have also implemented artificial neural network to validate the results obtained from the best algorithm among four. The following is my thesis statement. To solve the problem statement, the following are my objectives:

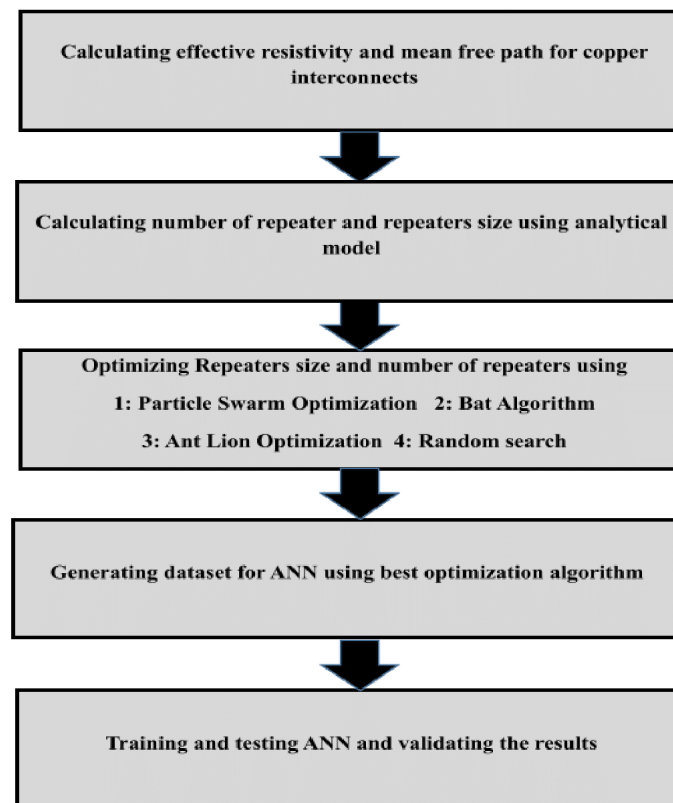
- To optimize the number of repeaters and repeaters size for copper interconnects using various optimization algorithms.
- To deploy Artificial Neural Networks to optimize the repeater size and number of repeaters and validating it with best performing optimization algorithm results.

### 1.5 Approach

Repeater insertion equations which are already available are simulated using python functions. In our thesis, we have worked upon the Particle Swarm Optimization(PSO), Ant Lion Optimization(ALO), Random Search(RS) and Bat algorithms for the optimal



repeater size and optimal number of repeaters. We have compared the results of the optimal repeater size and numbers computed analytically and from other optimization algorithms. We have produced the results for both delay optimized and power delay product optimized models. We have also implemented artificial neural network to validated the results obtained from the best optimization algorithm. The figure1.3 gives a brief idea about the approach followed in the thesis.



**Figure 1.3:** Flowchart of the Approach

### 1.6 Thesis Outline

This thesis is divided into five chapters. Let us see the content of each chapter briefly. This chapter (**Chapter-1**) is the introduction, which contains the basic information of the topic along with thesis statement, objectives and approach followed in the thesis.

In the next chapter (**Chapter-2**), we demonstrated the background work in detail. First we started with the literature survey of the field. After that we discussed the key related research done which have several research outcomes of various researchers. Further, we reviewed the contents of the key related research and organised them in tabular format. Then, we turned our focus on the most crucial part which is the research gap. We identified the research gap in the previous research done in the field of repeaters insertion in copper interconnects.

Our proposed work is documented from (**Chapter-3**) onwards; in that chapter, we describe the Analytical models which consists of resistivity, mean free path, figure of merit, optimal number of repeaters and repeaters size. Further, we started discussing about the optimization algorithms which we have implemented in our work starting from particle swarm optimization(PSO), random search(RS), bat algorithm(BA) and ending with ant lion optimization(ALO). After that we showed the results obtained for the effective resistivity and mean free path for both global and local copper interconnects. Further we presented the results obtained from the various optimization algorithms for both delay optimized and power delay product optimized repeaters number and size. After that we discussed about the performance comparison of all the implemented optimization algorithms which includes the analysis of figure of merit and processing time.

Then we move to our next chapter (**Chapter-4**), where we first discussed about the architecture of the artificial neural network which we have used and further showed the results obtained from the same. After that we also showed the performance analysis of the ANN.

In the last and final chapter (**Chapter-5**), we briefly concluded the whole work of the

thesis within a few paragraphs. We also compared the results obtained from particle swarm optimization and artificial neural network in this chapter. Later in this chapter, we also shed some light on possible improvements and future possibilities.



# 2

## Background Work

---

### 2.1 Literature Survey

Depending on the distance of signal propagation, interconnections can be categorised as either local or global. The propagation distance of a signal is largely determined by the interconnect's width and thickness, as well as the material from which it is fabricated. Local interconnects link circuit components that are very close to one another, like transistors that are only ten or so transistors' worth of distance apart from one another when they are contiguously laid out. Global interconnections can transmit over larger sub-circuits, for example. The Different Properties of Interconnects are

- Aspect ratio (AR) The Ratio of thickness to width
- ILD ratio The ratio of length to width
- Length of the Interconnect
- Pitch of the Interconnect : Sum of width and spacing

The provision of spacing enables adjacent Interconnects to be fabricated or joined without the need for conductive metal bridging. Interconnections play a significant role in signal propagation and data transmission. Any time delay or power loss will result in a weakening of the signal. Therefore, repeaters are added to interconnects to improve performance. Our primary objective is to determine the optimal number and size of repeaters for copper and hybrid interconnects. In addition, we must validate our results through the use of Particle Swarm optimization and Artificial Neural Networks. To reduce signal propagation's expense and lag time, it is necessary to develop an optimal layout. The obtained theoretical formula is an experimentally validated formula with multiple correction factors. Formula derivation is not part of the project. There are numerous genetic algorithms, including the Ant colony optimization algorithm and others. Notably, the optimal repeater size is the same regardless of the length of a given interconnect. Variable is the optimal number of repeaters.

## 2.2 Key Related Research

In the paper [11], optimal repeater designs for Cu, SWCNT bundle, and MWCNT nanointerconnects are presented. Also discussed is the viability of the ML NN in optimal repeater designs of Cu and CNT-based nanointerconnects. The width of global interconnect can range from several tens of nanometers to one micrometre, as predicted by ITRS. This article presents the optimised FoMs for Cu and CNT interconnects at the 14 nm and 7 nm technology nodes. Here, the resistance of imperfect contact is set to zero. It is demonstrated that CNT interconnects are superior to their Cu counterparts in terms of performance. It is demonstrated that MWCNT requires a small number of repeaters, reducing power consumption and giving it a performance advantage over Cu and SWCNT bundle interconnects.

The paper [12], presented a comparative analysis of repeater insertion designs in horizontal and vertical graphene nanoribbon (GNR) interconnects. Using the particle swarm optimization algorithm, the optimal numbers and sizes of repeaters are calculated, and then the results are used to train back-propagation neural networks. Using trained neural networks, the optimal repeater designs for GNR interconnects can be conducted rapidly. They proposed that the optimal repeater design method is more adaptable and flexible than conventional analytical techniques. Using the proposed method, they discovered that vertical GNR interconnects require fewer repeaters and achieve superior performance compared to their horizontal counterparts.

The authors of the paper [13] observed that the resistivity of rough on-chip interconnects increases while the mean free path decreases significantly when compared to smooth lines. In the analysis, current and future technology nodes, namely 45 nm, 22 nm, 13 nm, and 7 nm, were considered. The analytical models were validated against industry-standard field solvers (Ansys Q3D Extractor) and historical data available in the literature, both of which demonstrate excellent precision. The paper illustrates how the critical dimensions affect the effective resistivity of Cu interconnect lines.

## 2. Background Work

---

Copper-carbon (Cu-carbon) hybrid interconnects are proposed for the first time in the paper [14]. The copper-carbon nanotube composite interconnect is encapsulated by graphene barrier layers. Atomistic simulations indicate that the Cu-Carbon hybrid structure is more conductive than its parent structures, namely the Cu-CNT composite and the Cu-GNR hybrid. This is supported by simulation results demonstrating that the Cu-Carbon hybrid interconnect has the lowest delay among all alternatives.

In the article [15], By taking into account a fixed configuration that includes a CMOS driver, a bundled SWCNT interconnect system, and an ideal number of repeaters, a novel and extremely accurate finite-difference time-domain model is created for bundled single-walled carbon nanotube (SWCNT) interconnects. Using the superposition theorem, this iterative model is used to calculate the total closed-loop delay for the entire chain of repeaters. A precise transfer function is modelled for the interconnect system's chain of equispaced repeaters. The best number of repeaters is used as a dependent parameter in an analytical model for closed-loop delay that is further developed using the transfer function. In addition, an analysis is performed to determine the optimal number of repeaters for a given interconnect length in order to determine the minimum delay. In addition, a comprehensive study is conducted to determine the effect of interconnect length on time delay, the effect of increasing the number of repeaters on time delay reduction, and the effect of excitation magnitude with power delay product on time delay. Using SWCNT interconnects reduces the total number of repeaters and time delay by more than 40 and 50 percent, respectively, when compared to copper (Cu) interconnects.

Current-mode (CM) and voltage-mode (VM) nano-interconnect repeater designs are compared and contrasted in the paper. [16] The contact resistance is properly considered and studied for both Cu and carbon nanotube (CNT) nano-interconnects. The electrical performance of CM nano-interconnects is superior to that of VM ones, and they require fewer repeaters, freeing up more space on the chip. For instance, using a CM signalling scheme can cut down on the number of repeaters needed for delay-optimal multi-walled CNT interconnects by as much as 120 percent.



In the paper [17], the authors proposed a particle swarm optimisation (PSO)-based optimal repeater number for carbon nanotube (CNT) interconnects of varying lengths at 20 nm and 14 nm technology nodes. Initially, numerical equations for optimal repeaters were utilised to create a model. The PSO was trained using a variety of input parameters. We determined the optimal number of repeaters and propagation delay for CNT interconnects with lengths ranging from 500 to 2000 m. The results of numerical and PSO methods are compared and found to be within 2% of one another. In CNT interconnects, inverters based on CNTFETs (carbon nanotube field effect transistors) were used for the first time as repeaters, despite similar findings in prior research. They conducted the analysis for both  $h = 50$  and  $h = 75$  repeater sizes.

The goal of the paper [18] is to create an equivalent single-conductor (ESC) transmission-line (TL) model for the analysis of Cu-graphene interconnects, which are made of Cu wires encased in graphene barriers. Examining and evaluating the electrical performance of Cu-graphene interconnects using the ESC TL model. By using graphene barriers in place of the traditional diffusion barriers in the Cu/low-k interconnect, we show that both the delay time and the temperature rise can be reduced.

The authors of the paper [19] have looked into the possibility of optimising delay by inserting repeaters in folded graphene nanoribbon (FGNR) interconnect systems at various nanometer technology nodes. Modeling the mean free path as a function of the GNR width and Fermi energy. Models of the RLC equivalent circuit are used to analyse delay and power for global interconnections. Multiple graphene nanoribbons are stacked in either a horizontal or vertical orientation, and their performance is compared to that of FGNR. Results from their study demonstrate that the proposed FGNR interconnect with fully diffusive edges can achieve higher performance than the ML-HG NR and ML-VG NR interconnects, as well as traditional Cu interconnects, by significantly lowering the required number of repeaters.

### 2.3 Review of the Key Related Research

**Table 2.1:** Research Review

S.No.	Paper Name	Description	Limitations
1.	Wen-Sheng Zhao, Peng-Wei Liu, Huan Yu, Yue Hu, Gaofeng Wang, Madhavan Swaminathan "Repeater Insertion to Reduce Delay and Power in Copper and Carbon Nanotube-Based Nanointerconnects" <i>IEEE Access</i> , vol. 7(2019)	In this paper, optimal repeater designs for Cu, SWCNT bundle, and MWCNT nanointerconnects are presented. Also discussed is the viability of the ML NN in optimal repeater designs of Cu and CNT-based nanointerconnects.	In practical applications, it is only possible to obtain the circuit parameters experimentally for a specific foundry process at a specific technology node.

2.	Wen Li, Wen-Sheng Zhao, Peng-Wei Liu, Jing Wang, Gaofeng Wang "Optimal repeater insertion for horizontal and vertical graphene nanoribbon interconnects" <i>International Journal of Numerical Modelling: Electronic Networks, Devices and Fields</i> 33.2 (2020)	This paper presents a comparative analysis of repeater insertion designs in horizontal and vertical graphene nanoribbon (GNR) interconnects.	The system is implemented in a limited test area.
3.	Somesh Kumar and Rohit Sharma "Analytical Model for Resistivity and Mean Free Path in On-Chip Interconnects with Rough Surfaces" <i>IEEE Transactions on Emerging Topics in Computing</i> 6.2(2016)	This paper presents a novel analytical model for calculating resistivity and mean free path for on-chip copper interconnects with rough surfaces.	This paper only deals with resistivity and mean free path with not taking into consideration the role of repeaters.

## 2. Background Work

---

4.	Bhawana Kumari, Rahul Kumar, Rohit Sharma, AND Manodipan Sahoo”Design, Modeling and Analysis of Cu-Carbon Hybrid Interconnects” <i>IEEE Access</i> 9 (2021)	(Cu-carbon) hybrid interconnects are a newly proposed interconnection structure where copper-carbon nanotube composite interconnects are encapsulated by graphene barrier layers.	This paper deals with hybrid interconnects models and lack in single element’s study.
5.	C. Venkataiah, K. Satyaprasad, T. Jayachandra Prasad”Insertion of an Optimal Number of Repeaters in Pipelined Nano-ICs for Transient Delay Minimization” <i>Circuits, Systems, and Signal Processing</i> 38 (2019)	This paper demonstrates that a longer interconnect length is the cause of delay during the transient period, and that the optimal number of repeaters is the solution.	This paper deals with optimal number of repeaters only in delay optimized model not involving the power optimized models.

6.	<p>Peng-Wei Liu, Wen-Sheng Zhao, Da-Wei Wang, Jing Wang, Yue Hu, Gaofeng Wang "Optimal repeater insertion for nano-interconnects in current-mode signalling scheme" <i>Micro &amp; Nano Letters</i> 15.5 (2020)</p>	<p>In this study, the optimal repeater design for CM nano-interconnects was determined and compared to that of their VM counterparts. In addition, it was demonstrated that the optimal number of repeaters in the CM nano-interconnect is insensitive to the variation in weight of the power dissipation in FoM.</p>	<p>This paper only deals with CM and Vm counterparts of the nanointerconnects not dealing with the mean free path of the interconnect material.</p>
7.	<p>P. Uma Sathyakam, Shubham Raj, A. Karthikeyan and P. S. Mallick" A PSO based optimal repeater insertion technique for carbon nanotube interconnects" <i>International Journal of Electronics Letters</i> 10.3 (2022)</p>	<p>In this paper, the authors propose a particle swarm optimisation (PSO)-based optimal repeater number for carbon nanotube (CNT) interconnects of varying lengths at 20 nm and 14 nm technology nodes.</p>	<p>This paper discusses the optimal number of repeaters in CNT only at two technology nodes and lacks in the study of GNR and Cu.</p>

## 2. Background Work

---

8.	Zi-Han Cheng, Wen-Sheng Zhao, Da-Wei Wang, Jing Wang, Linxi Dong, Gaofeng Wang, and Wen-Yan Yin”Analysis of Cu-Graphene Interconnects” <i>IEEE Access</i> 6(2018)	The purpose of this paper is to develop an equivalent single-conductor (ESC) transmission-line (TL) model for analysis of Cu-graphene interconnects, i.e. Cu wires encapsulated with graphene barriers.	This paper only deals with single conductor transmission line and lacks in the study of multi conductor transmission line.
9.	Debaprasad Das”Delay optimization using repeater insertion in folded graphene nanoribbon interconnect systems” <i>International Journal of Numerical Modelling: Electronic Networks, Devices and Fields</i> 34.4 (2021)	In this paper, the authors explore the optimization of delay using repeater insertion in folded graphene nanoribbon (FGNR) interconnect systems for various nanometer technology nodes. Modeling the mean free path as a function of the GNR width and Fermi energy.	This paper focuses only on the delay optimization of the GNR but do not include the power optimization methods.

## **2.4 Identified Research Gaps**

In the past years, a series of research in the area of interconnects and repeater insertion in interconnects have happened. In order to evaluate any parameters in the interconnects, we first need to find the effective resistivity and effective mean free path of the material of interconnect. Various analytical models have been developed for the same and verified equations for these parameters have already been designed in case of Copper Interconnects. To calculate effective resistivity and effective mean free path, a number of manual calculations are needed. To overcome the same issue, we have developed various machine learning models to predict the effective resistivity and mean free path at a given technology node.

Apart from this, Repeaters are utilised to reduce connection response time by reducing the effects of resistance and capacitance. Our study focuses on the research done in the field of repeater insertion. Repeater insertion equations have already been deployed and optimization algorithms for the same have been developed. In our study we have worked upon the Particle Swarm Optimization(PSO), Ant Lion Optimization(ALO), Random Search(RS) and Bat algorithms for the optimal repeater size and optimal number of repeaters. We have also implemented artificial neural network to validate the results obtained from the best algorithm among four.

## **2.5 Summary**

In this chapter, we have discussed about repeaters in copper interconnects and how machine learning algorithms can be used to optimize the number of repeaters and repeaters size in copper interconnects. We have done the research analysis of the number of repeaters and repeaters size and the key related research that has been done in this field recently.





# 3

**Delay and Power Delay Product  
optimized number of repeaters and  
repeater size for Copper  
Interconnects using various  
optimization algorithms**

---

### 3. Delay and Power Delay Product optimized number of repeaters and repeater size for Copper Interconnects using various optimization algorithms

---

**Table 3.1:** Typical Interconnect Parameters

Technology Node(in nm)	On-Chip Interconnects			
	Local		Global	
	13 nm	7 nm	13 nm	7 nm
Parameters(in nm)				
Pitch ( $w + s$ )	27	13	40	20
Width ( $w$ )	13	7	20	10
Thickness ( $t$ )	26	15.4	46.8	24
Aspect Ratio (AR) (no unit)	2.0	2.20	2.34	2.40
Spacing ( $s$ )	14	6	20	10
Height from ground ( $h$ )	27	12	148.5	20
Dielectric $\varepsilon_r$ (no unit)	2.15	1.65	2.9	1.65

## 3.1 Analytical Models

The first step required to establish a research in this area is to note down the typical interconnect dimensions as per ITRS projections which are given in 3.1. Width of line is  $w$ , thickness is  $t$ , height from the reference ground is  $h$ , and spacing between the two interconnect lines is  $s$ .

After this we require all the equations related to effective resistivity and mean free path for copper interconnets followed by formulas for optimal number of repeaters and repeater size.

### 3.1.1 Resistivity

Based on the Fuchs-Sondheimer model and the Mayadas-Shatzkes model, the effective resistivity of the nanoscale Cu interconnects depending on the bulk resistivity of copper( $\rho_{bulk}$ ) can be calculated using the given equations:

$$\rho_{upper/lower} = \rho_{bulk} \left[ 1 - \frac{3}{4(t/\lambda_0)} \int_0^1 dq (q - q^3) \times \frac{2(-p_1 p_2 e^{-(t/q\lambda_0)})(1 - e^{-(t/q\lambda_0)}) - (p_1 + p_2)(1 - e^{-(t/q\lambda_0)})^2}{(1 - p_1 p_2 e^{-2(t/q\lambda_0)})} \right]^{-1} \quad (3.1)$$

where  $\rho_{upper/lower}$  is the resistivity considering scattering only on upper and lower surfaces,  $t$  is the interconnect thickness,  $p_1$  and  $p_2$  are the speculariry parameters,  $q$  is the constant

depending upon scattering angle( $\theta$ ) given by  $q=\cos \theta$ .

$$\rho_{sidewall} = \rho_{bulk} \left[ 1 - \frac{3}{4(w/\lambda_0)} \int_0^1 dq (q - q^3) \times \frac{2(-p_3 p_4 e^{-(w/q\lambda_0)})(1 - e^{-(w/q\lambda_0)}) - (p_3 + p_4)(1 - e^{-(w/q\lambda_0)})^2}{(1 - p_3 p_4 e^{-2(w/q\lambda_0)})} \right]^{-1} \quad (3.2)$$

where  $\rho_{sidewall}$  is the resistivity considering scattering only on sidewall surfaces,  $w$  is the interconnect width,  $p_3$  and  $p_4$  are the specularly parameters.

$$\rho_g = \frac{\rho_{bulk}}{3} \left[ \frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \times \ln\left(1 + \frac{1}{\alpha}\right) \right]^{-1} \quad (3.3)$$

with

$$\alpha = \frac{\lambda_0 R_g}{d(1 - R_g)} \quad (3.4)$$

where  $\rho_g$  is the resistivity of copper interconnect considering grain boundary scattering,  $\lambda_0$  is the mean free path of Copper(Cu),  $R_g$  is the reflection coefficient at grain boundaries and  $d$  is the average grain size.

The total effective resistivity of Copper is given by:

$$\rho_s = [\rho_{bulk} + (\rho_{upper/lower} - \rho_{bulk}) + (\rho_{sidewall} - \rho_{bulk}) + (\rho_g - \rho_{bulk})] \quad (3.5)$$

Based on the Fuchs-Sondheimer model and the Mayadas- Shatzkes model, the effective resistivity of the nanoscale Cu interconnects can be given as when sidewall scattering and layer scattering is not taken into consideration:

$$\rho_{Cu} = \rho_0 \left\{ \frac{1/3}{1/3 - \alpha/2 + \alpha^2 - \alpha^3 \ln(1 + 1/\alpha)} + \frac{3}{8} C (1 - p) \frac{1 + AR}{AR} \frac{\lambda_0}{W_{Cu}} \right\} \quad (3.6)$$

with,

$C=1.2$  and  $\alpha$  is same as given in the equation 3.4.

where  $\rho_0 = 2.04\mu\Omega \text{ cm}$  is the bulk resistivity,  $p_{Cu}=0.41$  is the specularly parameter of the Cu surface,  $R_g=0.22$  is reflectivity coefficient at grain boundaries,  $\lambda_0=37.3 \text{ nm}$  is

### 3. Delay and Power Delay Product optimized number of repeaters and repeater size for Copper Interconnects using various optimization algorithms

---

the Cu mean free path (MFP),  $d_g$  is the average distance between grain boundaries, and  $AR = H_{Cu}/W_{Cu}$  is the aspect ratio which is set as  $W_{Cu}$ . Then, the p.u.l resistance of the nanoscale Cu interconnect is calculated by  $R_{pul} = \rho_{cu}/W_{cu}H_{cu}$ .  $C_{pul}$  is set as 149.4pF/ $\mu$ m and 120.3pF/ $\mu$ m at the 14 nm and 7 nm technology nodes, respectively. Accordingly, the p.u.l. inductance can be calculated by  $L_{pul} = \mu_0\epsilon_0\epsilon_r/C_{pul}$ .

#### 3.1.2 Mean Free Path

The effective mean free path of copper can be calculated using the equation 3.7 given below:

$$\lambda_{Cu} = 3\lambda_0 \times \left[ \frac{1}{3} - \frac{\beta}{2} + \beta^2 - \beta^3 \times \ln\left(1 + \frac{1}{\beta}\right) \right] \quad (3.7)$$

with

$$\beta = \frac{\lambda_0 R_f}{D_g(1 - R_f)} \quad (3.8)$$

where  $\lambda_{Cu}$  is the effective mean free path of copper interconnect,  $\lambda_0$  is the mean free path of Copper(Cu),  $R_f$  is the reflection coefficient.

#### 3.1.3 Figure of Merit

The interconnect is divided into k segments, and each segment has a length of  $l/k$ . The repeaters are h times the minimum size, with the driver resistance  $R_{d0}/h$ , driver capacitance  $hC_{d0}$ , and load capacitance  $hC_{l0}$ . The 50% time delay of one segment can be calculated by

$$T_s = (1.48\xi + e^{-2.9\xi}1.35) \sqrt{L_{pul} \frac{l}{k} \left( C_{pul} \frac{l}{k} + hC_{l0} \right)} \quad (3.9)$$

with,

$$\xi = \frac{R_t}{2} \sqrt{\frac{C_{pul}}{L_{pul}}} \frac{R_T + C_T + R_T C_T (1 + C_{d0}/C_{l0}) + 0.5}{\sqrt{1 + C_T}} \quad (3.10)$$

Where  $R_T = R_{d0}/(hR_t)$ ,  $C_T = h_{C_{l0}}/C_0$ ,  $R_t = R_{pul}/k + 2R_c$ , and  $C_t = C_{pul}l/k$ . The total time delay is  $T_{total} = kT_s$ . The energy dissipation  $P_s$  consumed by one segment can be approximated as

$$P_s = \left( C_{pul} \frac{l}{k} + h(C_{d0} + C_{l0}) \right) V_{dd}^2 \quad (3.11)$$

The total power dissipation can be calculated by  $P_{total} = kP_s$ . The figure-of-merit (FoM) for global interconnect with repeater insertion has the following property:

$$F = (P_{total})^p \cdot (T_{total})^q \quad (3.12)$$

where  $p$  and  $q$  are weighting factors that can be tuned accordingly. For delay- and power-optimal repeater designs,  $p, q$  are 0, 1 and 1, 0, respectively. For simplicity, we have set both  $p$  and  $q$  as 1 in this study.

### 3.1.4 Repeaters in copper Interconnects

The number of repeaters can be calculated using the formula given in the equation 3.13:

$$n_{opt} = Inter \left[ \sqrt{\frac{R_t C_t}{2R_{d0}(R_{d0} + C_{l0})}} \frac{1}{[1 + 0.21(T_{L/R})^3]^{0.28}} \right] \quad (3.13)$$

where  $n_{opt}$  is the optimal number of repeaters,  $R_t$  is the resistance per unit length,  $C_t$  is the capacitance per unit length,  $R_{d0}$  is the driver resistance,  $C_{l0}$  is the driver capacitance and  $T_{L/R}$  is the time delay function given in the equation 3.15.

The repeater size can be calculated by using the equation 3.14:

$$h_{opt} = \sqrt{\frac{R_{d0} C_t}{R_t C_{l0}}} \frac{1}{[1 + 0.18(T_{L/R})^3]^{0.26}} \quad (3.14)$$

### 3. Delay and Power Delay Product optimized number of repeaters and repeater size for Copper Interconnects using various optimization algorithms

---

with

$$T_{L/R} = \sqrt{\frac{L_{pul}}{R_{pul}[R_{d0}(C_{d0} + C_{l0})]}} \quad (3.15)$$

where  $h_{opt}$  is the optimal repeater size.

## 3.2 Machine Learning Optimization Algorithms

### 3.2.1 PSO Algorithm

The Particle Swarm Optimization Algorithm is a population-based stochastic algorithm that was inspired by the social behaviour of fish and birds. In the case of birds, they form a flock, and everyone follows the bird that is closest to the food particle. The term optimization refers to the process of discovering the optimal solution by maximising the use of available resources. In this context, optimization may refer to locating the minimum or maximum of a problem. Every particle in the swarm represents a solution to the problem at hand. The swarm continues to migrate until the optimal solution is discovered, which in this case is maxiter, or the maximum number of iterations to be performed. The Particle Swarm Optimization Algorithm can be used to determine the minimum or maximum value of a function for a specified range of variable values. In the repeater design, we will see that the time delay function concept is used to determine the optimal number of repeaters and repeater size. In each iteration, the best solution for each individual particle is computed, and from these best solutions, the optimal solution to the problem is derived. At any instant time  $t$  the velocity and position of Swarm is given by the equations 3.16 and 3.17 :

$$V_i = [V_{i1}, V_{i2}, V_{i3}, \dots, V_{im}]^T \quad (3.16)$$

$$X_i = [X_{i1}, X_{i2}, X_{i3}, \dots, X_{im}]^T \quad (3.17)$$

The personal best and global best are given by the equations 3.18 and 3.19 :

$$p_{best}(t) = [p_{i1}, p_{i2}, p_{i3}, \dots, p_{im}]^T \quad (3.18)$$

$$g_{best}(t) = [g_{i1}, g_{i2}, g_{i3}, \dots, g_{im}]^T \quad (3.19)$$

The update formulas for all particles in the search space can be expressed as given in the eqautions 3.20 and 3.21:

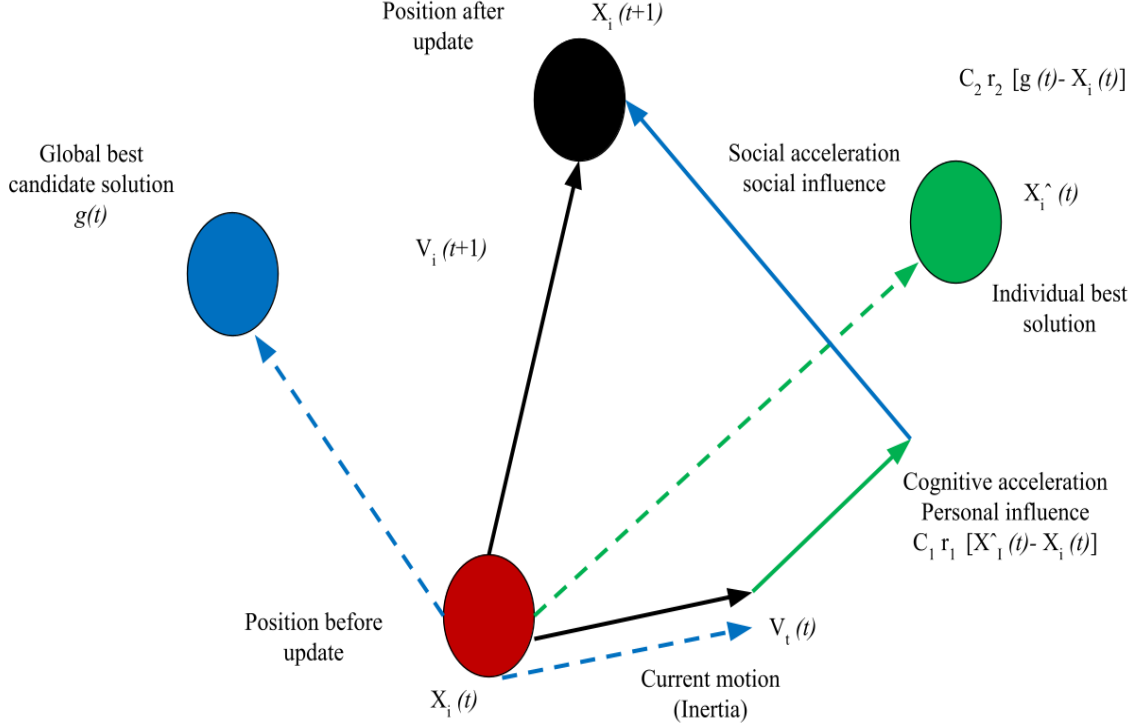
$$V_{i+1}(t+1) = W_{ei}V_i(t) + c_1r_1(p_{besti}(t)/X_i(t)) + c_2r_2(g_{best}(t)/Xi(t)) \quad (3.20)$$

$$X_{i+1}(t+1) = X_i(t) + V_{i+1}(t+1) \quad (3.21)$$

where  $W_{ei}$  is the weight inertia factor calculated using the eqaution 3.22:

$$W_{ei} = W_{maximum} - (W_{minimum} - W_{minimum}).iter/maxiter \quad (3.22)$$

$c_1$  and  $c_2$  are inertia and cognitive constant. The figure 3.1 depicts the vectorial representation of the particle swarm optimisation. It also gives us a clear view how the particle velocity and particle position is updated in various iterations.



**Figure 3.1:** Vectorial Representation of Particle Swarm Optimisation

The figure 3.2 shows the working of particle swarm optimisation using a flowchart.

### 3. Delay and Power Delay Product optimized number of repeaters and repeater size for Copper Interconnects using various optimization algorithms

---

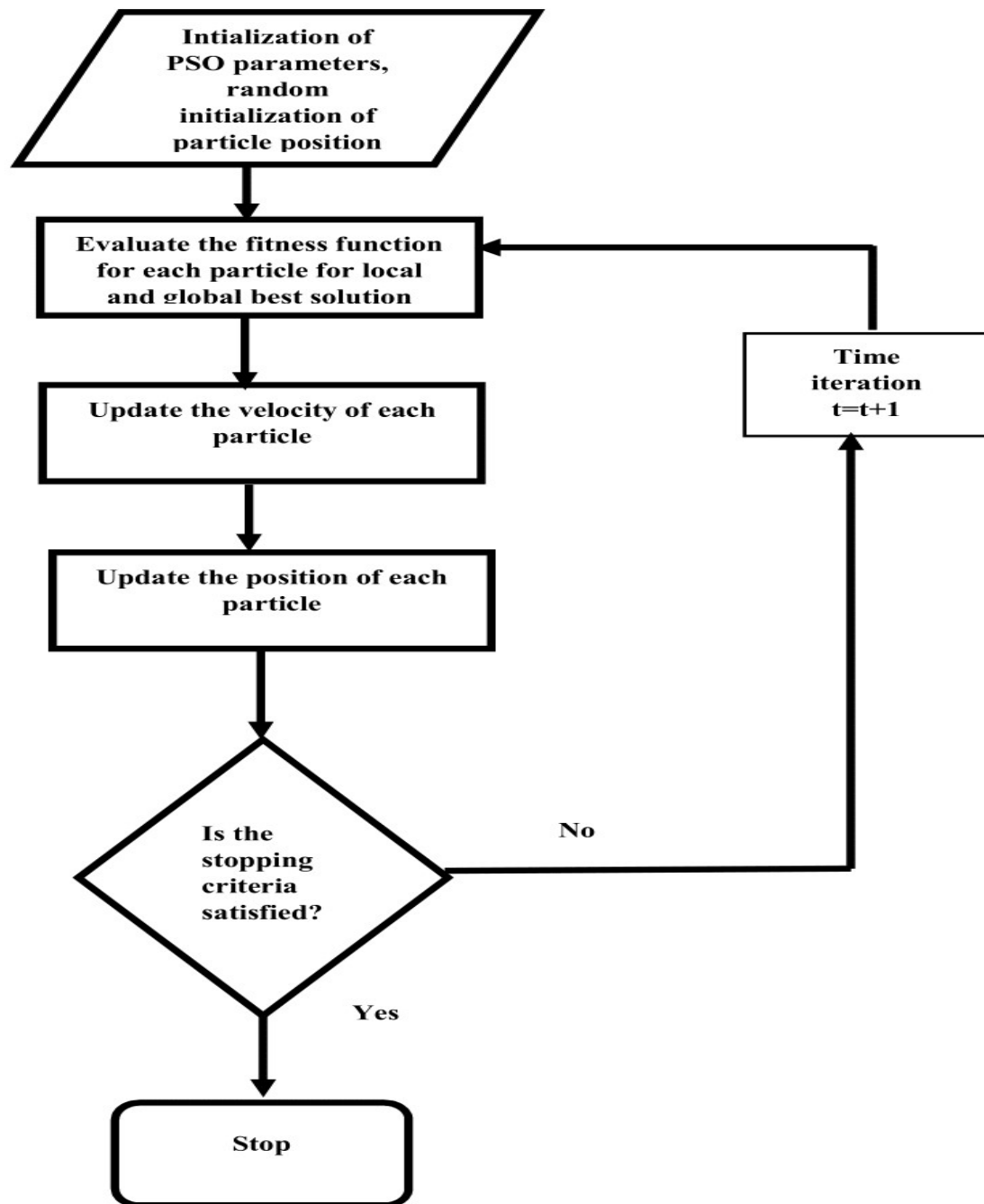


Figure 3.2: Flowchart-for-basic-PSO-algorithm



### 3.2.2 Random Search

Random search algorithm is an effective optimization algorithm that can be used to find the optimal solution of a problem within a given search space. The algorithm randomly generates candidate solutions, evaluates them using an objective function, and selects the best solution found so far. The algorithm repeats this process for a fixed number of iterations or until a convergence criterion is met. The performance of a model is strongly dependent on the values of its hyperparameters, therefore selecting the proper ones is critical for successful results.

Random search selects a set of hyperparameters at random from a predetermined search space and evaluates the model's performance with those hyperparameters. This procedure is done a number of times, and the optimal collection of hyperparameters is chosen based on the model's performance metric (such as accuracy or loss). Random search has the benefit of investigating a larger range of hyperparameters and being less computationally costly when compared to other hyperparameter tuning strategies such as grid search.

Let  $f : R^n \implies R$  denote the fitness or cost function to be minimised. Let  $x \in R^n$  represent a search-space position or potential solution. The fundamental RS algorithm is thus as follows:

- Set  $x$  to a random place in the search space.
- Repeat until a termination requirement is fulfilled (e.g., number of iterations executed or appropriate fitness reached):
  - Take a new location  $y$  from the hypersphere with a radius of a set radius surrounding the existing point  $x$ .
  - If  $f(y) < f(x)$ , then set  $x = y$  to the new location.

### **3.2.3 Bat Algorithm**

The bat algorithm is a metaheuristic optimisation technique that was inspired by bat echolocation. Bats produce ultrasonic waves and listen for echoes to identify and capture their prey during the hunting process. The algorithm is divided into four stages: startup, echolocation, movement, and updating.

Bat Algorithm:

---

---

```
Initialize the bat population  $x_i$  and  $v_i$  ( $i = 1, 2, \dots, n$ )

Initialize frequencies  $f_i$ , pulse rates  $r_i$  and the loudness  $A_i$ 

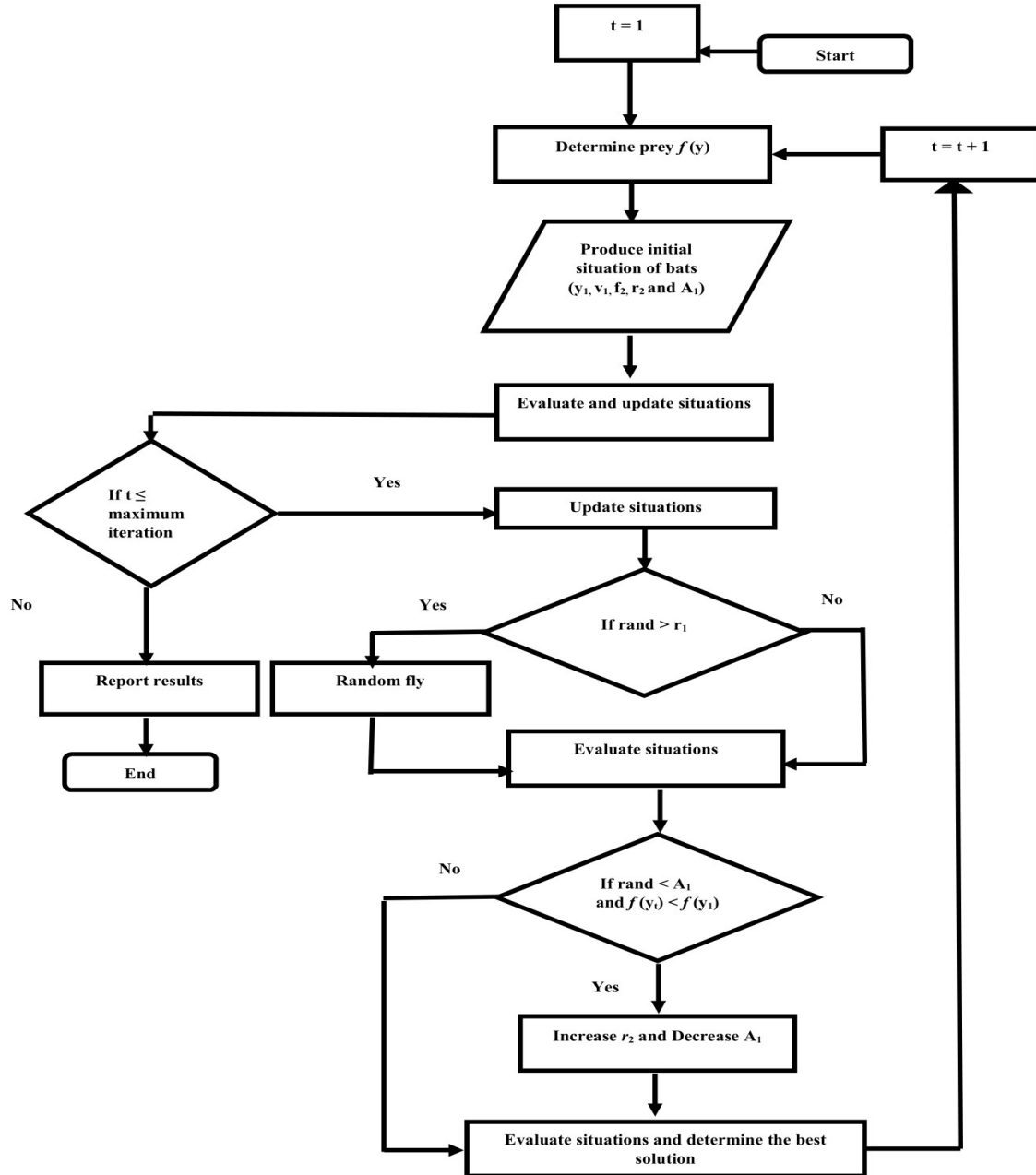
while ( $t < \text{Max number of iterations}$ ) do
    Generate new solutions by adjusting frequency
    Update velocities and locations/solutions
    if ( $\text{rand} > r_i$ ) then
        Select a solution among the best solutions
        Generate a local solution around the selected best solution
        Generate a new solution by flying randomly

    if ( $\text{rand} < A_i \& f(x_i) < f(x)$ ) then
        Accept the new solutions
        Increase  $r_i$  and reduce  $A_i$ 
    Rank the bats and find the current best  $x$ 
```

---

The method begins by populating a population of bats, with each bat represented as a vector of d-dimensional location and velocity, as well as a frequency and a loudness. A bat's location illustrates one possible solution to the optimisation issue. Each bat generates an ultrasonic wave pulse during each algorithm iteration, which is utilised to seek the solution space. The frequency and loudness of the pulse are modified based on the best answer identified thus far, and the algorithm replicates the pulse's echo to find the next best option. The new position of a bat is then updated depending on the pulse's echo. The algorithm also replicates bat movement by adjusting the velocity of a bat based on its current position and the best answer determined thus far. This movement is random, but it promotes the best solutions. Based on the quality of the solution, the algorithm then changes the frequency and volume of the bat. The Bat Algorithm iterates through the

search process, narrowing the search space in pursuit of optimal solutions. The method terminates when a stopping requirement, such as a maximum number of iterations or a specified degree of convergence, is fulfilled. The figure 3.3 shows the working of Bat Algorithm using a flowchart.



**Figure 3.3:** Flowchart of Bat Algorithm

### **3.2.4 Ant Lion Optimization**

Ant lion optimisation (ALO) is a metaheuristic algorithm inspired by the hunting behaviour of ant lions, which are insects that capture and prey on ants in sand pits. ALO was introduced in 2013 by Seyedali Mirjalili, a computational intelligence researcher.

The ALO algorithm begins with a population of ant lion agents, each representing a potential solution to the optimisation issue. The agents travel around the search space and interact with one another according to a set of rules inspired on the behaviour of ant lions and ants. Each ant lion agent travels randomly throughout the movement phase, with a preference for places with higher fitness values. Based on the optimisation issue being solved, the fitness function evaluates the quality of a solution.

During the trapping phase, the ant lion agents set traps in the search area in order to capture prey (i.e., potential solutions). The traps are represented in the search space as a cone-shaped area, and the size and form of the cone are determined by the fitness of the ant lion agent.

The prey collected in the traps are evaluated for fitness during the updating phase, and the ant lion agents change their locations and fitness values based on the fitness of the caught prey.

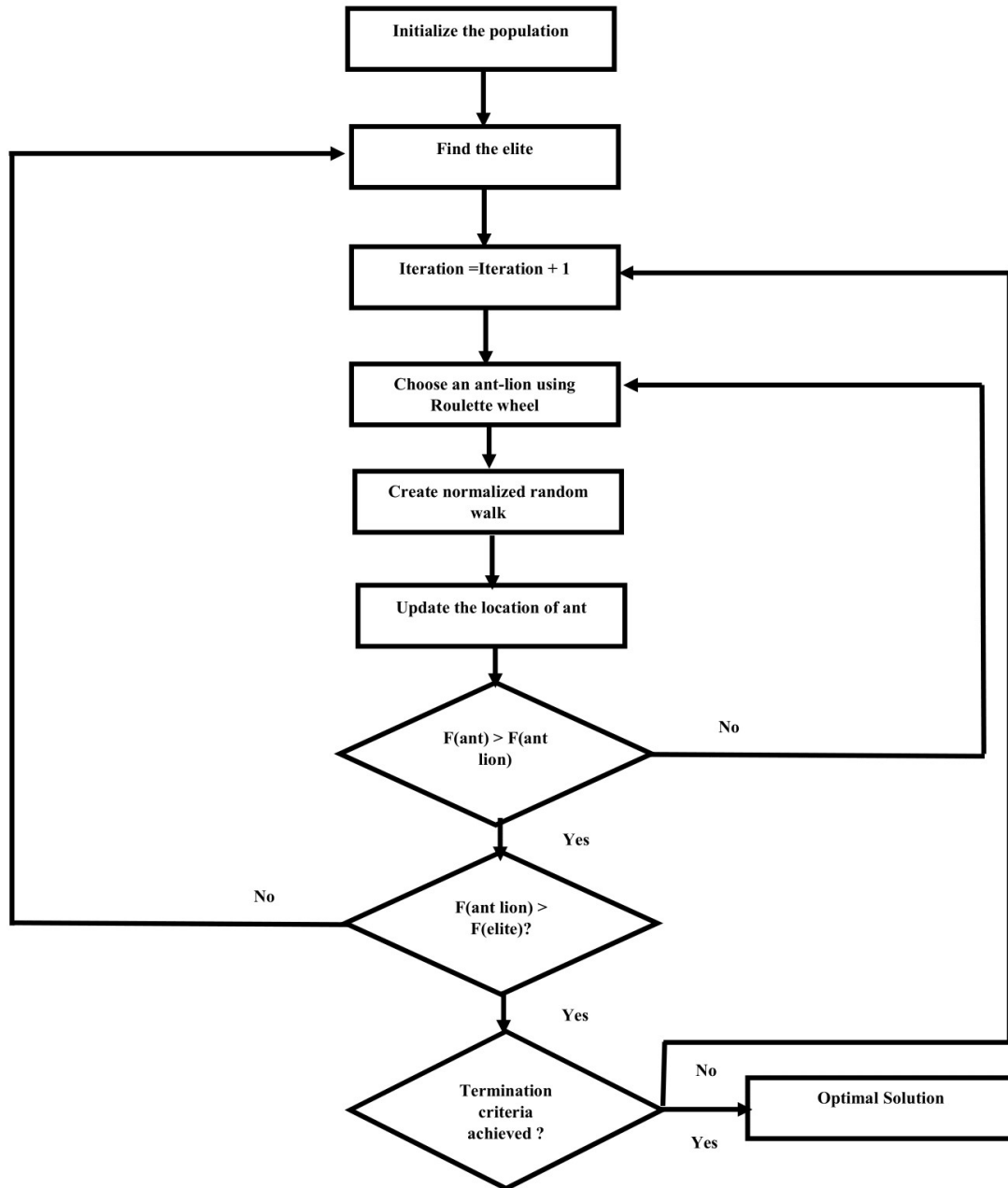
As they walk between antlion traps, we score them using a fitness function. Ants navigate the world using a stochastic strategy. We employ a random walk. The ants' mission is to dodge the antlions. The following equation is used to calculate an ant's random walk:

$$X(t) = [0, cumsum(2r(t_1) - 1), cumsum(2r(t_1) - 1), ..., cumsum(2r(t_n) - 1)]$$

$$r(t) = \begin{cases} 1 & rand > 0.5 \\ 0 & rand \leq 0.5 \end{cases}$$

where cumsum is the cumulative sum, n is the maximum number of iterations, t is the random walk step (iteration in this case), r(t) is a stochastic function, and rand is a

random integer produced with a uniform distribution in the interval  $[0, 1]$ . The figure 3.4 shows the working of Ant Lion Optimization using a flowchart.



**Figure 3.4:** Flowchart for Ant Lion Optimization

### 3.3 Results and Discussions

We have designed the mathematical functions in python to determine the effective resistivity, mean free path for copper interconnects for both global and intermediate levels. Alongwith this, we have designed functions for the time delay equation and implemented the Particle Swarm Optimization, Bat, Ant Lion Optimization and Random Search algorithm to optimize the number of repeaters and repeater size in copper interconnects.

#### 3.3.1 Copper Interconnects

We have designed the graphs in International System Of Units(SI units) and calculated the effective resistivity varying with width of the interconnect in global as well as local interconnects shown in figure 3.5. The figure clearly depicts that on increasing the width of the interconnect, the effective resistivity of the interconnect decreases in both global and local interconnects. We have also designed the graphs in International System Of Units(SI

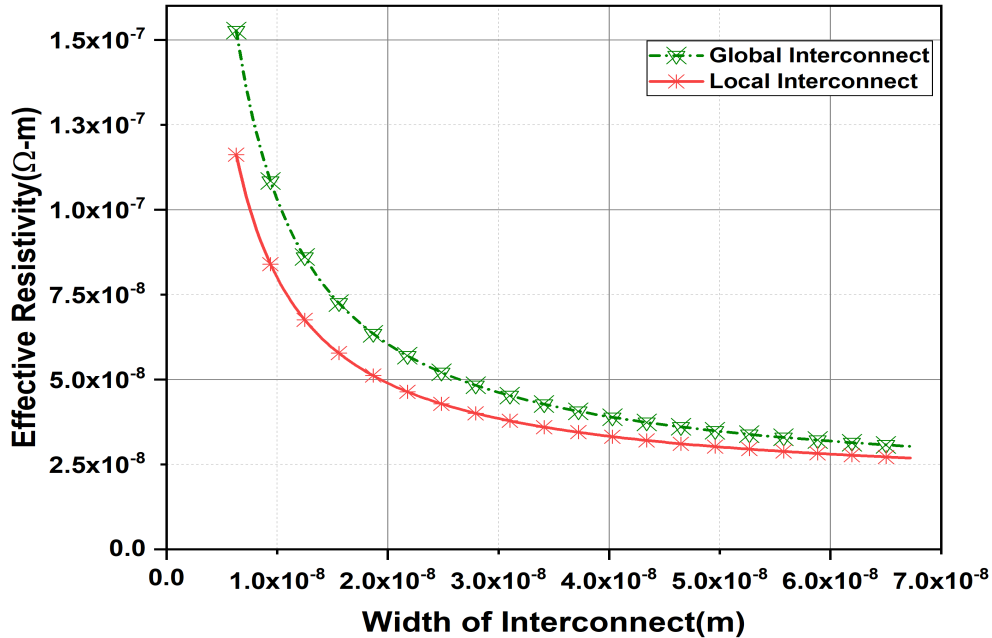


Figure 3.5: Effective Resistivity vs Width of Interconnect

units) and calculated the effective mean free path varying at different technology node

in local/intermediate and global interconnects which is shown in figure 3.6. It is clear from the shown graphs that the effective mean free path increases with the increase in the technology node. Also the value of effective mean free path for global interconnect is more than that of local interconnect for same technology node. For our study, we have plotted the values of effective mean free path at 7nm, 13nm, 22nm and 45nm technology nodes.

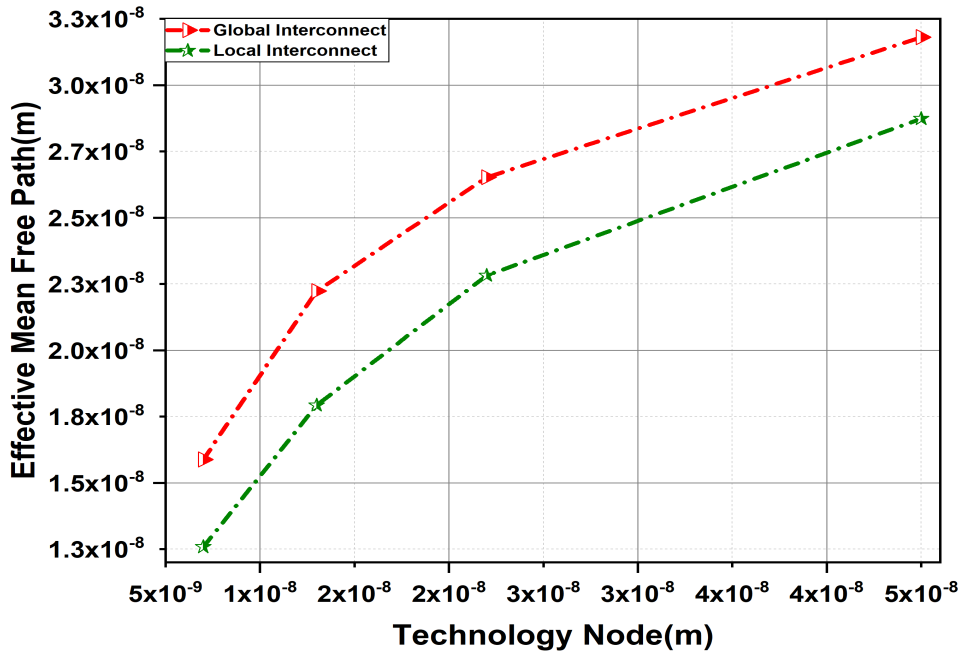


Figure 3.6: Effective mean free path vs Technology node

### 3.3.2 Delay Optimized Repeaters Number and Size Dependency upon Length in Copper Interconnects

The number of repeaters required in a copper interconnect system depends on the length of the interconnect. As the length of the interconnect increases, the signal attenuation and delay also increase, leading to a decrease in signal quality. Therefore, more repeaters are required to maintain the signal quality and to improve the performance of the system. The figure3.7 depicts the variation of the optimal number of repeaters when

### 3. Delay and Power Delay Product optimized number of repeaters and repeater size for Copper Interconnects using various optimization algorithms

---

calculated using the formula available and using various optimization algorithms like particle swarm optimization, bat algorithm, random search and ant lion optimization at 7 and 13nm technology node.

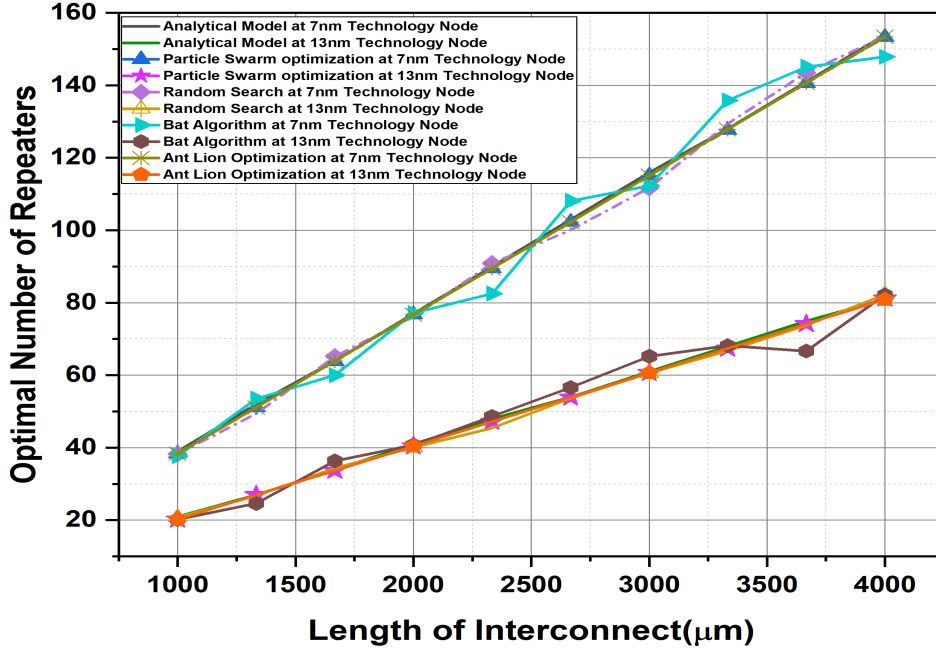


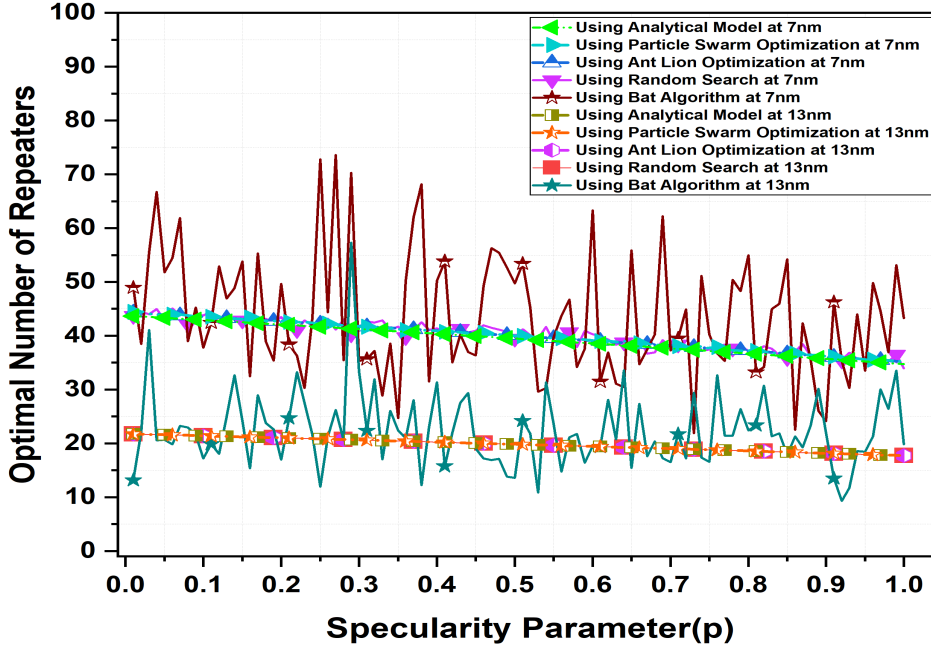
Figure 3.7: Optimal Number of Repeaters vs Length of Interconnect

#### 3.3.3 Delay Optimized Repeaters Number and Size Dependency upon Specularity Parameter in Copper Interconnects

The number of repeaters required in a copper interconnect system depends upon the specularity parameter which is denoted by 'p' in the equation of copper resistivity. Due to the change in 'p', the value of resistance per unit length changes due to which both the repeaters size and number of repeaters changes. The figure3.8 show the variation in the optimal number of repeaters on varying the value of specularity parameter for all the four optimization algorithms namely particle swarm optimization, bat algorithm, ant lion optimization and random sear. It can be easily observed from the graph that optimal number of repeaters required decreases on increasing specularity parameter. It is clearly



visible that the PSO and ALO both converges at both technology nodes at given values of the parameters while the other two algorithms could not produce expected results on one or the other technology node.



**Figure 3.8:** Optimal Number of Repeaters vs Specularity Parameter

The figure3.9 shows the findings of the repeater size on varying specularity parameter using Particle Swarm Optimization(PSO), Bat Algorithm(BA), Ant Lion Optimization(ALO), and Random Search(RS) algorithms at 7nm technology node. It is clearly visible that the PSO, ALO and RS all converges at 7nm technology node at given values of the parameters while the bat algorithm could not produce expected results. Repeater size increases with increasing specularity parameter. The figure3.10 shows the results of the number of repeaters size on varying specularity parameter using Particle Swarm Optimization(PSO), Bat Algorithm(BA), Ant Lion Optimization(ALO), and Random Search(RS) algorithms at 13nm technology node. It is clearly visible that the PSO, ALO and RS all converges at 13nm technology nodes at given values of the parameters while the bat algorithm could not produce expected results.

### 3. Delay and Power Delay Product optimized number of repeaters and repeater size for Copper Interconnects using various optimization algorithms

---

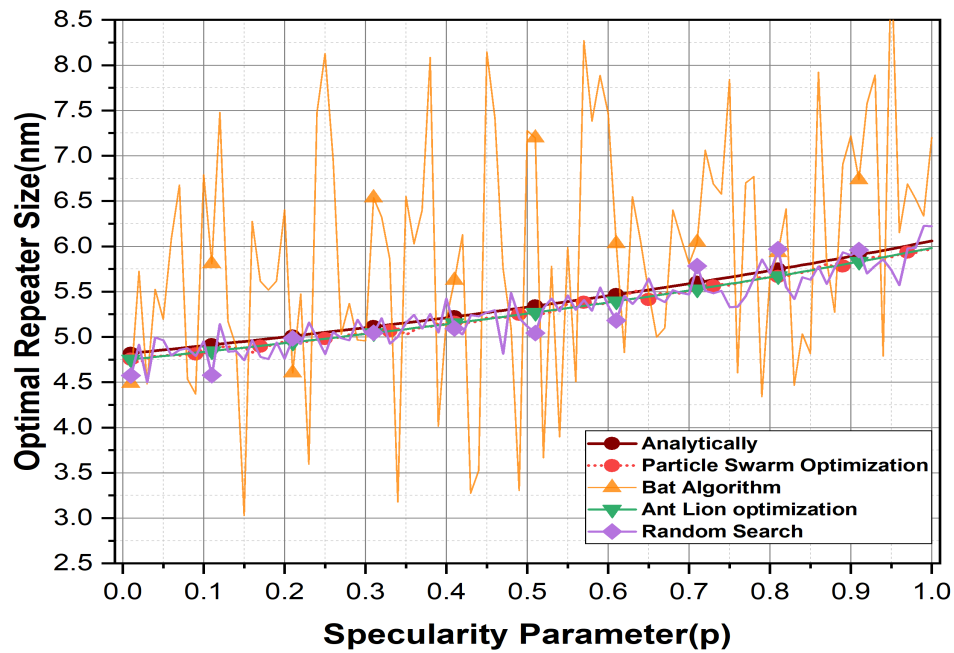


Figure 3.9: Repeaters Size vs Specularity Parameter at 7nm Technology Node

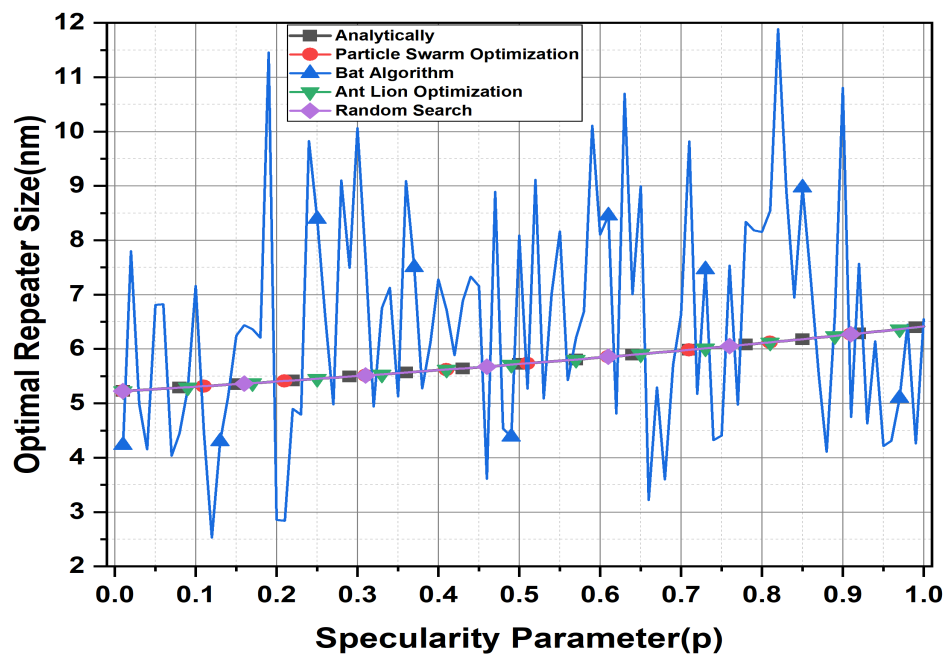


Figure 3.10: Repeaters Size vs Specularity Parameter at 13nm Technology Node

On the basis of the above findings, we can infer that the bat algorithm is not producing the results as per expectation in the delay optimized model. So, we can't use it for producing the dataset for the neural network. Only PSO and ALO both have shown their capability to converge for both the repeaters size and repeaters number when varied on length and specularly parameter.

### **3.3.4 Power Delay Product(PDP) Optimized Repeater Number Dependency upon Length in Copper Interconnects**

The number of repeaters required in a copper interconnect system depends on the length of the interconnect in PDP model as well. As the length of the interconnect increases, the signal attenuation and delay also increase, leading to a decrease in signal quality but the required number of repeaters are less than delay optimized at the same length. The values for the analytically calculated remains the same which we already shown in the delay optimized model.

The figure3.11 shows the results of optimal number of repeaters obtained from the Particle Swarm Optimization(PSO), Random Search(RS), Bat Algorithm(BA), and Ant Lion Optimization(ALO) algorithms on varying length of the interconnect. ALO and PSO both converges on the given values of parameters to find optimal number of repeaters matching with the analytical values. Random Search also approaches to the desired values but bat algorithm fails to converge here for both technology nodes.

During calculation of these values, we use the Figure of Merit formula to develop power delay product function to optimize the values of repeater size and repeaters number. For calculating the same, we require the voltage value which we have taken as 1V in our calculations.

### 3. Delay and Power Delay Product optimized number of repeaters and repeater size for Copper Interconnects using various optimization algorithms

---

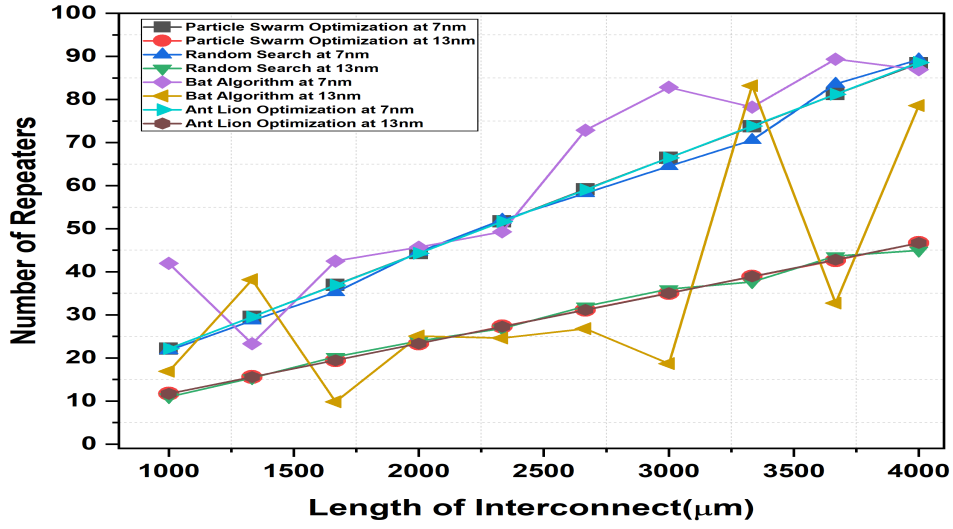


Figure 3.11: Optimal Number of Repeaters vs Length of Interconnect

#### 3.3.5 Power Delay Product(PDP) Optimized Repeaters Number and Size Dependency upon Specularity Parameter in Copper Interconnects

The number of repeaters required in a copper interconnect system also depends upon the specularity parameter which is denoted by 'p' in the equation of copper resistivity. Due to the change in 'p', the value of resistance per unit length changes due to which both the repeaters size and number of repeaters changes. The change in value of the p changes the time delay function values due to which it becomes a major factor during the calculation of the optimal repeater size and numbers in PDP model. The figure3.12 shows the variation in the repeater size on varying the value of p which also remains the same here. Repeater size increases with increasing specularity parameter. The findings of the repeaters size using Particle Swarm Optimization(PSO), Bat Algorithm(BA), Ant Lion Optimization(ALO), and Random Search(RS) algorithms in PDP model at both 7nm and 13nm technology nodes. It is clearly visible that the PSO and ALO both converges at both technology nodes at given values of the parameters while the other two algorithms could not produce expected results on one or the other technology node.

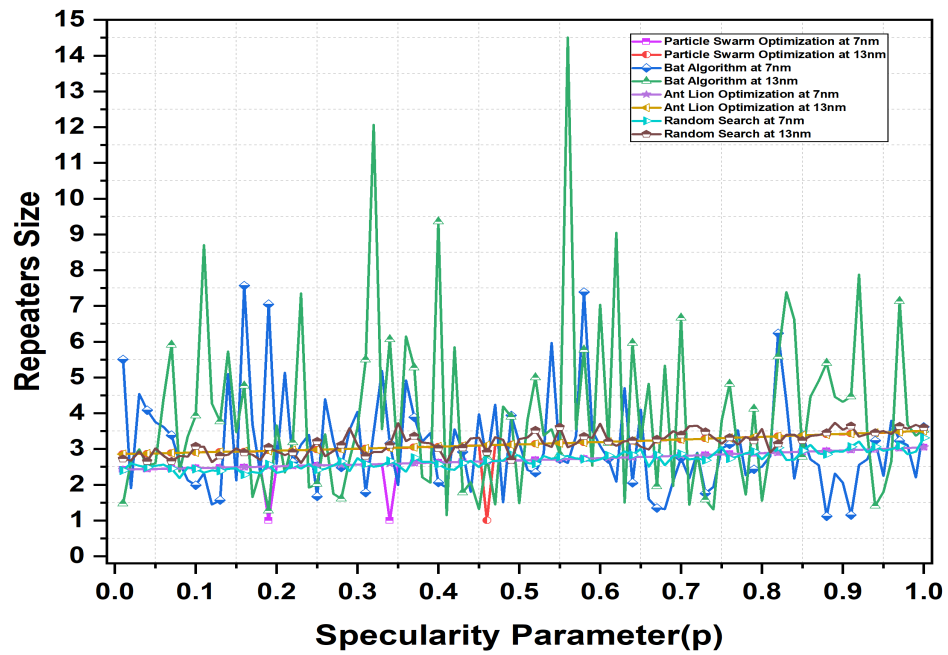


Figure 3.12: Repeaters Size vs Specularity Parameter

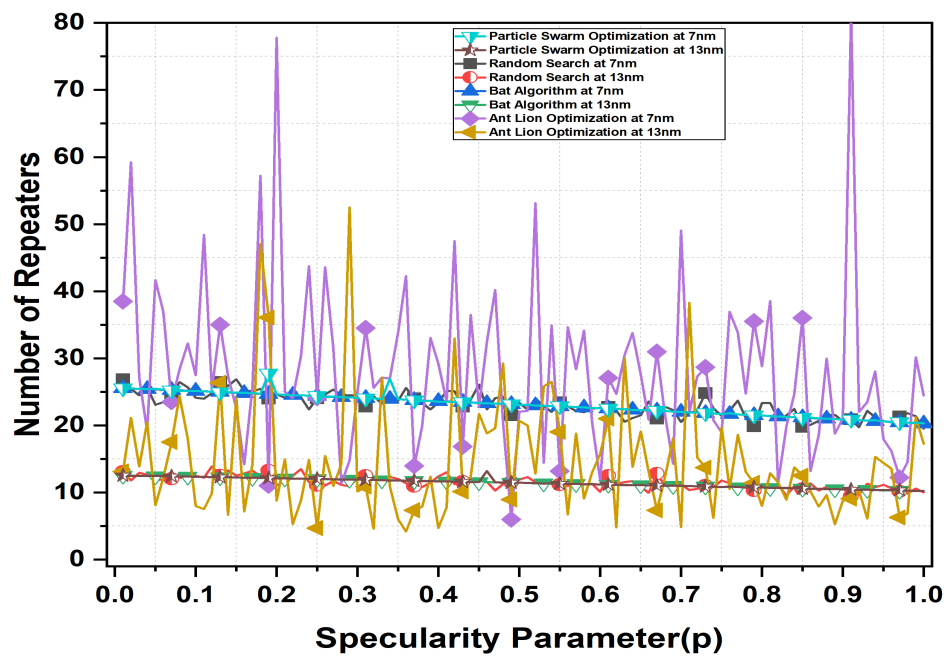


Figure 3.13: Repeaters Number vs Specularity Parameter

### **3. Delay and Power Delay Product optimized number of repeaters and repeater size for Copper Interconnects using various optimization algorithms**

---

The figure3.13 shows the results of the number of repeaters using Particle Swarm Optimization(PSO), Bat Algorithm(BA), Ant Lion Optimization(ALO), and Random Search(RS) algorithms in PDP model at both 7nm and 13nm technology nodes. It is clearly visible that the PSO, ALO and RS all converges at both technology nodes at given values of the parameters while the bat algorithm could not produce expected results on both the technology nodes.

On the basis of the above findings, we can infer that the bat algorithm is not producing the results as per expectation in the delay optimized model. So, we can't use it for producing the dataset for the neural network. Only PSO and ALO both have shown their capability to converge for both the repeaters size and repeaters number.

#### **3.3.6 Analysis of the Figure of Merit and Processing Time for various Optimization Algorithms**

We have calculated the Figure of Merit on length=  $1000\mu\text{m}$  when it is calculated for specular parameter and  $p= 0.41$  when it is calculated against length of the interconnect. We have done all the analysis only for 13nm technology node. The figure3.14 shows the variation of the Figure of Merit with the Number of Iterations. The Line depicting the Bat Algorithm shows that the Bat Algorithm does not converge in 100 iterations. Ant Lion Optimization converges in only 5 iterations, Random Search converges in 15 iterations and Particle Swarm Optimization converges in 20 iterations. As we have already seen that bat algorithm fails in most of the results which are also visible from this figure. The figure3.15 shows how the processing time increases in each of the optimization algorithm. Ant Lion Optimization takes the most time among all due to which we can not use this algorithm since total time to converge in this algorithm is much more than Particle Swarm optimization, Bat Algorithm and Random Search Algorithm. Therefore, we have remained with only Random Search and Particle Swarm Optimization algorithms as verified to generate the dataset for neural network but we have seen at few places random search algorithm fails to produce desired results.

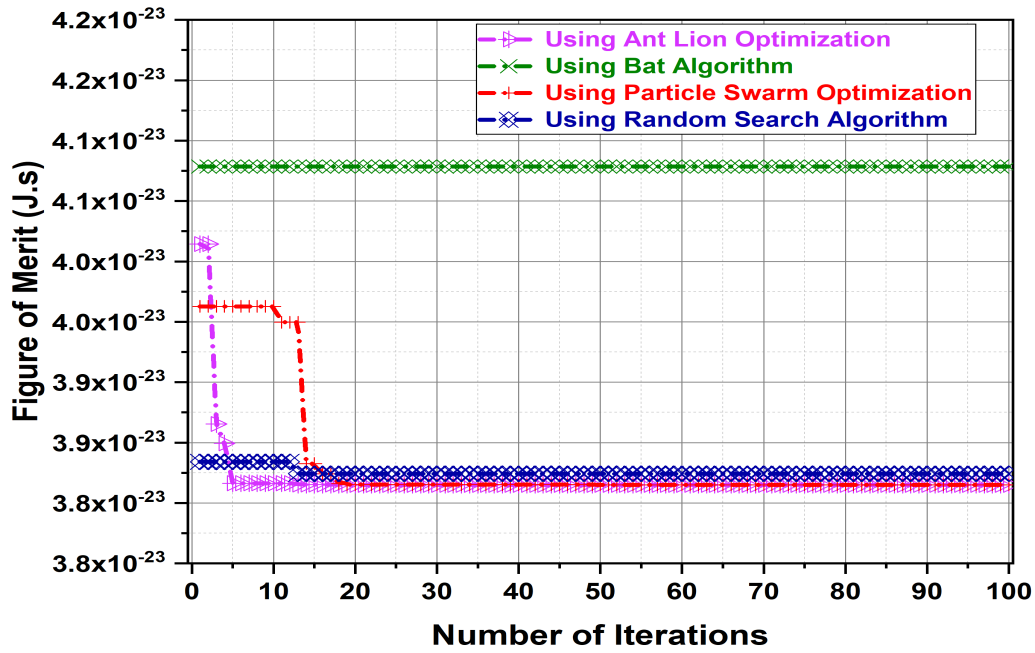


Figure 3.14: Figure of Merit Dependency upon Number of Iterations for various Algorithms

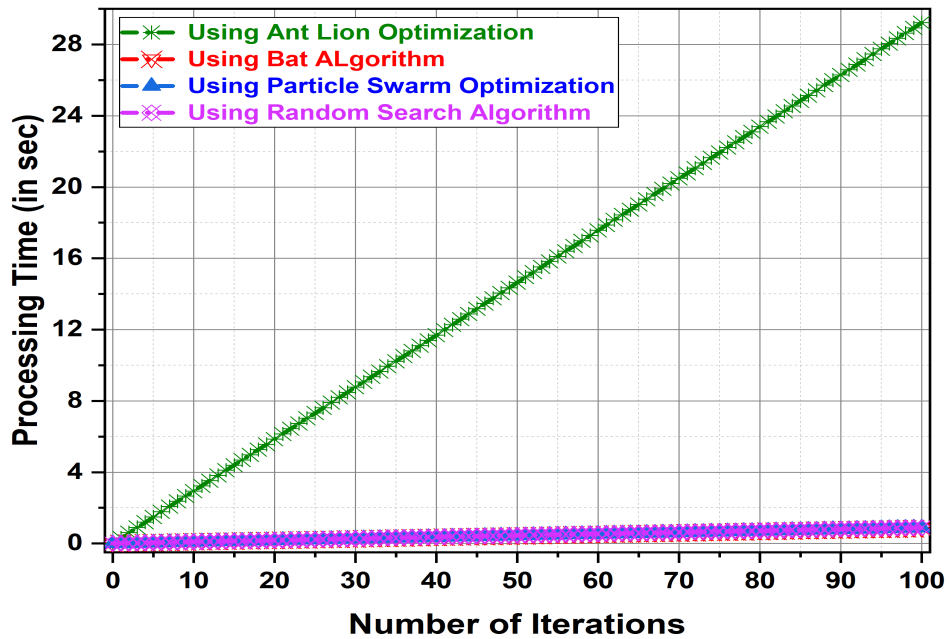


Figure 3.15: Processing Time for various Algorithms for given Number of Iterations

### 3. Delay and Power Delay Product optimized number of repeaters and repeater size for Copper Interconnects using various optimization algorithms

---

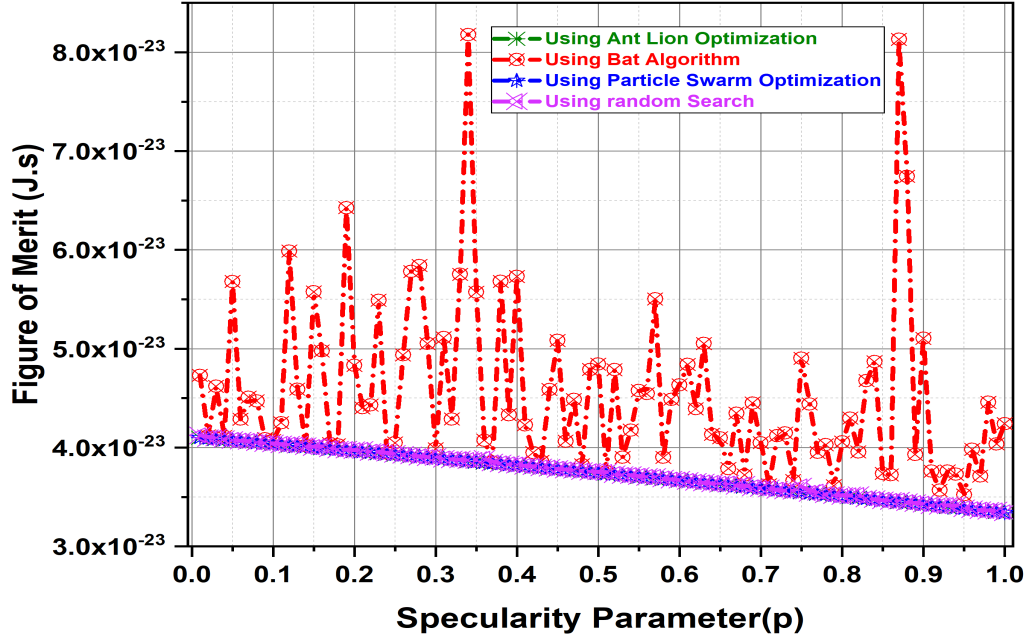


Figure 3.16: Figure of Merit Dependency upon Specularity Parameter for various Algorithms

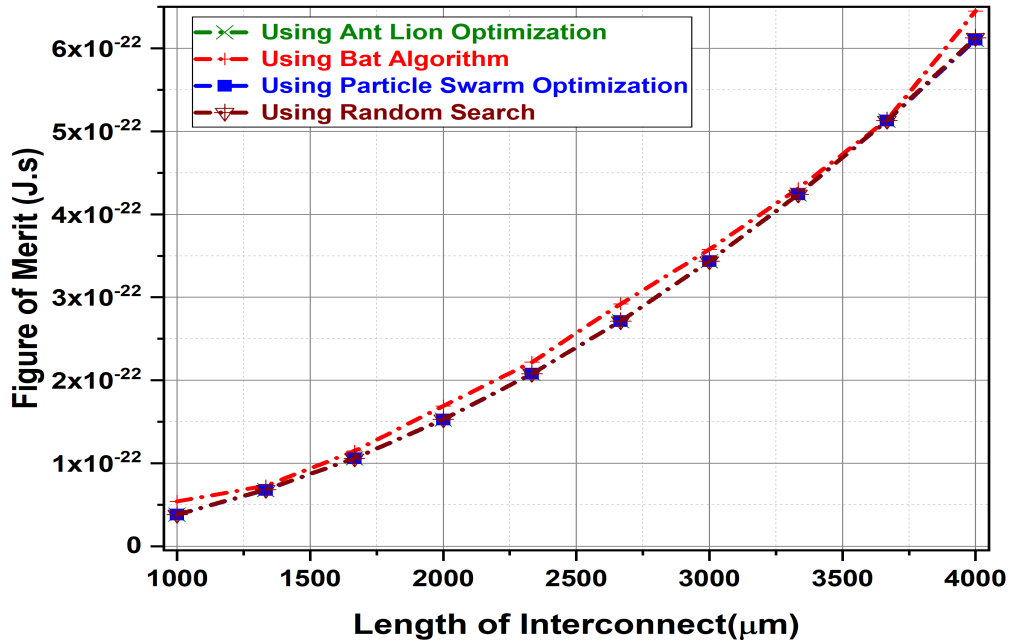


Figure 3.17: Figure of Merit Dependency upon Length of Interconnect for various Algorithms



On the basis of the above findings, we reach to a conclusion that we can make use of Particle Swarm Optimization for generating dataset for Neural Network. Figure of Merit is also our optimization function in the PDP model due to which it depends on both specularly parameter as well as length of the interconnect. The figure 3.16 and 3.17 shows the variation of FoM with specularly parameter and length of interconnect respectively for all the four optimization algorithms.

## **3.4 Summary**

In this chapter, we started with dicussion about the analytical models for the number of repeaters and their size. After that, we tried to produce the same results using Particle Swarm Optimization, Random Search. Ant Lion Optimization and Bat ALgorithm and after that we figured out that most of the algorithms are available to converge to the desired results at some or the other conditions. In the end, we did an anlysis of the figure of merit with number of iterations and processing time with number of iterations.

# 4

## Artificial Neural Networks for the repeater size and number of repeaters for Cu Interconnects

---

## 4.1 Artificial Neural Network

Deep learning relies on artificial neural networks as its fundamental building blocks. To solve complex data-driven problems, deep learning employs artificial neural networks that mimic human brain behaviour. Now, deep learning is a subset of machine learning, which falls under the AI umbrella. Machine learning and deep learning are interrelated fields that aid artificial intelligence by providing a set of algorithms and neural networks to solve data-driven problems. Deep learning utilises artificial neural networks within the human brain. A neural network functions when it receives input data. This data was processed by multiple layers of perceptrons to generate the desired output. Perceptrons in artificial neural networks accept and process inputs by passing them from the input layer to the hidden layer and then to the output layer. As each input is passed from the input layer to the hidden layer, a random initial weight is assigned. Where the perceptron output is incorrect, the neural network is trained using the back-propagation method. Initially, when designing the neural network, random weights are assigned to each input. We read only the weight of each input in order to minimise the error. This leads to a more precise output, which is precisely what backpropagation means. When output does not match the desired output, error back-propagation is used to update network parameters and minimise the error function (i.e. the squared error between the output and desired output). Repeat this process until the output does not match the desired output.

$$Output = w_1i_1 + w_2i_2 + w_3i_3 + ..... + w_ni_n + b \quad (4.1)$$

where  $w_i$  = weight for input and  $b$ =bias \* weight for bias.

The inputs are multiplied by their respective weights, and their sum is then passed through the network for further processing. Then, a numeric value known as bias is assigned to each perceptron, and each perceptron is subjected to activation or a transformation function that determines whether or not a particular perceptron receives activation. When output does not match the desired output, error backpropagation is used to update network

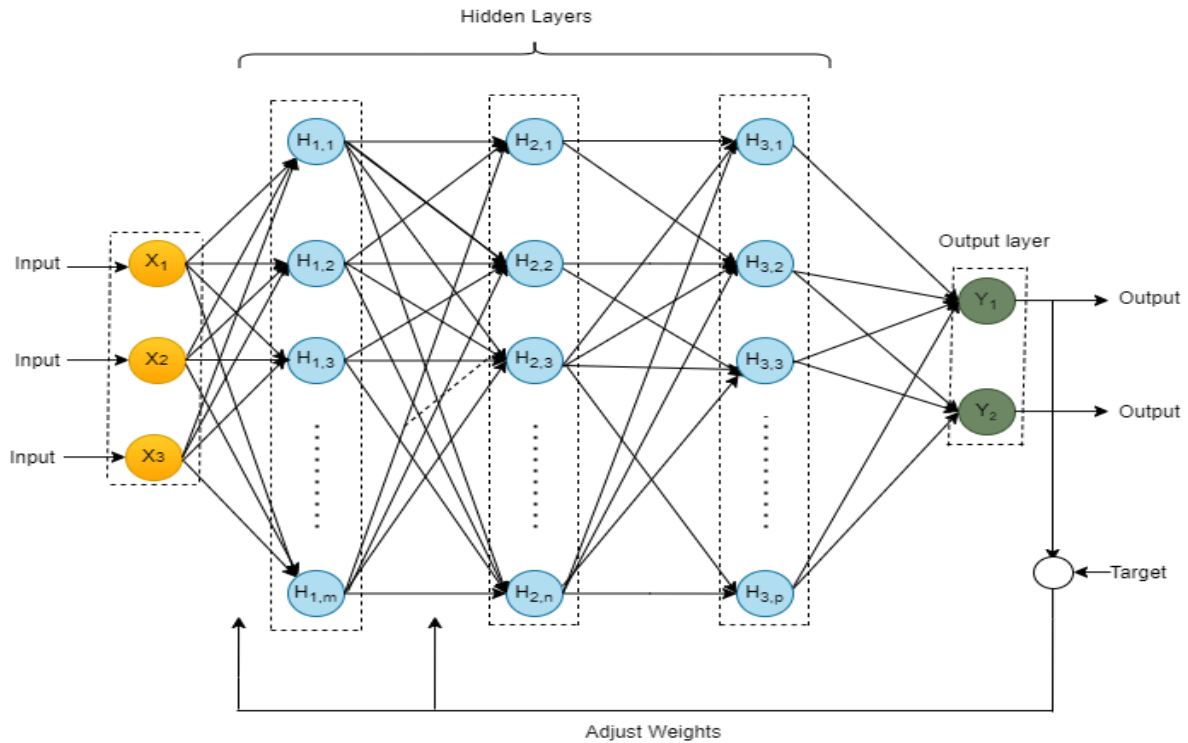
#### 4. Artificial Neural Networks for the repeater size and number of repeaters for Cu Interconnects

parameters and minimise the error function (i.e. the squared error between the output and desired output). This procedure is repeated until the actual output does not match the desired output. To compute error, we will employ the sigmoid function.

$$\text{sigmoid}(x) = \frac{1}{1 + e^{-x}} \quad (4.2)$$

$$\frac{d(\text{sigmoid}(x))}{dx} = \frac{e^{-x}}{(1 + e^{-x})^2} \quad (4.3)$$

When the perceptron output is wrong in such a situation we train the neural network by using the back-propagation method. Initially while designing the neural network the weights to each input are initialized with some random values and these waves denote the importance of each input variable therefore if we propagate backward in a neural network and compare the actual output to the predicted output.



**Figure 4.1:** Artificial Neural Network

## 4.2 Analysis of the Artificial Neural Network

Neural networks are widely recognized for their exceptional computational efficiency as they can directly predict the optimal solution. Compared to conventional methods, NNs demand less simulation time. For instance, if the PSO algorithm were to handle tens of thousands of data items, it would take around 25 hours to complete, while a neural network could accomplish the task in just about 4 seconds. We have taken three inputs technology nodes, length of interconnect and specularly parameter. We have used 20,000 samples dataset. We have developed a neural network having input layer, three hidden layers and output layer having 3 nodes in input layer, 30,12,5 nodes in three hidden layers and 2 nodes in the output layer. We have used 'sigmoid' as the activation function for the input layer and two hidden layers. For one hidden layer, we have used 'relu' activation function and output layer has 'sigmoid' as activation function.

The error backpropagation algorithm is utilized to adjust the parameters of the neural network and minimize the error between the network outputs and desired targets, typically measured by the squared error. This process is repeated iteratively until the output accuracy reaches the desired level. To train the network, the Levenberg-Marquardt (LM) algorithm is employed, which is a nonlinear optimization method that combines the strengths of both the Gauss-Newton and gradient descent techniques.

The figure4.2 and figure4.3 shows the processing time and mean squared error(loss) variation on number of epochs. The neural network converges in 200 epochs and 200 epochs take 8seconds times in ANN. The same dataset would have taken about 50hours from particle swarm optimization depicting the usefulness of ANN.

The table4.1 shows the values of repeater size, number of repeaters which are found through particle swarm optimization and artificial neural networks at the given length of  $1000\mu\text{m}$  and at 13nm technology node. The table also shows the comparison between the processing time of artificial neural network and particle swarm optimization at same given conditions.

#### 4. Artificial Neural Networks for the repeater size and number of repeaters for Cu Interconnects

---

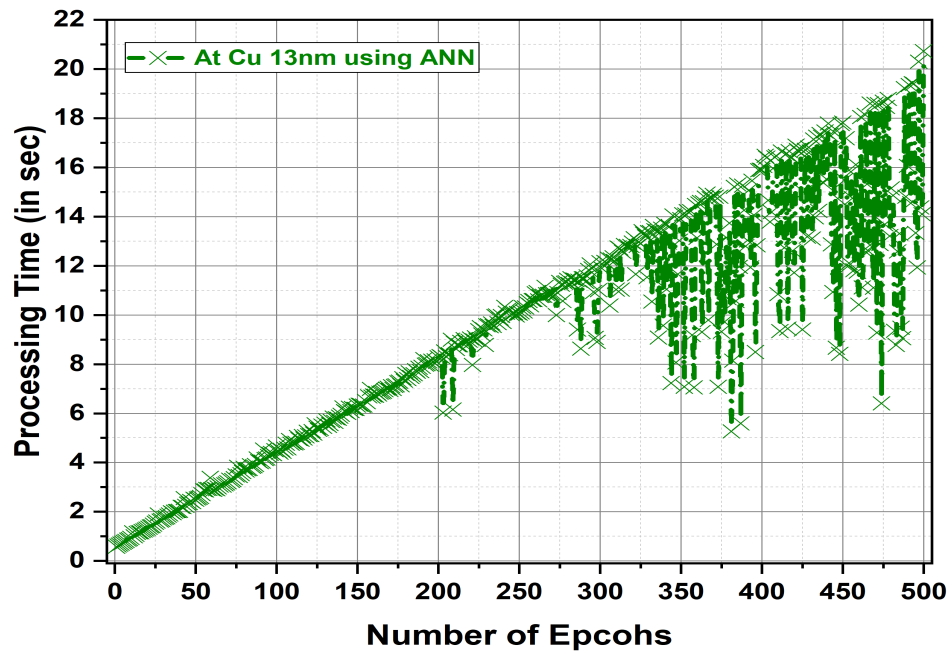


Figure 4.2: Variation in the Processing Time on increasing Number of Epochs

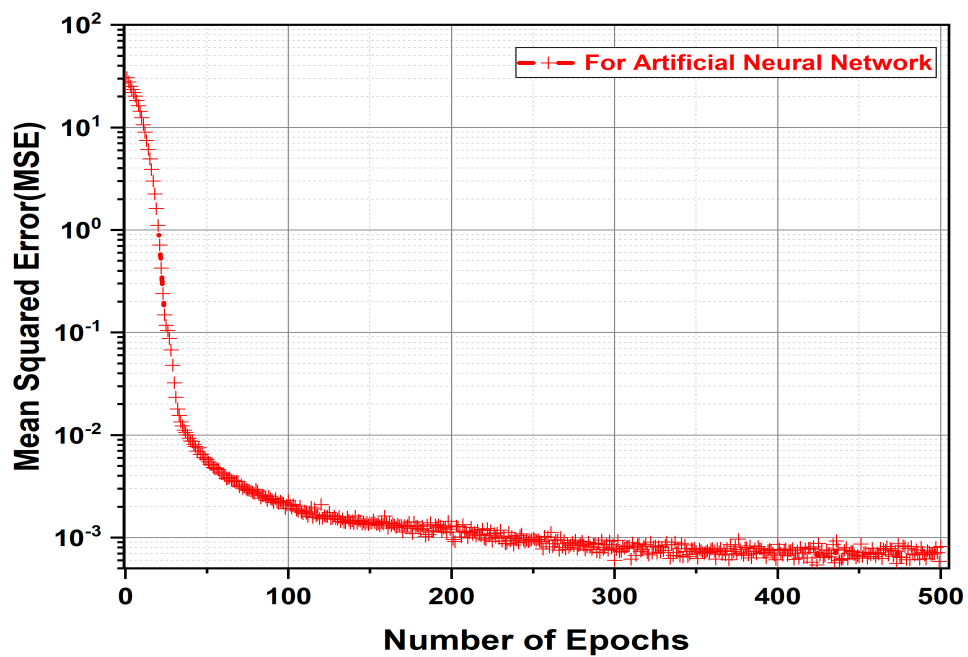


Figure 4.3: Variation in the Mean Squared Error on increasing Number of Epochs

**Table 4.1:** Comparative Analysis of the Results at  $1000\mu\text{m}$  length and 13nm technology node.

Parameters	PSO	ANN
Repeater Size	5.6150	5.615714
Number of Repeaters	38.404	38.379
Processing Time	50hrs	8sec

## 4.3 Summary

In this chapter, we have discussed about the architecture of the neural network we have built. We also threw light on the activation functions used in the neural network training. We have also discussed about the results obtained from the best optimization algorithm found in the last chapter which is particle swarm optimization with our neural network results in the table4.1. We have also shown the variations in the mean squared error and processing time with respect to the number of epochs run in the neural network.

# 5

## Conclusions and Future Scope

---



## 5.1 Conclusion

The effective resistivity of copper interconnect is an important factor in the design and manufacture of various ICs. The next important factor is the effective mean free path of the interconnects. We have designed machine learning models and analytical functions to approximate the value of effective resistivity and mean free path in copper interconnects. We have designed the mathematical models in python to visualise the optimal number of repeaters in copper interconnect at various technology nodes analytically. In this study, we have optimised the number of repeaters and repeater size using all the four Particle Swarm Optimization, Bat Algorithm, Ant Lion Optimization and Random Search Algorithm and comparative study is done for all the four algorithms for 7 and 13nm technology nodes in copper interconnects in both time delayed and power delayed product models. From the results obtained, we conclude that among the four optimization algorithms Particle Swarm Optimization is the best one to produce desired results.

Further we deployed the Artificial Neural Network producing the similar results to the expectation in few seconds as compared to Particle Swarm Optimization which take 50hours for the same data.

The similar machine learning can be extended to the study of Carbon Nano Tube(CNT) interconnects, Graphene Nanoribbon interconnects(GNR), Cu-CNT, Cu-GNR, Borophene, Cu-BNR and all other interconnects.

# Bibliography

- [1] S. Kumar, “Design space exploration of nanoscale interconnects with rough surfaces,” pp. 2–3, 12 2015. [Online]. Available: <https://doi.org/10.1109/EDAPS.2015.7383683>
- [2] M. Al Hafiz, M. MacKenzie, and C. Kwok, “Design methodology of focusing elements for multilevel planar optical systems in optical interconnects,” *Optical Engineering*, vol. 48, pp. 5401–, 12 2009. [Online]. Available: <https://doi.org/10.1117/1.3269682>
- [3] M. Stucchi, P. J. Roussel, Z. Tokei, S. Demuynck, and G. Groeseneken, “A comprehensive learner-aware tddb lifetime model for advanced cu interconnects,” *IEEE Transactions on Device and Materials Reliability*, vol. 11, no. 2, pp. 278–289, 2011. [Online]. Available: <https://doi.org/10.1109/TDMR.2011.2121909>
- [4] K. Agarwal, D. Sylvester, and D. Blaauw, “Modeling and analysis of crosstalk noise in coupled rlc interconnects,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 5, pp. 892–901, 2006. [Online]. Available: <https://doi.org/10.1109/TCAD.2005.855961>
- [5] C. Venkataiah, K. Satyaprasad, and T. Prasad, “Insertion of an optimal number of repeaters in pipelined nano-interconnects for transient delay minimization,” *Circuits, Systems, and Signal Processing*, vol. 38, pp. 1–17, 02 2019. [Online]. Available: <https://doi.org/10.1007/s00034-018-0876-7>
- [6] [Online]. Available: <https://www.lamresearch.com/products/our-solutions/>
- [7] Y. Ismail and E. Friedman, “Effects of inductance on the propagation delay and repeater insertion in vlsi circuits,” in *Proceedings 1999 Design Automation Conference (Cat. No. 99CH36361)*, 1999, pp. 721–724. [Online]. Available: <https://doi.org/10.1109/DAC.1999.782051>
- [8] Q. Lu, Z. Zhu, Y. Yang, and R. Ding, “Analysis of propagation delay and repeater insertion in single-walled carbon nanotube bundle interconnects,” *Microelectronics Journal*, vol. 54, pp. 85–92, 2016. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0026269216301379>
- [9] K. Banerjee and A. Mehrotra, “A power-optimal repeater insertion methodology for global interconnects in nanometer designs,” *IEEE Transactions on Electron Devices*, vol. 49, no. 11, pp. 2001–2007, 2002. [Online]. Available: <https://doi.org/10.1109/TED.2002.804706>
- [10] X.-C. Li, J.-F. Mao, H.-F. Huang, and Y. Liu, “Global interconnect width and spacing optimization for latency, bandwidth and power dissipation,” *IEEE Transactions on Electron Devices*, vol. 52, no. 10, pp. 2272–2279, 2005. [Online]. Available: <https://doi.org/10.1109/TED.2005.856795>

- [11] W.-S. Zhao, P.-W. Liu, H. Yu, Y. Hu, G. Wang, and M. Swaminathan, "Repeater insertion to reduce delay and power in copper and carbon nanotube-based nanointerconnects," *IEEE Access*, vol. 7, pp. 13 622–13 633, 2019. [Online]. Available: <https://doi.org/10.1109/ACCESS.2019.2893960>
- [12] W. Li, W.-S. Zhao, P. Liu, J. Wang, and G. Wang, "Optimal repeater insertion for horizontal and vertical graphene nanoribbon interconnects," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 33, 03 2020. [Online]. Available: <https://doi.org/10.1002/jnm.2696>
- [13] S. Kumar and R. Sharma, "Analytical model for resistivity and mean free path in on-chip interconnects with rough surfaces," *IEEE Transactions on Emerging Topics in Computing*, vol. PP, pp. 1–1, 08 2016. [Online]. Available: <https://doi.org/10.1109/TETC.2016.2597542>
- [14] B. Kumari, R. Kumar, R. Sharma, and M. Sahoo, "Design, modeling and analysis of cu-carbon hybrid interconnects," *IEEE Access*, vol. PP, pp. 1–1, 08 2021. [Online]. Available: <https://doi.org/10.1109/ACCESS.2021.3104299>
- [15] C. Venkataiah, K. Satyaprasad, and T. Prasad, "Insertion of an optimal number of repeaters in pipelined nano-interconnects for transient delay minimization," *Circuits, Systems, and Signal Processing*, vol. 38, pp. 1–17, 02 2019. [Online]. Available: <https://doi.org/10.1007/s00034-018-0876-7>
- [16] P.-W. Liu, W.-S. Zhao, D. Wang, J. Wang, Y. Hu, and G. Wang, "Optimal repeater insertion for nano-interconnects in current-mode signaling scheme," *Micro Nano Letters*, vol. 15, 01 2020. [Online]. Available: <https://doi.org/10.1049/mnl.2019.0765>
- [17] P. Uma Sathyakam, S. Raj, A. Karthikeyan, and P. Mallick, "A pso based optimal repeater insertion technique for carbon nanotube interconnects," *International Journal of Electronics Letters*, vol. 10, no. 3, pp. 344–353, 2022. [Online]. Available: <https://doi.org/10.1080/21681724.2021.1941283>
- [18] Z.-H. Cheng, W.-S. Zhao, D. Wang, J. Wang, L. Dong, G. Wang, and W.-Y. Yin, "Analysis of cu-graphene interconnects," *IEEE Access*, vol. PP, 09 2018. [Online]. Available: <https://doi.org/10.1109/ACCESS.2018.2869468>
- [19] D. Das, "Delay optimization using repeater insertion in folded graphene nanoribbon interconnect systems," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 34, 07 2021. [Online]. Available: <https://doi.org/10.1002/jnm.2872>

