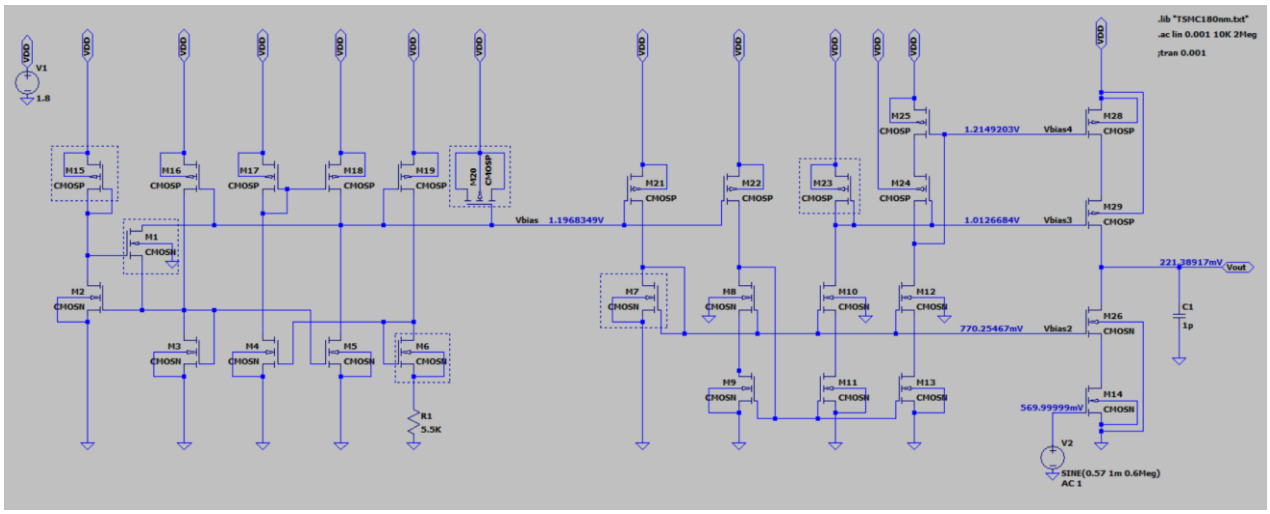
Indian Institute of Technology Ropar

EE301: Analog Ciruits

180nm:

The LTspice schematic for the 180nm circuit:



TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.51	volts
SHORT	20.0/0.18			
Idss		547	-250	uA/um
Vth		0.51	-0.51	volts
Vpt		4.8	-5.6	volts
WIDE	20.0/0.18			
Ids0		14.4	-4.7	pA/um
LARGE	50/50			
Vth		0.43	-0.42	volts
Vjbkd		3.1	-4.3	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		175.4	-35.6	uA/V^2
Low-field Mobility		416.52	84.54	cm^2/V*s

The image above is taken from the provided 180nm_file_information.txt file.

Here we can see that the values are given as:

For NMOS:

U_nC_{ox} = 175.4*2 = 350.8 uA/V^2

Threshold Voltage V_{th} = 0.5 V

For PMOS:

U_pC_{ox} = -35.6*2 = -71.2 uA/V^2

Threshold Voltage V_{th} ≈ -0.5 V

Lets, assume the frequency to be F = 0.6MHz or 600KHz

And we know that: $F = \frac{1}{2\pi * C * R_{out}}$

Capacitance is given as C = 1pF

Putting the values of F and C we get R_{out} = 265393 KΩ

And Voltage gain $A_v = g_m * R_{out}$

As per the target specifications, A_v = 20 or 26dB

So, we get $g_m = \frac{A_v}{R_{out}} = 75.3\ \mu A/V$

For NMOS:

In saturation, the current equation is: $I_D = \frac{1}{2}\ \mu_n C_{ox} \frac{W}{L}\ {V_{ov}}^2$

Where $V_{ov} = V_{gs} - V_{th}$

For NMOS:

In saturation, the current equation is: $I_D = \frac{1}{2}\ \mu_n C_{ox} \frac{W}{L}\ {V_{ov}}^2$

Where $V_{ov} = V_{gs} - V_{th}$

$V_{gs} \geq V_{th}$ & $V_{ds} \geq V_{gs} - V_{th}$

We can get the swing as:

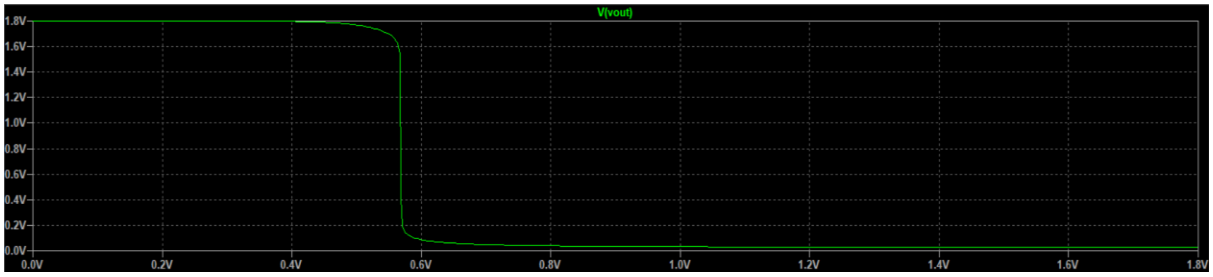
$$V_g \geq V_{th} - V_s \quad \& \quad V_g \leq V_{th} + V_{th}$$

Assuming $V_{ds\ sat}$ = 0.2V

For Amplifer, I got the swing as (using V_{th} = 0.5 & $V_{ds\ min}$ or $V_{ds\ sat}$ = 0.2) :

1. M14: 0.5 – 0.7
2. M26: 0.7 – 0.9
3. M29: 0.9 – 1.1
4. M28: 1.1 – 1.3

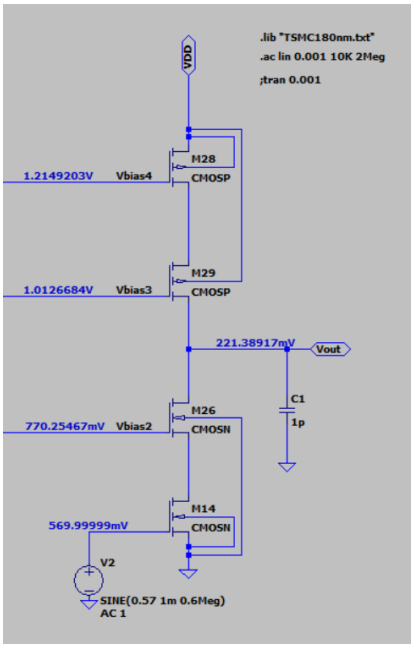
Now ran a DC sweep from 0V to 1.8V to get the V_{bias1} :



From the graph it can be clearly seen that the V_{bias1} = 0.57V

Now, taking biasing voltages in the voltage swing range to ensure operation of all mosfet in saturation region.

We checked for different values of corresponding bias voltages Vbias2, Vbias3 and Vbias4 and W/L ratios according to bias voltages to get the 26dB gain.



And got the values as:

V_{bias1} = 0.57V, W/L = 3.7

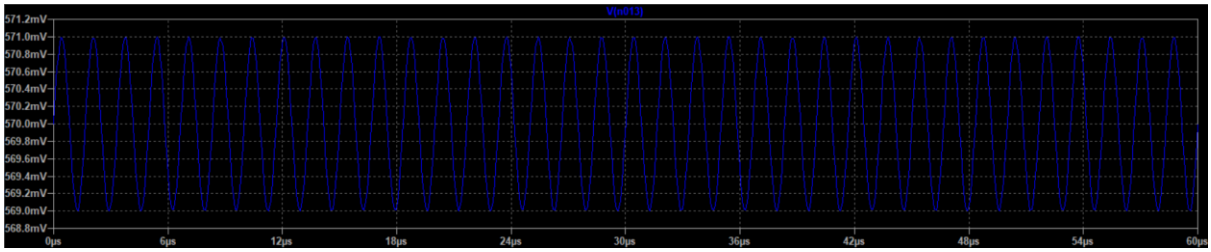
V_{bias2} = 0.77 V, W/L = 3.7

V_{bias3} = 1.01 V, W/L = 10.4

V_{bias4} = 1.21 V, W/L = 10.4

Observations:

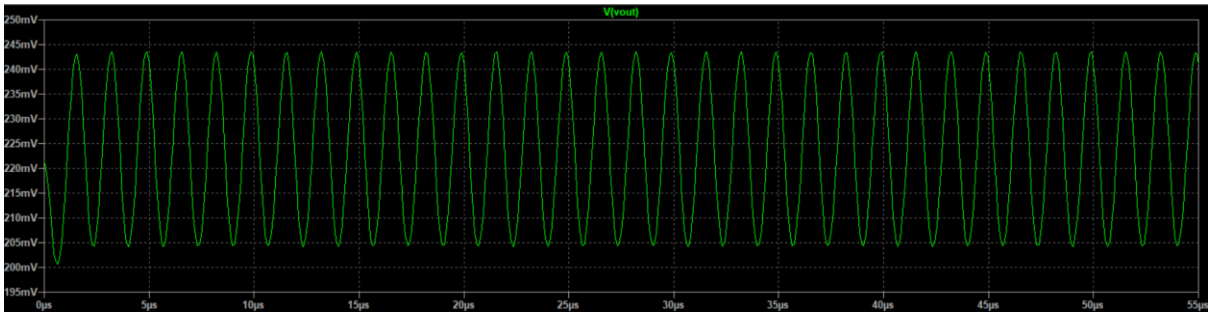
Input Voltage:



We have given input bias voltage or DC offset = 0.57V and small signal AC voltage amplitude = 1mV.

So the peak-peak input voltage = 2mV

Output Voltage:

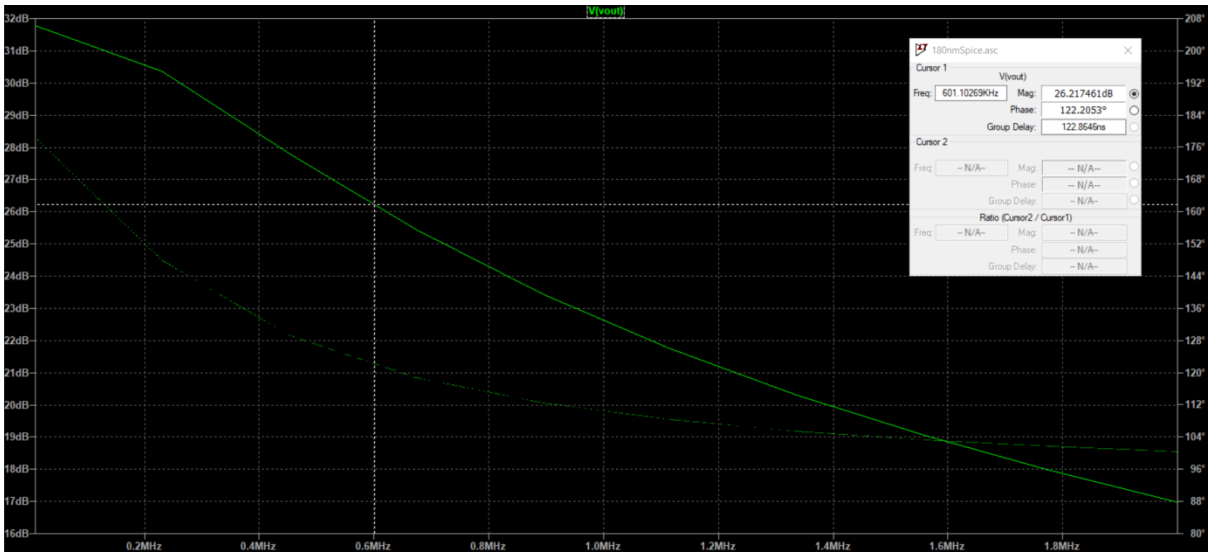


Got the output as Vmax = 243mV & Vmin = 203mV.

So peak-peal = 40mV.

So voltage gain = (peak-peak output)/(peak-peak input) = 40/2 = 20 V/V

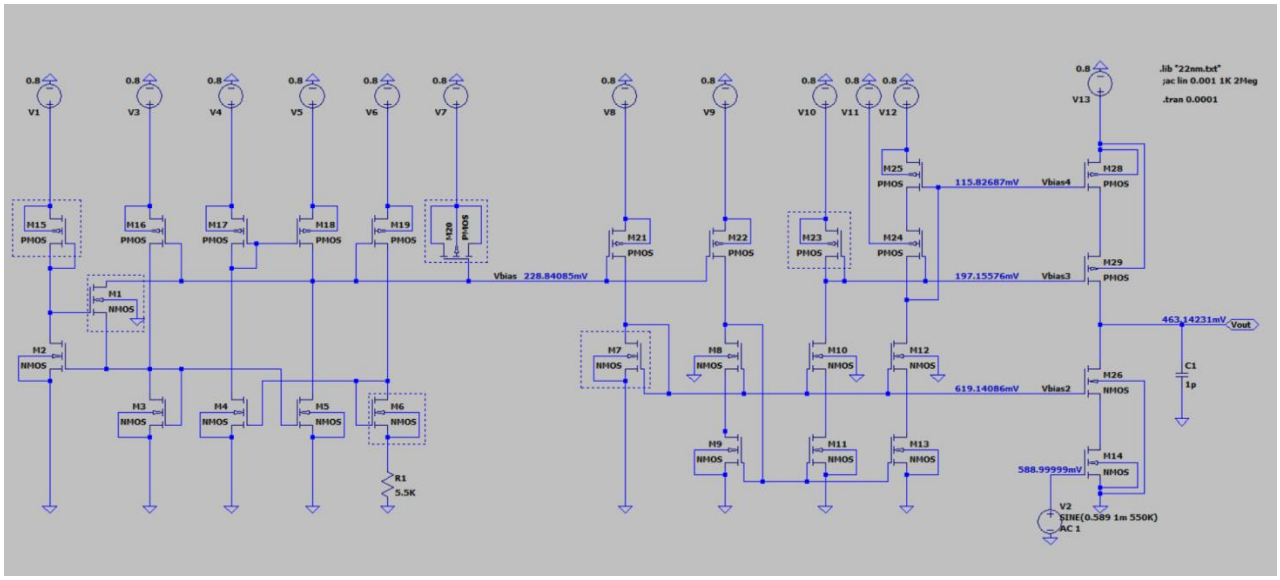
Gain vs Frequency:



Can be seen from the frequency curve as well that is shown above that the gain comes out to be 26dB that is 20V/V.

22NM:

The LTspice schematic for the 22nm circuit:



Since the information file for 22nm was not provided, so I searched on google to get the values for 22nm and got a range of values so took the mid values as shown below.

For NMOS:

U_nC_{ox} = 100 – 200(range) ≈ 150 uA/V^2

Threshold Voltage V_{th} = 0.2 – 0.4 ≈ 0.3V

For PMOS:

U_pC_{ox} = 50 – 100(range) = -70 uA/V^2

Threshold Voltage V_{th} ≈ -0.3 V

Lets, assume the frequency to be F = 0.550MHz or 550KHz

And we know that: $F = \frac{1}{2\pi * C * R_{out}}$

Capacitance is given as C = 1pF

Putting the values of F and C we get R_{out} = 289519 KΩ

And Voltage gain $A_v = g_m * R_{out}$

As per the target specifications, A_v = 20 or 26dB

So, we get $g_m = \frac{A_v}{R_{out}} = 69\ \mu A/V$

For NMOS:

In saturation, the current equation is: $I_D = \frac{1}{2}\ \mu_n C_{ox} \frac{W}{L}\ {V_{ov}}^2$

Where $V_{ov} = V_{gs} - V_{th}$

For NMOS:

In saturation, the current equation is: $I_D = \frac{1}{2}\,\mu_n C_{ox}\frac{W}{L}\,{V_{ov}}^2$

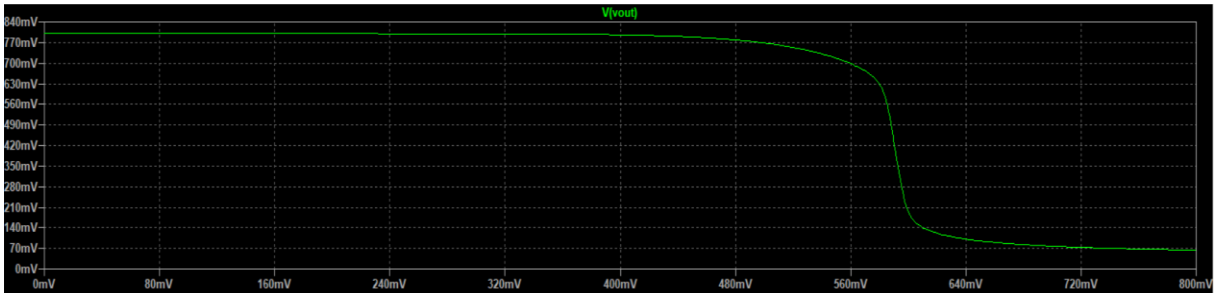
Where $V_{ov} = V_{gs} - V_{th}$

$V_{gs} \geq V_{th}$ & $V_{ds} \geq V_{gs} - V_{th}$

We can get the swing as:

$$V_g \geq V_{th} - V_s \quad \& \quad V_g \leq V_{th} + V_{th}$$

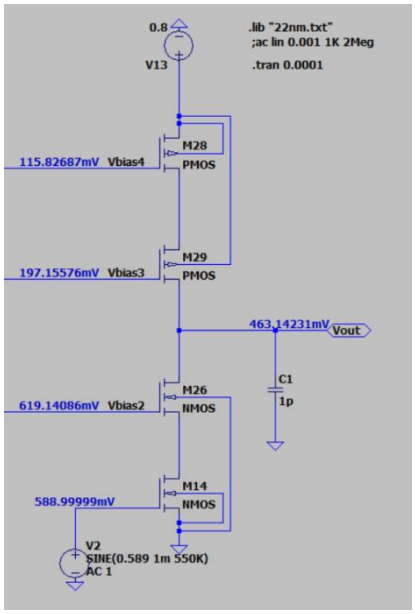
Now ran a DC sweep from 0V to 1.8V to get the V_{bias1} :



From the graph it can be clearly seen that the V_{bias1} = 0.589V

Now, taking biasing voltages in the voltage swing range to ensure operation of all mosfet in saturation region.

We checked for different values of corresponding bias voltages Vbias2, Vbias3 and Vbias4 and W/L ratios according to bias voltages to get the 26dB gain.



And got the values as:

V_{bias1} = 0.589V, W/L = 8.1

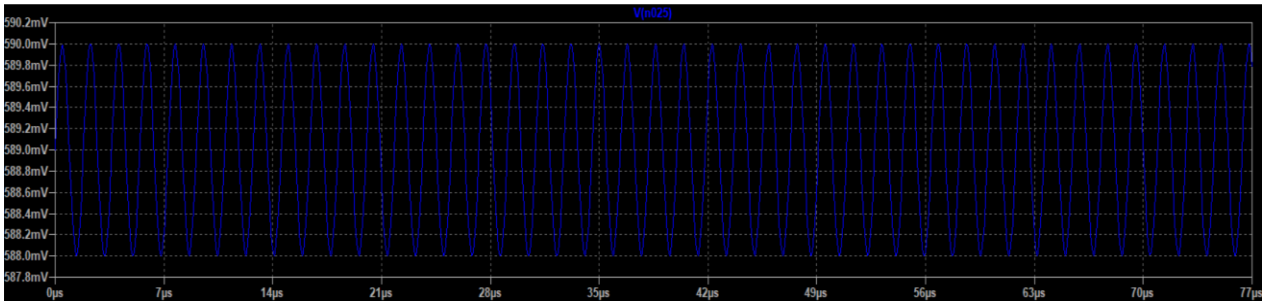
V_{bias2} = 0.619V, W/L = 8.1

V_{bias3} = 0.197 V, W/L = 17

V_{bias4} = 0.115 V, W/L = 17

Observations:

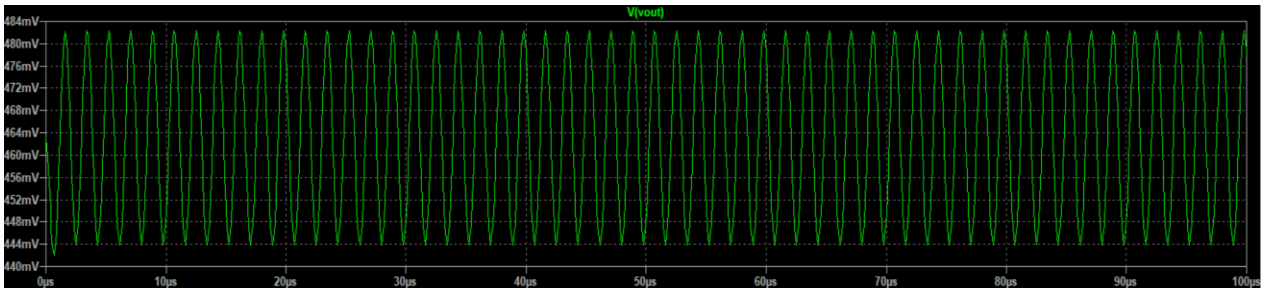
Input Voltage:



We have given input bias voltage or DC offset = 0.589V and small signal AC voltage amplitude = 1mV.

So the peak-peak input voltage = 2mV

Output Voltage:

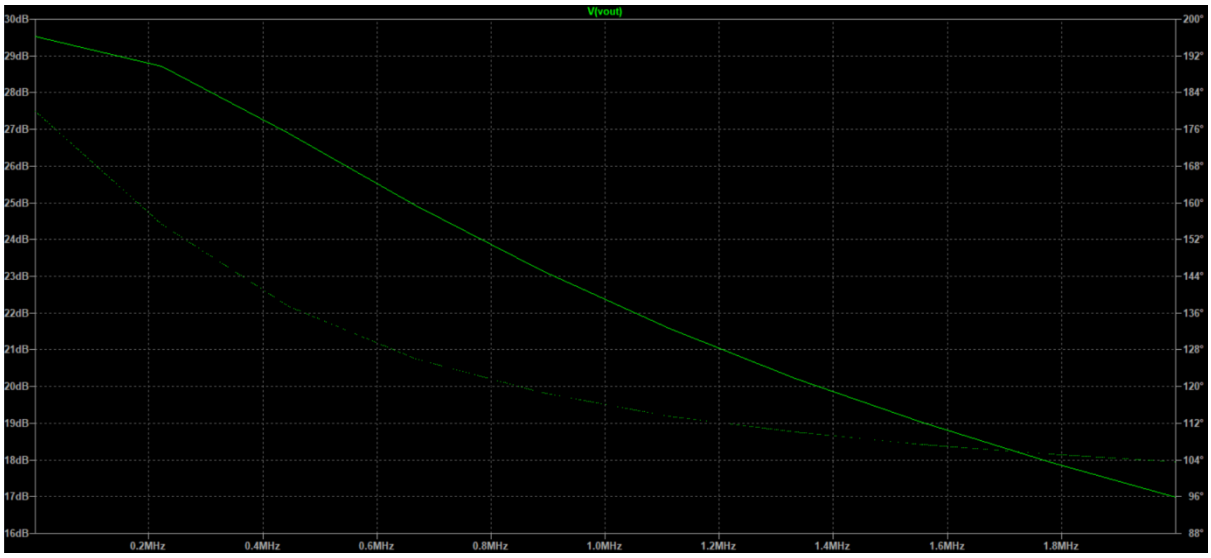


Got the output as Vmax = 482mV & Vmin = 442mV.

So peak-peal = 40mV.

So voltage gain = (peak-peak output)/(peak-peak input) = 40/2 = 20 V/V

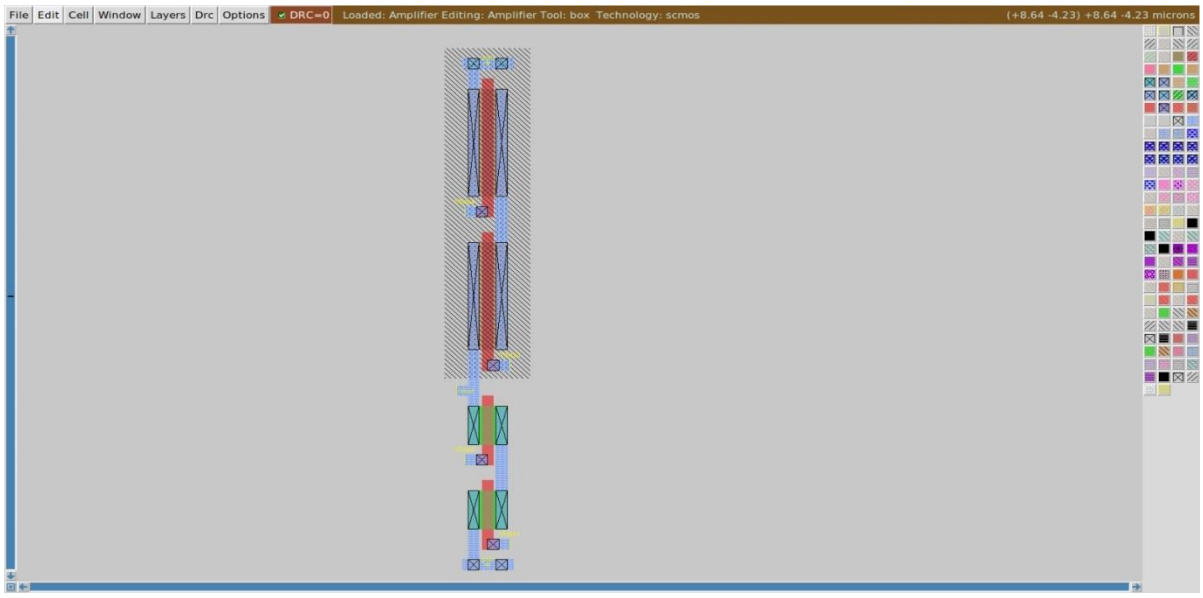
Gain vs Frequency:



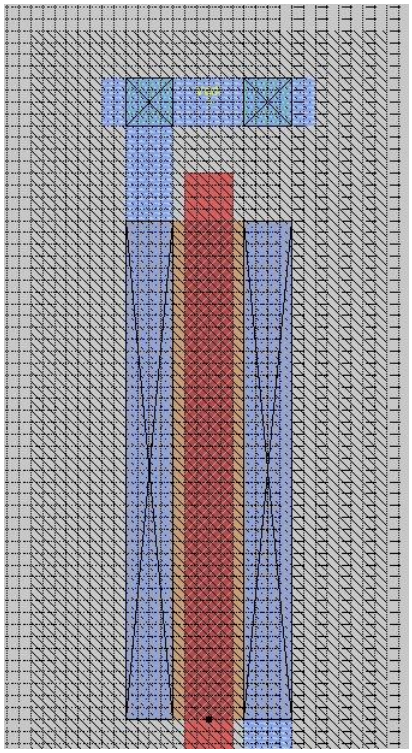
Can be seen from the frequency curve as well that is shown above that the gain comes out to be 26dB that is 20V/V.

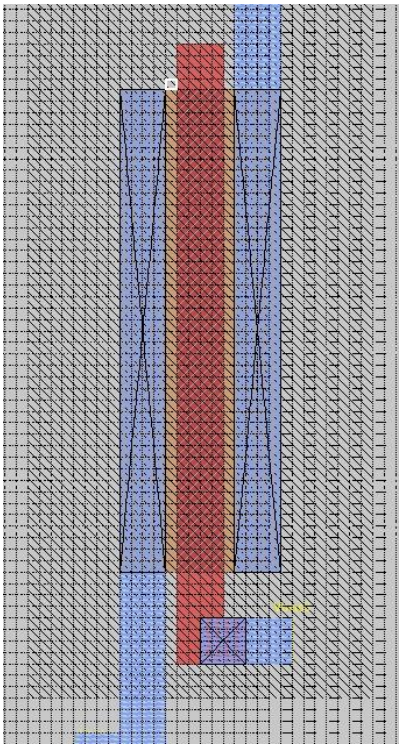
MAGIC LAYOUT:

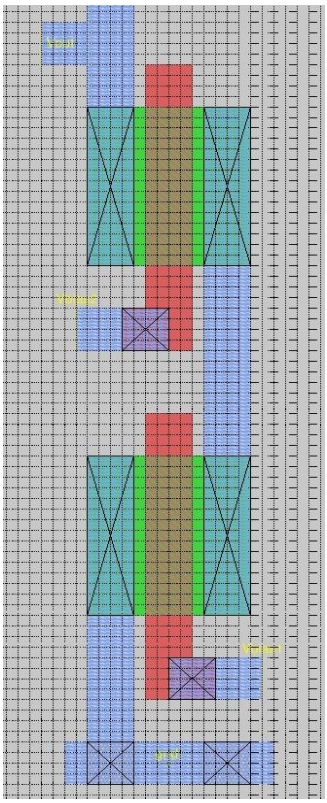
Cascode Amplifer:



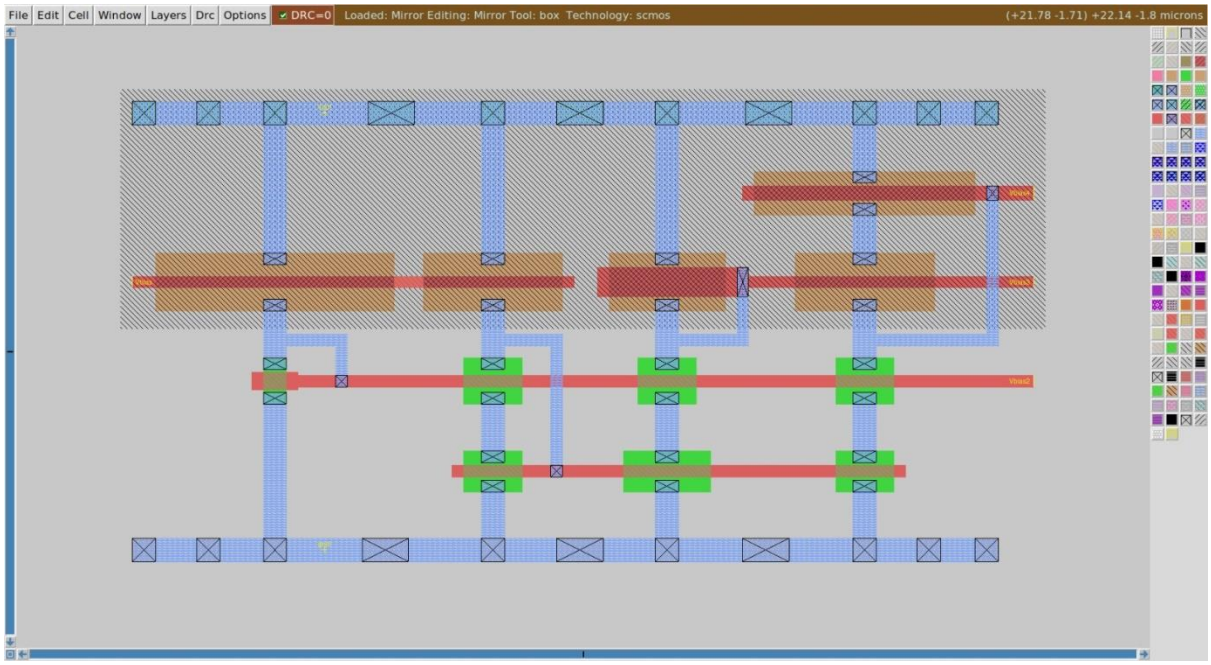
More zoomed images of cascade amplifier magic layout:



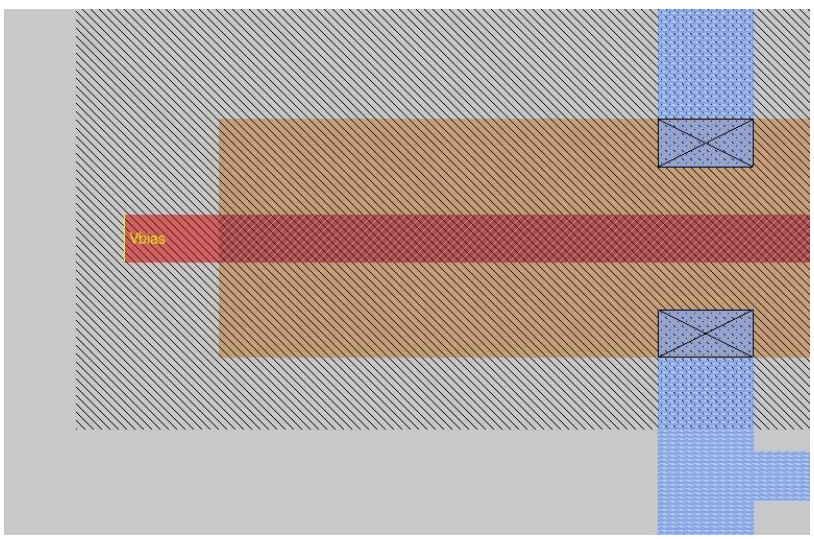


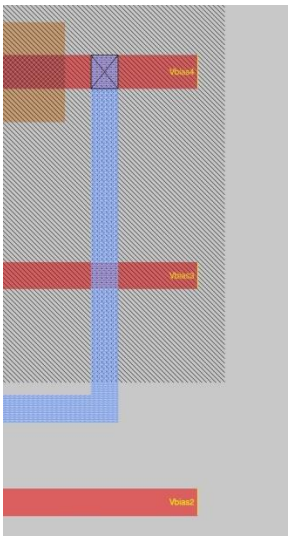


Current Mirror:



Zoomed images of input and output terminals:





THANK YOU ☺