Appendix B

Complete CDAC FPGA Board UCF

 # clock pins

```
NET "clk" LOC = "P51"; # Bank = 0, Signal name = FPGA_clk_25
NET "clk" CLOCK_DEDICATED_ROUTE = FALSE;
```

 # Pin assignment for seven segment

```
NET "Colon"  LOC =  "P124"; # Signal name = Colon (:)
NET "Top DP"  LOC =  "P123"; # Signal name =  DP of the rightmost seven segment display
NET "seg<0>" LOC = "P140"; # Bank = 1, Signal name = CA
NET "seg<1>" LOC = "P137"; # Bank = 1, Signal name = CB
NET "seg<2>" LOC = "P134"; # Bank = 1, Signal name = CC
NET "seg<3>" LOC = "P133"; # Bank = 2, Signal name = CD
NET "seg<4>" LOC = "P131"; # Bank = 2, Signal name = CE
NET "seg<5>" LOC = "P127"; # Bank = 1, Signal name = CF
NET "seg<6>" LOC = "P126"; # Bank = 1, Signal name = CG
NET "dp" LOC = "P121";          # Bank = 1, Signal name = DP
NET "anode<0>" LOC = "P120"; # Bank = 1, Signal name = AN0
NET "anode<1>" LOC = "P119"; # Bank = 1, Signal name = AN1
NET "anode<2>" LOC = "P118"; # Bank = 1, Signal name = AN2
NET "anode<3>" LOC = "P117"; # Bank = 1, Signal name = AN3
```

 # Pin assignment for LEDs

```
NET "led<7>" LOC = "P97" ; # Bank = 3, Signal name = LD7
NET "led<6>" LOC = "P98" ; # Bank = 2, Signal name = LD6
NET "led<5>" LOC = "P99" ;  # Bank = 2, Signal name = LD5
NET "led<4>" LOC = "P100" ;  # Bank = 2, Signal name = LD4
NET "led<3>" LOC = "P101" ; # Bank = 2, Signal name = LD3
NET "led<2>" LOC = "P102" ; # Bank = 3, Signal name = LD2
NET "led<1>" LOC = "P104" ; # Bank = 2, Signal name = LD1
NET "led<0>" LOC = "P105" ;  # Bank = 2, Signal name = LD0
```

 # Pin assignment for SWs

```
NET "sw<14>" LOC = "P78";  # Bank = 2, Signal name = SW14
NET "sw<13>" LOC = "P79";  # Bank = 2, Signal name = SW13
NET "sw<12>" LOC = "P80";  # Bank = 2, Signal name = SW12
NET "sw<11>" LOC = "P81";  # Bank = 2, Signal name = SW11
NET "sw<10>" LOC = "P82";  # Bank = 2, Signal name = SW10
NET "sw<9>" LOC = "P83";  # Bank = 3, Signal name = SW9
NET "sw<8>" LOC = "P84";  # Bank = 3, Signal name = SW8
NET "sw<7>" LOC = "P85";  # Bank = 3, Signal name = SW7
NET "sw<6>" LOC = "P87";  # Bank = 3, Signal name = SW6
NET "sw<5>" LOC = "P88";  # Bank = 3, Signal name = SW5
NET "sw<4>" LOC = "P92";  # Bank = 3, Signal name = SW4
NET "sw<3>" LOC = "P93";  # Bank = 2, Signal name = SW3
```

 # Pin assignment for push buttons

```
NET "btn<0>" LOC = "P139";  # Bank = 1, Signal name = BTN0
NET "btn<1>" LOC = "P143";  # Bank = 0, Signal name = BTN1
NET "btn<2>" LOC = "P142"; # Bank = 2, Signal name = BTN2
NET "btn<3>" LOC = "P141"; # Bank = 0, Signal name = BTN3
```

 # Pin assignment for VGA

```
NET "hsync" LOC = "P47"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = HSYNC
NET "vsync" LOC = "P46"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = VSYNC


NET "OutRed<2>"  LOC = "P59"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = RED2
NET "OutRed<1>"  LOC = "P61"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = RED1
NET "OutRed<0>"  LOC = "P62"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = RED0
NET "OutGreen<2>"  LOC = "P56"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = GRN2
NET "OutGreen<1>"  LOC = "P57"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = GRN1
NET "OutGreen<0>"  LOC = "P58"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = GRN0
NET "OutBlue<2>"  LOC = "P48"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = BLU1
NET "OutBlue<1>"  LOC = "P50"  | DRIVE = 2  | PULLUP ; # Bank = 1, Signal name = BLU0
```