

Binary Code				Grey Code			
B ₃	B ₂	B ₁	B ₀	G ₃	G ₂	G ₁	G ₀
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	1
1	1	0	0	1	1	0	0
1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1

~ Tenth table of binary to grey

code conversion ~

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Experiment - 2
Objective :- Binary to grey code conversion and vice versa.

Components :- • ST2611 Digital circuit Development platform trainer with power supply cord.

- DB06 - code conversion.
- Set of wires.

Theory:- from the previous experiments, we studied that the binary code of data is represented by two values such as 0's and 1's and mainly used in the world of computer. Gray code is a form of binary code that uses a different method of incrementing from one number to the next. With gray code, only one bit changes state from one position to another. This feature allows a system designer to perform some error.

~~Binary to Gray code Conversion~~ :- The following example will be very useful for knowing the conversion of binary to gray code. In this conversion method, take down the MSB of present binary number as the primary bit or MSB bit of the gray code number is similar to the binary number.

To get the straight gray coded bits for generating the corresponding gray coded digit for a given binary digits. do the same thing with the next binary bit and third bit then note down the product bit. The truth table of binary to gray

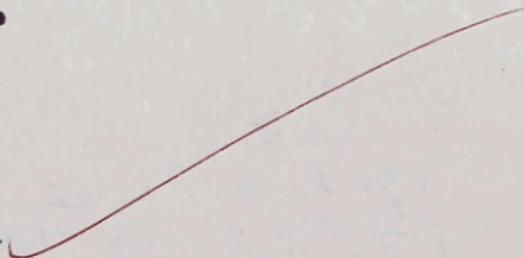
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Code conversion can be seen at Table(1).

gray to binary code conversion:- This gray to binary conversion method also uses the working concept of binary to gray code conversion.

The following concept of ~~binary~~ to ~~gray~~ code To change gray to binary code, take down

the MSB digit of gray code number as primary digit or the MSB of binary digit or the MSB of binary code is similar to the gray code.



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Experiment - 3

Objective :- Implementation of given Boolean function using logic gates in both SOP and POS form.

Two input SOP :- $AB + \bar{A}\bar{B}$

Two input POS :- $(A+B)(B+C)(A+\bar{C})$

Apparatus required :- Digital lab kit, single strand wires, ICS broadbands, connecting wires.

Theory :-

a) SOP :- It is the sum of product form in which the term are taken as 1. It is denoted in the K-map expression by sigma Σ .

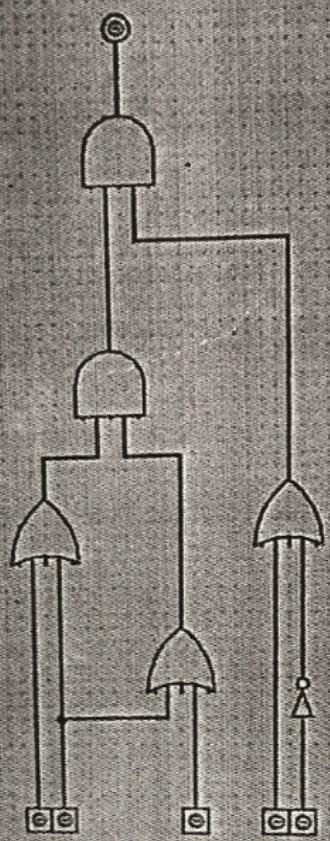
$$AB + \bar{A}\bar{B}$$

Truth table for SOP expression :-

A	B	\bar{A}	\bar{B}	AB	$\bar{A}\bar{B}$	$AB + \bar{A}\bar{B}$
0	0	1	1	0	1	1
0	1	1	0	0	0	0
1	0	0	1	0	0	0
1	1	0	0	1	0	1

b) POS :- It is the product of sum form in which the terms are taken as 0. it is denoted in the K-map expression by the sigma pie (Π).

$$(A+B)(B+C)(A+\bar{C})$$



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Truth table for POS expression:-

A	B	C	$A+B$	$B+C$	$A+\bar{C}$	$(A+B)(B+C)(A+\bar{C})$
0	0	0	0	0	1	0
0	0	1	0	1	0	0
0	1	0	1	1	1	0
0	1	1	1	1	0	1
1	0	0	1	0	1	0
1	0	1	1	1	1	0
1	1	0	1	1	1	1
1	1	1	1	1	1	1

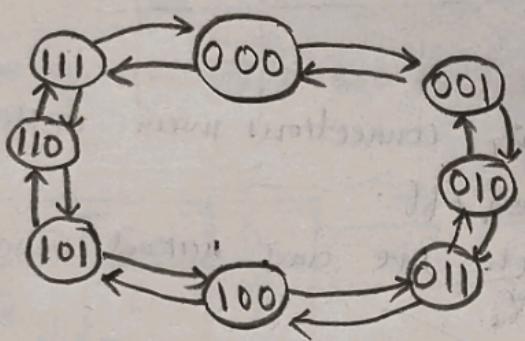
Result:- Hence given boolean expression is implemented by the logic gates.

i) $AB + \bar{A}\bar{B}$

ii) $(A+B)(B+C)(A+\bar{C})$

Precaution:-

- i) connecting wire should be rubbed with sand paper so that there is no rust.
- ii) Make sure the apparatus is switched off while placing IC's and connecting the wires.
- iii) The connection should be tight.



~ State diagram ~

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Experiment -5

Objective:- Design and verify the 4 bit synchronous counter.

Apparatus Used:-

Component	Specification	QTY.
1) JK flip-flop	IC 7476	2
2) 4 I/P AND GATE	IC 7411	1
3) OR GATE	IC 7432	1
4) XOR GATE	IC 7486	1
5) NOT GATE	IC 7404	1
6) IC Trainer kit		1
7) Patch cords		35

Theory:-

Synchronous counter:- A simpler way of implementing the logic for each bit of an ascending counter is for each bit to toggle when all of the less significant bits are at a logic state.

Synchronous counter can also be implemented with hardware finite state machines.

Procedure:-

- i) Connections as per as circuit diagram.
- ii) Logical input are given as per as Ckt diagram.
- iii) observe the output & verify the truth table.

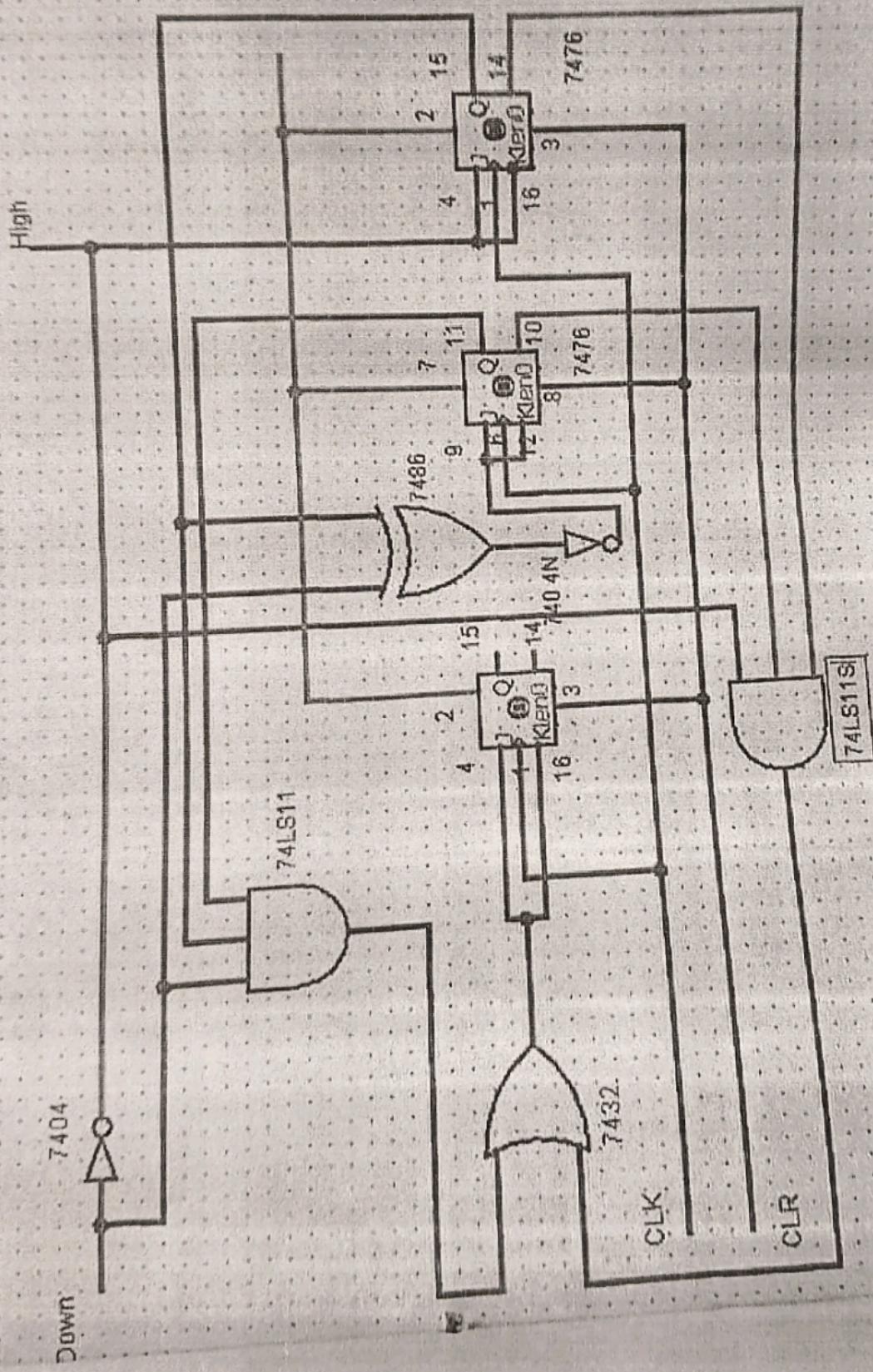
Result:- Study of 4 bit Synchronous counter and verified its truth table.

Precautions:-

- 1) All connections should be tight.

Truth Table:-

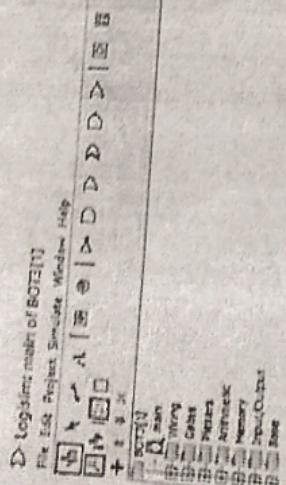
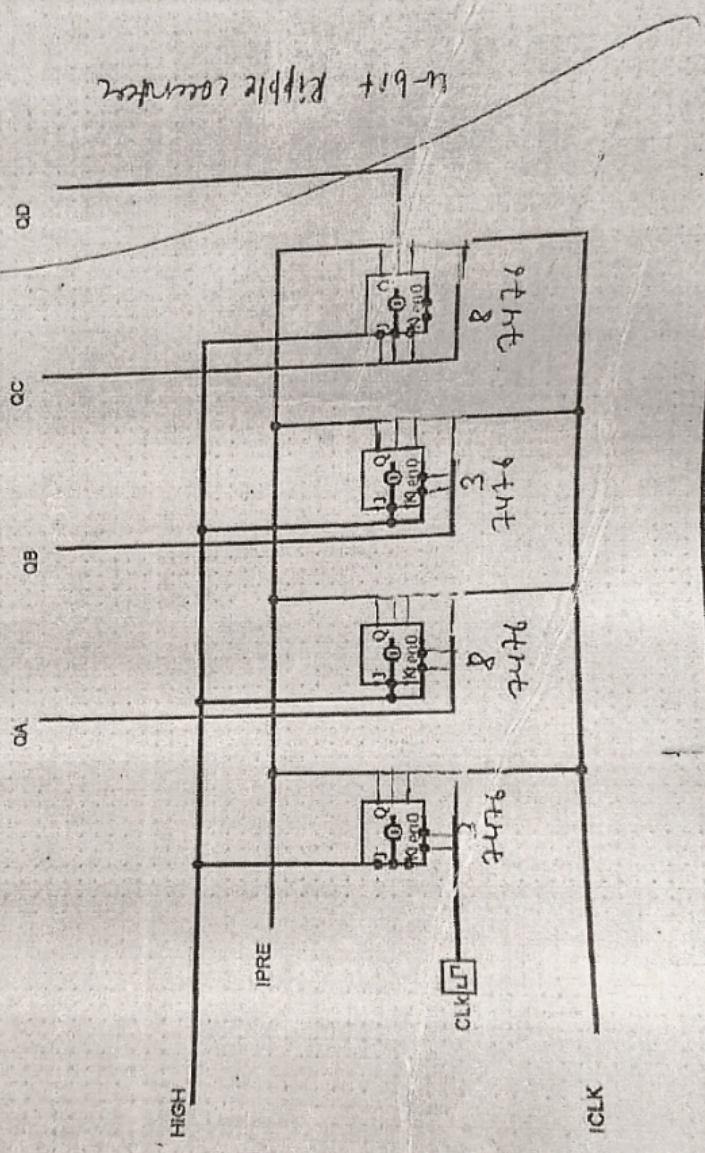
CLK	QA(H)	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	-	0
5	1	0	-	0
6	0	1	-	0
7	1	1	-	0
8	0	0	0	-
9	1	0	0	-
10	0	1	0	-
11	1	1	0	-
12	0	0	1	-
13	1	0	1	-
14	0	1	1	-
15	1	1	1	-



T.C. 7476 (4-bit Asynchronous Counter)

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- 2) All IC's should be checked before starting the experiment.
- 3) Always connect ground first and then connect Vcc.
- 4) The kit should be off before change the connection
- 5) After completion, switch off the supply of the apparatus.



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Experiment - 6

Objective:- To design and verify 4 bit ripple (asynchronous) counter.

Apparatus required:-

component	Specification	QTY
1) JK flip-flop	IC 7476	2
2) NAND GATE	IC 7400	1
3) IC Trainer kit	-	1
4) Patch cords	-	30

Theory:- A counter is a register capable of counting no. of clock pulse arriving at its clock input. Counter represents the no. of clock pulses arrived. In asynchronous first flip-flop is clocked by external pulse and then each successive flip-flop is clocked by Q or Q O/P of previous stage. As soon the clock of second stage is triggered by O/P of first stage because of inherent propagation delay time all flip-flops are not activated at same time which results in asynchronous operation.

Procedure:-

- i) connections are given as per as ckt diagram.
- ii) logical ips are given as per ckt diagram.
- iii) observe the O/P and verify the truth table.

Result:- Study of 4 bit asynchronous counter and verified its truth table.

Precaution:- i) All IC's should be checked before starting the experiment.

ii) Always connect ground first and then connect Vcc.

Characteristics for T-flip-flop:-

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Characteristics of S-R flip-flop:-

Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Intermediate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Intermediate

Characteristics of D-flip-flop:-

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

Characteristics of J-K flip-flop:-

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

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Experiment - 7

Objective:- Verification of state tables of R-S flip-flop, J-K flip-flop, T flip-flop, D flip-flop using NAND & NOR gates.

Apparatus:- IC 7400 (NAND GATE), IC 7402 (NOR GATE), IC 7408 (AND GATE).

Theory:-

Flip-flop:- The basic one bit digital memory ckt is known as flip-flop. It can store either '0' or '1'. Flip-flops are classified according to the no. of inputs.

R-S Flip-flop:- The ckt is similar to SR latch except enable signal is replaced by clock pulse.

D-flip-flop:- The modified clocked SR flip-flop is known as D-flip-flop. From the truth table of SR flip-flop we see that the o/p of SR flip-flop is unpredictable state when the I/P are same and high. In many practical applications, these I/P conditions are not required. These I/P conditions can be avoided by making them complement of each other.

J-K Flip-flop:- In RS-Flip-flop, the I/P R-S leads to an indeterminate o/p. The RS flip-flop ckt may be rejoin. If both I/P are 1 then also o/p are complement of each other.

T-Flip-flop:- It is also known as toggle flip-flop. The T-flip flop is modification of the J-K flip-flop. Both the J-K I/P of the J-K flip-flops are held at logic 1 the clock signal continuously changes.

Precautions:-

- 1) All connections should be tight.
- 2) Always connect ground first and then connect Vcc.