1. (12 pts) Assume ideal diodes, find the diode states for the circuits shown in Figure 1, and calculate the current I and voltage V.

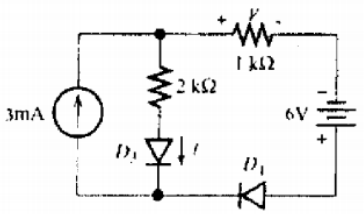


Figure 1

2.For the BJT amplifier circuit shown in Figure 2, where Vc=20V, β=200, $V_{BEQ} = 0.7V$,

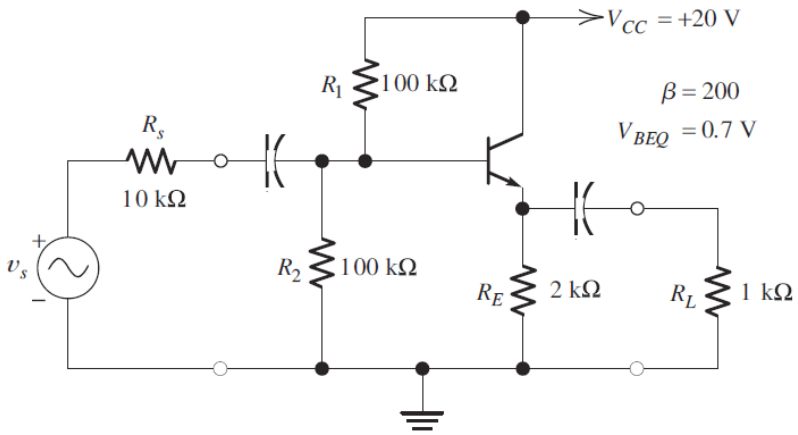
a. Find the value of I_{BQ}, I_{CQ}。

b. Draw the small-signal equivalent circuit of the amplifier.

c. Find the voltage gain.

d. Find the input resistance, r_i .

e. Find the output resistance, r_o.

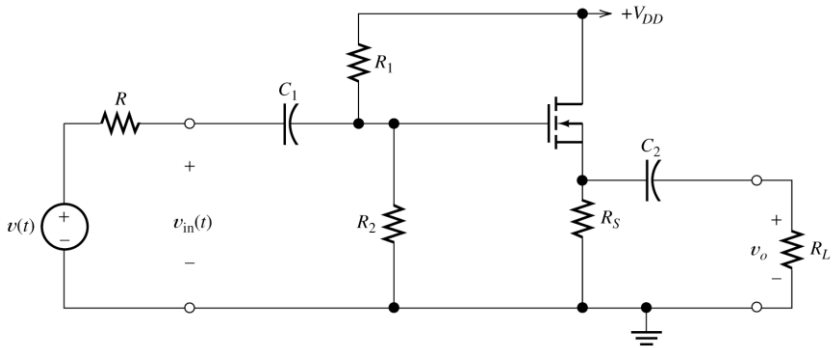


3. The circuit shown in Figure 3 is a common-drain (or source follower) amplifier. The transistor parameters, and component values are: RL = 1 kΩ and R1 = R2 =2 MΩ. KP=50 μA/V^2, V_{to}=1V, L=2 μm, W=160 μm.

a. **Find the value for R_S to achieve I_{DQ} = 10 mA.**

b. **Draw the AC small-signal equivalent circuit.**

c. **Determine the values of the input resistance Ri, the output resistance R0, and voltage gain Av.**



4. The circuit composed of ideal operational amplifiers is shown in Figure 4,

a. Derive the expression of V_0.

b. When $R_1 = R_2 = R_3 = R_f$, V_0=?

c. What is the feedback type of R_f?

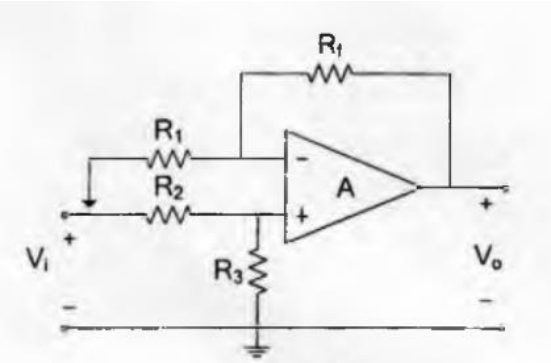


Figure 4

5. (12 pts) The sequential logic circuit and clock signal are shown in Figure 5.

a. List the truth tables of JK flip flop and D flip flop. (6pts)

b. Sketch the Q_0 and Q_1 versus time.(Assuming that Q_0 and Q_1 be "0" at beginning)(6pts)

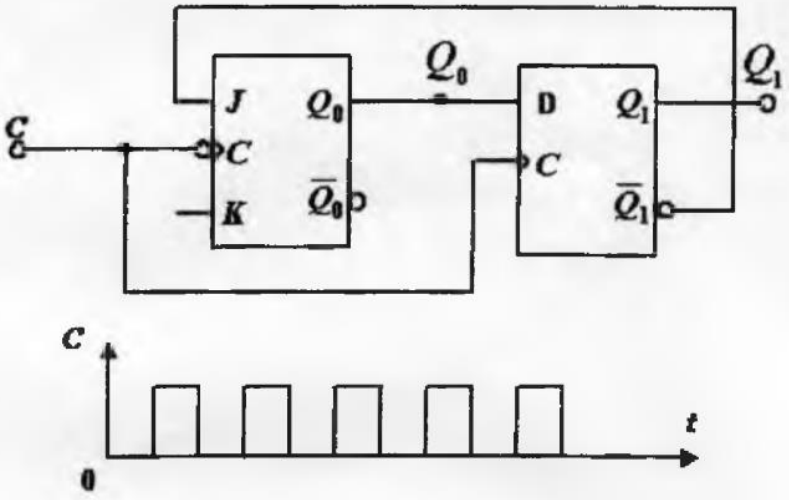


Figure 5

6. (16 pts) The operation rules of three motors A, B and C are as follows: when C is not started up, B can not be started up; when B is not started up, A can not be started up. Design a logic circuit outputs the alarm signal F when operation rules are not obeyed.

a. Let the motor started be 1 and the motor stopped be 0. Let alarm signal appears be 1, otherwise be 0. Construct the truth table of F. (4pts)

b. Write the sum-of-products implementation for F. (4pts)

c. Construct a Karnaugh map for above logic function F and reduce it.(4 pts)

d. Realize the function using AND, OR and NOT gates. (4pts)

7. The differential amplifiers is shown below, where β =50, U_{be} =0.7V, input voltage u_{i1}=6mV, u_{i2}=4mV ,Ucc=6V, Ee=-6V, R_B=10 kΩ , Rc=5 kΩ,R_E=5 kΩ;

a. Find the values of I_{BQ}, I_{CQ}.

b. Decompose $u_{i1}$and $u_{i2}$to common-mode signals $u_{ic1}$and u_{ic2}as well as differential signals $u_{id1}$and u_{id2} .

c. Calculate the single-ended outputs $u_{od1}$and $u_{od2}$for differential signals;

d. If the gain of common mode signal for single-ended outputs is $Ac = -Rc/2R_E$, calculate the single-ended outputs $u_{o1}$and u_{o2};

e. Calculate the common-mode output $u_{oc}$and differential output u_{od}.