

EE-204

Computer Architecture

**PROJECT REPORT**

**General Cache Simulator**

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**Introduction To Project:**

The cache simulator is used in order to simulate substitutions in cache using replacement policies (FIFO and LRU) and write back into the cache (using the write-allocate policy). The idea is to give an input file with commands, trace the results of that input simulating cache functions so that we can keep track of cache hits and misses.

# **Specification:**

# **Input:**

There will be two input files named description and input respectively.

* The description file will consist of details such as block size(unsigned power 2) , total no of blocks(unsigned power 2) and associativity. There are 4 such files depending upon the set associativity which can be either 2-way, 4-way, 8-way or 16-way.
* Where as the input file will consist of address of access and access operation.

# **User Interface:**

1. User will be asked to select a cache description file depending upon the set associativity.
2. Next, the user will be asked to select a replacement policy
3. In the end, user will choose an input file (containing the address of the access and the operation of access i-e read or write) .

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# **Output:**

* Number of access count
* Number of read hits
* Number of read misses
* Number of write hits
* Number of write misses

# **Working of the project:**

Cache is a class that contains four informations:

* Cache\_Data
* Upper\_Data (used as a tag in the set)
* Time\_Access (used in the LRU algorithm)
* Time\_Load (used in the FIFO algorithm)

These informations are modeled as a dynamic array 2-D which contains the following positions:

* Set (number\_of\_lines / associativity)
* Line (associativity)

To access data in the cache, the only thing that is necessary is the set, which is the information about "index" in an address. To access the line is used , an "upper" information. The upper is used only for comparisons to know which line (block) should be accessed because the set doesn't have any particular order.

Given access addresses and access operations , the simulator will check for a hit or a miss . Incase of a miss the user selected replacement policy will be applied . Once all the access are made , it will return the total misses and hits (read and write both) .

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# **Achieved result**

# **2-way Associativity with 64 KB cache size and 2^4B block size**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Access counts** | **Read hits** | **Read misses** | **Write hits** | **Write misses** | **FIFO Time** | **LRU time** |
| **Input 1** | 87 | 5 | 59 | 13 | 10 | 0.0001 | 0.000 |
| **Input 2** | 248 | 41 | 124 | 34 | 85 | 0.003 | 0.002 |
| **Input 3** | 463 | 30 | 276 | 37 | 120 | 0.003 | 0.003 |
| **Input 4** | 994 | 27 | 456 | 34 | 477 | 0.009 | 0.006 |

# **4-way Associativity with 16 KB cache size and 2^11 B block size**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Access counts** | **Read hits** | **Read misses** | **Write hits** | **Write misses** | **FIFO Time** | **LRU time** |
| **Input 1** | 87 | 26 | 38 | 9 | 14 | 0.000 | 0.000 |
| **Input 2** | 284 | 112 | 53 | 103 | 16 | 0.001 | 0.001 |
| **Input 3** | 463 | 184 | 122 | 101 | 56 | 0.003 | 0.003 |
| **Input 4** | 994 | 344 | 139 | 302 | 209 | 0.006 | 0.0013  333333 |

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# **8-way Associativity with 64 KB cache size and 2^9 B block size**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Access counts** | **Read hits** | **Read misses** | **Write hits** | **Write misses** | **FIFO Time** | **LRU time** |
| **Input 1** | 87 | 50 | 14 | 16 | 7 | 0.000 | 0.00 |
| **Input 2** | 284 | 134 | 31 | 116 | 3 | 0.0012 | 0.001 |
| **Input 3** | 463 | 254 | 52 | 132 | 25 | 0.006 | 0.005 |
| **Input 4** | 994 | 421 | 62 | 444 | 67 | 0.02 | 0.009 |

# **16-way Associativity with 32KB Block size and 2^10B total no of blocks**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Access counts** | **Read hits** | **Read misses** | **Write hits** | **Write misses** | **FIFO Time** | **LRU time** |
| **Input 1** | 87 | 43 | 21 | 14 | 9 | 0.001 | 0.000 |
| **Input 2** | 284 | 122 | 43 | 122 | 7 | 0.004 | 0.002 |
| **Input 3** | 463 | 229 | 77 | 122 | 35 | 0.008 | 0.006 |
| **Input 4** | 994 | 393 | 90 | 397 | 144 | 0.009 | 0.008 |

# **Conclusion :**

This simulator helps in keeping track of cache hits and misses on different access using write allocate policy . This project concludes that we can use any of the above mentioned replacement policies incase of a miss . Also different set associativity give different hits and misses , there is also difference in the mapping of the cache .