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1. The narious members of the 8051 family baced on this Rom are:

a) 8031 - No Rom

b) 80xx - Mask, ROM

c) 87xx. - EPROM

- d) 89xx Flash EEPROM (Example: AT89C51, ATE9LV51, AT89S51)
- 3-bit microcontrollers. 8031/80C31 have the came integrated puriphicals as 8051 MCUS 4 I/O posts, two 16-bit timess/counterly of counters, on-chip oscillator and a cerial post. The MCUS have 188 keytes of internal RAM, and, in addition to that, can utilize upto 04KB of external data memory. The micro-controllers don't have on-chip ROM and must use external pregram memory.
- -) 8051: It has 188 bytes of RAM, 4KB of on-elrip ROM, two 16 bit times counters, our cesial post, six intersupt sources, 8-bit ALV and 4 posts of 8 bits each. It has a Hanard Memory Anchitecture i.e., it has 16 bit Address bus (each of RAM and ROM) and 8-bit data bus.
- + 8052: This microcontroller has 256 bytes of RAM and 3 times. In addition to the standard features of 8051, the microcontroller has an added 128 bytes of RAM and a times. It has one serial post and 8 interrupt sources
- 3 8751: This mics occurt roller u the UV-EPROM sussion of 8051.

  This chip has only UK bytes of UV-EPROM. Its required to have access to the PROM bushes and the UV-EPROM esases to erase the contents of the chip before its programmed again.



HT89C51: Its an 8-bit microcontroller from the Atmelifamily. Its the feash Rommersion of 8051. Its a uppin IC package with 4KB flash memory. It has four ports and they altegether provide 32 programmable GPIO pins.

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-) ATRACES : Its am 8-bit CMOS microcontroller from 8051

Jamily of Atmul microcontrollers. It has 8k flash

minory and 256 bytes of RAM. It has 32 I/O pins

comprising of three 1b-bit times, external interrupt,

full-duffer arrial fort, on chip esculator and clock

circuitsy.

The comparison charit of 8051 family members is as follows:

								1
-	8051 family	ROM	RAM	Times	Int	Eopin	Other	
	8031	o'K	128	2	. 6	32		
	8051	- UK	188	2	6	. 32	_	
	8052	8K	256	- 430	8.	32		1
	8953	12K	a56	1 13 113	19	32	WD	
	8955	ZOK	256	3	8	32	WD	
	898252	* & K	12561	11,3:11	19	32	ISP	
	891051	-1K	64	11300	3	. 16	AC	
	892051	2K	128	a	16.11	16 m	AC	
		, ,			14	1		

WD: Water Dog Timer

Ac: Analog comparator

ISP: In System Programable

		CLASCALACE				
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		111 11/6				
Ans 2	PLOTI WE VE	de del col beller de de cons				
	PI 1 - 8 14- 10.0 (ADD)	the same of the sa				
	P1.2-3 (10)	11.				
	P1.3 4. =1-P0.2(AD2)					
	Plu 6 36 - PO.3(AD')	,				
	PIS O SE POU (ADM)	the state of the s				
	916-7 34-005/ADS)					
	P1-7-10 (ADC)					
	RST-9. 22- PO.7 (ADT)					
	(RXD) PBC -10 8051 91-EA/VPP					
	(TXO)P2.1-11 20 ALE/PROG					
******	(INTO) 13.2 -12 29 FSEN					
	(10) P3.13 - 13, 12 - 14 - 20 - P2.7 (AIC)					
	(11) P3.4 - 14 27 - P2.6 (AIM) (11) P3.5 - 15 26 - P2.5 (AIX)					
	(WR) P3-6	21 1 11 1 2				
	(RD) P3.7 -17 24-P2.3 (AII)	attaches de les				
	YTAL2-18 23-P2.2 (A10)  YTAL1-19 22-P2.1 (A01)					
	GND-20 21 - P2.0/A8)					
	Pin Diagram of 8051 microcontro	ller				
4	Pin Diagram of 8051 microcontroller The pin descriptions are as follows:					
	Pins 1-8 (Post 1): Pins 1+08 are PORT 1 pins					
	aired an willful a trit hidis portional in out I pu	that below 54				
	pins consists of 8-bit bedisectional input / ou	ipm post wan				
1.4	internal pull- up xillstors.					
146	internal pull-up suistors.	11 10				
•	Pin 9 (RST): Pin 9 is the Reset input Pin. I	s an active				
-	bign pin i.e. if the RST pin & high for a	minimum				
,	of the machine cycles, the microcontrolle	r will be				
	The water age of the phone of	i cet to non7				
	resetie, all pens are set to 0000, SPE	s 2011000)				
	and the RAM content becomes zero.					
	The state of the s					
• 3	Pine in -17 [Post S]: rivis 10 to 17 Joseph the Pol	RT 3 pins of the				
	Pins 10-17 (Post 3): Pins 10 to 17 form the PORT 3 pins of th					
	8051 microconstroller. Post 3 also acts as a biolisectional input/eutput pest with internal pur-ups. Additional					
	input / eutput part with market pun ups.	, and				
		(a AV 9)				

## the Port 3 has some special functions:

Post 3 Pin	Function	Description
P3.0	RXD	serial Input
P3.1	TXD	Serial output
P3. 2	TNTO	External Interrupt o
P3.3	INT1	External Interrupt 1
P3.4	70	Timero
P3.5	71	Timer 1
P3.6	WR	External munory write
P3-7	RD	External memory read

- · Pins 18419: Pins 18 and 19 on XTAL2 and XTAL i.e., the pins for connecting external oscillator using a quartz chystal oscillator or a TTL oscillator.
- · Pin 20 (GND): Pin 20 is the ground Pin of 8051 microcontroller. It represents DV and is connected to the negative terminal of the power supply:
- · Pins 31-38 (Post 2): These are the post 2 pins of 8051.

  Its area a bidirectional port i.e., all the post 2 pins act as input or output. Additionally, when external memory is interfaced, Post 2 pins acts as the higher order address byte. Post 2 pins have internal pull-ups.
- fin 29 (PSEN): Pin 29 is the program store enable pin CPSEN). It operates on active low signal. Using this fin, external program memory can be seed. Its generally connected to the DE pin of the ROM.



- o lin 30 (ALE/PROG): Pin 30 is the Address laten Enable Pin. It exerates on active night pin. Using this pin, external address can be deparated from data (as they are multiplexed by Port 0 of 2051). During Frash Programming, this pin acts as program pulse input (PROG).
  - · Pin 3t (EA/VPP): Pin 31 is the External Access Enable Pin i.e., it allows external Program Memory. Code from the external program memory can be fetched only if this pin is low. For normal operations, this pin to pulled HIGH.
- · Pins 32-39 (Post 0): Pins 32-39 are Post o pins. They are also bidisectional I/O pins but without any internal pull-ups in order to use Post o pins as I/O post.

In addition to acting as I/O post, Post o also acts as lower order address / data bus when external memory is accessed.

· Pin 40 (Vcc): Pin 40 is the pourer supply pin to which the supply noltage is given (+5v).

The compatibility is the property of the contract of the contr



Given, EPROM = 32K i.e.,  $2^{10} \times 2^5 = 2^{15} = 15$  address lines (10 Am)

RAM = 16K i.e.,  $2^{10} \times 2^4 = 2^{14} = 14$  address lines (10 Am)

Post o is used as multiplexed data and address lines.

WR and RD of RAM are connected to P3.6 and P3.7 of 805).

PSEN is connected to OE of the EPROM

EA is low to enable external EPROM and RAM

	y Lakyhares	4	, Vice	11Un 9	Ycc	
	e famorii :	L I o dia v	V. 100 - 0	111111111111111111111111111111111111111	147	
1	PO.7		and the same of th		Dy - Do	
1	P.O. O		D7 - D0	,		
		7415373	A7-A0		A7-A0	
	ALE	G OC .	1-11, 1-11	. ' 1	11-1	
	8051	. + ) = 11 +	32K EPROM	111 11	16K.RAM	
	P2.0		AE-A14 .		AsTAIS	
ì	PSEN	P.O. 11 1. 2 111	OE OE	P2.6-0	CS (AIM)	
	P3.6		ĊS		RD WR	
	P2.7	THE THE PERSON NAMED IN	Admirate state property and the		1.15	
		1 161 11/11 11	and the same of the same of the same	transfer to the transfer		

Memory interface ciscuit diagram for interfacing 32K EPROM and lok RAM with 8051 microcontrolla