

a-Si TFT LCD Single Chip Driver 240RGBx320 Resolution and 262K Color Datasheet

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1. Introduction

ILI9325D is a 262,144-color one-chip SoC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes RAM for graphic data of 240RGBx320 dots, and power supply circuit.

ILI9325D has four kinds of transmission interfaces which are i80-system MPU interface (8-/9-/16-/18-bit bus width), VSYNC interface (system interface + VSYNC, internal clock, DB[17:0]), serial data transfer interface (SPI), RGB 6-/16-/18-bit interface (DOTCLK, VSYNC, HSYNC, ENABLE, DB[17:0]).

In RGB interface and VSYNC interface mode, the combined use of high-speed RAM write function and widow address function enables to display a moving picture at a position specified by a user and still pictures in other areas on the screen simultaneously, which makes it possible to transfer display the refresh data only to minimize data transfers and power consumption.

ILI9325D can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The ILI9325D also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the ILI9325D an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, PDA and PMP where long battery life is a major concern.

2. Features

- ◆ Single chip solution for a liquid crystal QVGA TFT LCD display
- ◆ 240RGBx320-dot resolution capable with real 262,144 display color
- ◆ Support MVA (Multi-domain Vertical Alignment) wide view display
- ◆ Incorporate 720-channel source driver and 320-channel gate driver
- ◆ Internal 172,800 bytes graphic RAM
- ◆ CABBC (Content Adaptive Brightness Control)
- ◆ System interfaces
 - i80 system interface with 8-/9-/16-/18-bit bus width
 - Serial Peripheral Interface (SPI)
 - RGB interface with 6-/16-/18-bit bus width (VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0])
 - VSYNC interface (System interface + VSYNC)
- ◆ Internal oscillator and hardware reset
- ◆ Reversible source/gate driver shift direction
- ◆ Window address function to specify a rectangular area for internal GRAM access
- ◆ Abundant functions for color display control
 - γ -correction function enabling display in 262,144 colors
 - Line-unit vertical scrolling function
- ◆ Partial drive function, enabling partially driving an LCD panel at positions specified by user
- ◆ Incorporate step-up circuits for stepping up a liquid crystal drive voltage level up to 6 times (x6)
- ◆ Power saving functions
 - 8-color mode
 - standby mode
 - sleep mode
- ◆ Low -power consumption architecture
 - Low operating power supplies:
 - IOVCC = 1.65V ~ 3.3 V (interface I/O)
 - VCI = 2.5V ~ 3.3 V (analog)
- ◆ LCD Voltage drive:
 - Source/VCOM power supply voltage
 - DDVDH - GND = 4.5V ~ 6.0
 - VCL - GND = -2.0V ~ -3.0V
 - VCI - VCL \leq 6.0V
 - Gate driver output voltage
 - VGH - GND = 10V ~ 20V
 - VGL - GND = -5V ~ -15V
 - VGH - VGL \leq 30V
 - VCOM driver output voltage
 - VCOMH = (VCI+0.2)V ~ (DDVDH-0.2)V

- $V_{COML} = (V_{CL} + 0.2)V \sim 0V$
- $V_{COMH} - V_{COML} \leq 6.0V$
- ◆ a-TFT LCD storage capacitor: Cst only

4. Pin Descriptions

Pin Name	I/O	Type	Descriptions																																																																														
Input Interface																																																																																	
IM3, IM2, IM1, IM0/ID	I	IOVCC	Select the MPU system interface mode																																																																														
			<table><tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU-Interface Mode</th><th>DB Pin in use</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting invalid</td><td></td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting invalid</td><td></td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>i80-system 16-bit interface</td><td>DB[17:10], DB[8:1]</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>i80-system 8-bit interface</td><td>DB[17:10]</td></tr><tr><td>0</td><td>1</td><td>0</td><td>ID</td><td>Serial Peripheral Interface (SPI)</td><td>SDI, SDO</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>9-bit 3 wires Serial Peripheral Interface</td><td>SDA, SCL, nCS</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>8-bit 4 wires Serial Peripheral Interface</td><td>SDA, SCL, nCS, RS (D/CX)</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting invalid</td><td></td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting invalid</td><td></td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>i80-system 18-bit interface</td><td>DB[17:0]</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>i80-system 9-bit interface</td><td>DB[17:9]</td></tr><tr><td>1</td><td>1</td><td>*</td><td>*</td><td>Setting invalid</td><td></td></tr></table>	IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use	0	0	0	0	Setting invalid		0	0	0	1	Setting invalid		0	0	1	0	i80-system 16-bit interface	DB[17:10], DB[8:1]	0	0	1	1	i80-system 8-bit interface	DB[17:10]	0	1	0	ID	Serial Peripheral Interface (SPI)	SDI, SDO	0	1	1	0	9-bit 3 wires Serial Peripheral Interface	SDA, SCL, nCS	0	1	1	1	8-bit 4 wires Serial Peripheral Interface	SDA, SCL, nCS, RS (D/CX)	1	0	0	0	Setting invalid		1	0	0	1	Setting invalid		1	0	1	0	i80-system 18-bit interface	DB[17:0]	1	0	1	1	i80-system 9-bit interface	DB[17:9]	1	1	*	*	Setting invalid	
			IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use																																																																									
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1	1	*	*	Setting invalid																																																																													
When the serial peripheral interface is selected, IM0 pin is used for the device code ID setting.																																																																																	
nCS	I	MPU IOVCC	A chip select signal. Low: the ILI9325D is selected and accessible High: the ILI9325D is not selected and not accessible Fix to the GND level when not in use.																																																																														
RS	I	MPU IOVCC	A register select signal. Low: select an index or status register High: select a control register Fix to either IOVCC or GND level when not in use.																																																																														
nWR/SCL	I	MPU IOVCC	A write strobe signal and enables an operation to write data when the signal is low. Fix to either IOVCC or GND level when not in use. SPI Mode: Synchronizing clock signal in SPI mode.																																																																														
nRD	I	MPU IOVCC	A read strobe signal and enables an operation to read out data when the signal is low. Fix to either IOVcc or GND level when not in use.																																																																														
nRESET	I	MPU IOVCC	A reset pin. Initializes the ILI9325D with a low input. Be sure to execute a power-on reset after supplying power.																																																																														
SDI / SDA	I/O	MPU IOVcc	SPI interface input pin. The data is latched on the rising edge of the SCL signal. In the 8/9-bit serial peripheral interface, this pin is used as bi-directional data pin.																																																																														
SDO	O	MPU IOVCC	SPI interface output pin. The data is outputted on the falling edge of the SCL signal. Let SDO as floating when not used.																																																																														
DB[17:0]	I/O	MPU IOVCC	An 18-bit parallel bi-directional data bus for MPU system interface mode 8-bit I/F: DB[17:10] is used.																																																																														

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Pin Name	I/O	Type	Descriptions
			9-bit I/F: DB[17:9] is used. 16-bit I/F: DB[17:10] and DB[8:1] is used. 18-bit I/F: DB[17:0] is used. 18-bit parallel bi-directional data bus for RGB interface operation 6-bit RGB I/F: DB[17:12] are used. 16-bit RGB I/F: DB[17:13] and DB[11:1] are used. 18-bit RGB I/F: DB[17:0] are used. Unused pins must be fixed to GND level.
ENABLE	I	MPU IOVCC	Data ENEABLE signal for RGB interface operation. Low: Select (access enabled) High: Not select (access inhibited) The EPL bit inverts the polarity of the ENABLE signal. Fix to either IOVCC or GND level when not in use.
DOTCLK	I	MPU IOVCC	Dot clock signal for RGB interface operation. DPL = "0": Input data on the rising edge of DOTCLK DPL = "1": Input data on the falling edge of DOTCLK Fix to the GND level when not in use
VSYNC	I	MPU IOVCC	Frame synchronizing signal for RGB interface operation. VSPL = "0": Active low. VSPL = "1": Active high. Fix to the GND level when not in use.
HSYNC	I	MPU IOVCC	Line synchronizing signal for RGB interface operation. HSPL = "0": Active low. HSPL = "1": Active high. Fix to the GND level when not in use
FMARK	O	MPU IOVCC	Output a frame head pulse signal. The FMARK signal is used when writing RAM data in synchronization with frame. Leave the pin open when not in use.
LEDPWM/ TESTO1	O	VCI	PWM signal output to control LED driver for LED brightness dimming.
LEDON/ TESTO2	O	VCI	This pin is connected to external LED driver. It's a LED driver control pin which is used for turning ON/OFF of LED backlight.
LCD Driving signals			
S720~S1	O	LCD	Source output voltage signals applied to liquid crystal. To change the shift direction of signal outputs, use the SS bit. SS = "0", the data in the RAM address "h00000" is output from S1. SS = "1", the data in the RAM address "h00000" is output from S720. S1, S4, S7, ... display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9, ... display blue (B) (SS = 0).
G320~G1	O	LCD	Gate line output signals. VGH: the level selecting gate lines VGL: the level not selecting gate lines
VCOM	O	TFT common electrode	A supply voltage to the common electrode of TFT panel. VCOM is AC voltage alternating signal between the VCOMH and VCOML levels. Adjust the VCOM amplitude with the VDV bits.
VCOMH	O	-	The high level of VCOM AC voltage.
VCOML	O	-	The low level of VCOM AC voltage.
VGS	I	GND or external resistor	Reference level for the grayscale voltage generating circuit. The VGS level can be changed by connecting to an external resistor.
Charge-pump and Regulator Circuit			

Pin Name	I/O	Type	Descriptions
VCI	I	Power supply	A supply voltage to the analog circuit. Connect to an external power supply of 2.5 ~ 3.3V.
GND	I	Power supply	GND for the analog side: GND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
VCI1	O	-	An internal reference voltage for the step-up circuit1. The amplitude between VCI1 and GND is determined by the VC[2:0] bits. Make sure to set the VCI1 voltage so that the DDVDH, VGH and VGL voltages are set within the respective specification.
DDVDH	O	Stabilizing capacitor	Power supply for the source driver and VCOM drive.
VGH	O	Stabilizing capacitor	Power supply for the gate driver.
VGL	O	Stabilizing capacitor	Power supply for the gate driver.
VCL	O	Stabilizing capacitor	VCOML driver power supply. VCL = 0.5 ~ -VCI. Place a stabilizing capacitor between GND
C11+, C11-	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 1.
C13+, C13- C21+, C21- C22+, C22-	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 2.
VREG1OUT	I/O	Stabilizing capacitor	Output voltage generated from the reference voltage. The voltage level is set with the VRH bits. VREG1OUT is (1) a source driver grayscale reference voltage, (2) VCOMH level reference voltage, and (3) VCOM amplitude reference voltage. Connect to a stabilizing capacitor. VREG1OUT = 3.0 ~ (DDVDH - 0.2)V.
Power Pads			
IOVCC	I	Power supply	A supply voltage to the interface pins: IM[3:0], nRESET, nCS, nWR, nRD, RS, DB[17:0], VSYNC, HSYNC, DOTCLK, ENABLE, SCL, SDI, SDO. IOVCC = 1.65 ~ 3.3V and VCI ≥ IOVcc. In case of COG, connect to VCI on the FPC if IOVCC=VCI, to prevent noise.
VDDD	O	Step-up capacitor	Digital circuit power pad. Connect these pins with the 1uF capacitor.
GND	I	Power supply	GND = 0V.
Test Pads			
DUMMY3~15 DUMMY20~27	-	-	Dummy pad. Leave these pins as open.
TEST_EN	I	IOGND	Test pins (internal pull low). Connect to GND or leave these pins as open.
TEST1, 2, 3	I	IOGND	Test pins (internal pull low). Connect to GND or leave these pins as open.
TS0~8	I	OPEN	Test pins (internal pull low). Leave them open.
IOGNDDUM	O	GND	GND pin.
TSO	O	OPEN	Test pins. Leave them open.
TESTO1~16	O	Open	Test pins. Leave them open.

Liquid crystal power supply specifications Table 1

No.	Item		Description
1	TFT Source Driver		720 pins (240 x RGB)
2	TFT Gate Driver		320 pins
3	TFT Display's Capacitor Structure		Cst structure only (Common VCOM)
4	Liquid Crystal Drive Output	S1 ~ S720	V0 ~ V63 grayscales
		G1 ~ G320	VGH - VGL
		VCOM	VCOMH - VCOML: Amplitude = electronic volumes
5	Input Voltage	IOVCC	1.65 ~ 3.30V
		VCI	2.50 ~ 3.30V
6	Liquid Crystal Drive Voltages	DDVDH	4.5V ~ 6.0V
		VGH	10V ~ 20V
		VGL	-5V ~ -15V
		VCL	-1.9V ~ -3.0V
		VGH - VGL	Max. 30V
		VCI - VCL	Max. 6.0V
7	Internal Step-up Circuits	DDVDH	VCI1 x2
		VGH	VCI1 x4, x5, x6
		VGL	VCI1 x-3, x-4, x-5
		VCL	VCI1 x-1

5. Pad Arrangement and Coordination

Chip Size: 17820um x 700um

Chip thickness : 280um (typ.)

Pad Location: Pad Center.

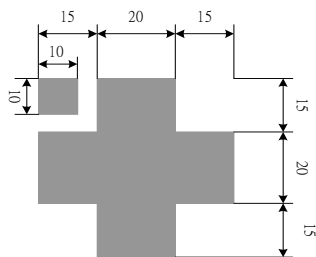
Coordinate Origin: Chip center

Au bump height: 12um (typ.)

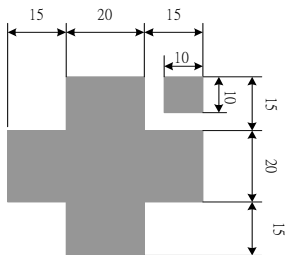
Au Bump Size:

1. 16um x 98um
Gate: G1 ~ G320
Source: S1 ~ S720
2. 50um x 80um
Input Pads
Pad 1 to 243.

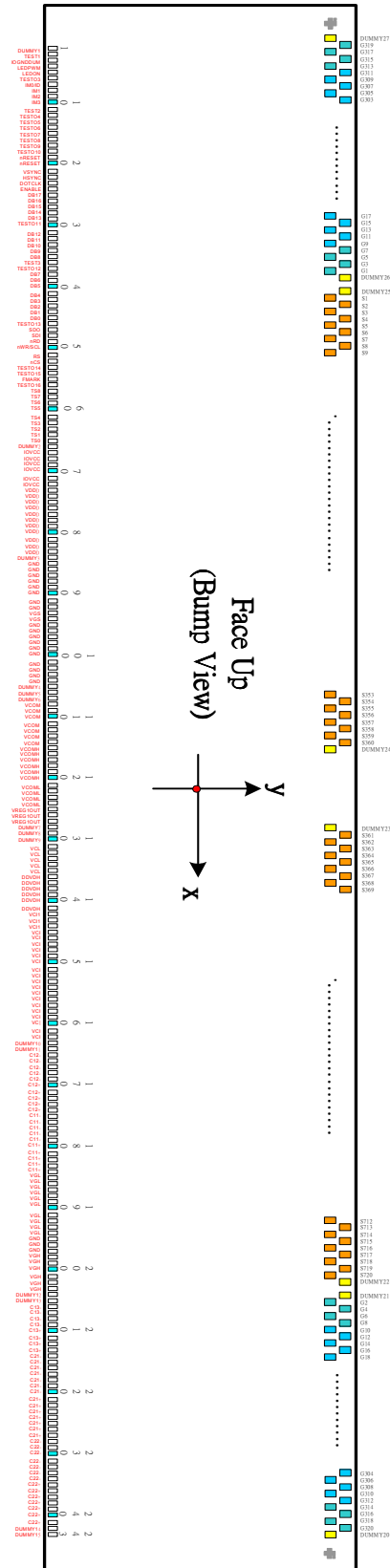
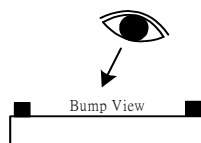
Alignment Marks



Alignment Mark: A1



Alignment Mark: A2



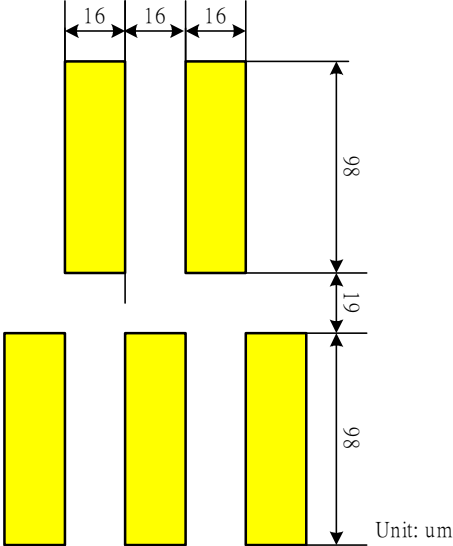
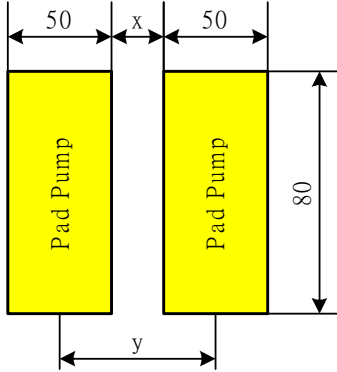
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	TEST EN	-8610	-254	61	TS4	-4130	-254	121	VCOML	70	-254	181	C11+	4270	-254	241	C22+	8470	-254
2	TEST1	-8540	-254	62	TS3	-4060	-254	122	VCOML	140	-254	182	C11+	4340	-254	242	DUMMY14	8540	-254
3	IOGNDDUM	-8470	-254	63	TS2	-3990	-254	123	VCOML	210	-254	183	C11+	4410	-254	243	DUMMY15	8610	-254
4	LEDPWM / TESTO1	-8400	-254	64	TS1	-3920	-254	124	VCOML	280	-254	184	C11+	4480	-254	244	DUMMY20	8659	128
5	LEDON / TESTO2	-8330	-254	65	TS0	-3850	-254	125	VREG1OUT	350	-254	185	VGL	4550	-254	245	G320	8643	245
6	TESTO3	-8260	-254	66	TS0	-3780	-254	126	VREG1OUT	420	-254	186	VGL	4620	-254	246	G318	8627	128
7	IM0/ID	-8190	-254	67	IOVCC	-3710	-254	127	VREG1OUT	490	-254	187	VGL	4690	-254	247	G316	8611	245
8	IM1	-8120	-254	68	IOVCC	-3640	-254	128	DUMMY7	560	-254	188	VGL	4760	-254	248	G314	8595	128
9	IM2	-8050	-254	69	IOVCC	-3570	-254	129	DUMMY8	630	-254	189	VGL	4830	-254	249	G312	8579	245
10	IM3	-7980	-254	70	IOVCC	-3500	-254	130	DUMMY9	700	-254	190	VGL	4900	-254	250	G310	8563	128
11	TEST2	-7910	-254	71	IOVCC	-3430	-254	131	VCL	770	-254	191	VGL	4970	-254	251	G308	8547	245
12	TESTO4	-7840	-254	72	IOVCC	-3360	-254	132	VCL	840	-254	192	VGL	5040	-254	252	G306	8531	128
13	TESTO5	-7770	-254	73	VDDD	-3290	-254	133	VCL	910	-254	193	VGL	5110	-254	253	G304	8515	245
14	TESTO6	-7700	-254	74	VDDD	-3220	-254	134	VCL	980	-254	194	VGL	5180	-254	254	G302	8499	128
15	TESTO7	-7630	-254	75	VDDD	-3150	-254	135	VCL	1050	-254	195	GND	5250	-254	255	G300	8483	245
16	TESTO8	-7560	-254	76	VDDD	-3080	-254	136	DDVDH	1120	-254	196	GND	5320	-254	256	G298	8467	128
17	TESTO9	-7490	-254	77	VDDD	-3010	-254	137	DDVDH	1190	-254	197	GND	5390	-254	257	G296	8451	245
18	TESTO10	-7420	-254	78	VDDD	-2940	-254	138	DDVDH	1260	-254	198	VGH	5460	-254	258	G294	8435	128
19	nRESET	-7350	-254	79	VDDD	-2870	-254	139	DDVDH	1330	-254	199	VGH	5530	-254	259	G292	8419	245
20	nRESET	-7280	-254	80	VDDD	-2800	-254	140	DDVDH	1400	-254	200	VGH	5600	-254	260	G290	8403	128
21	VSYSN	-7210	-254	81	VDDD	-2730	-254	141	DDVDH	1470	-254	201	VGH	5670	-254	261	G288	8387	245
22	HSYSN	-7140	-254	82	VDDD	-2660	-254	142	VCI1	1540	-254	202	VGH	5740	-254	262	G286	8371	128
23	DOTCLK	-7070	-254	83	VDDD	-2590	-254	143	VCI1	1610	-254	203	VGH	5810	-254	263	G284	8355	245
24	ENABLE	-7000	-254	84	DUMMY3	-2520	-254	144	VCI1	1680	-254	204	DUMMY12	5880	-254	264	G282	8339	128
25	DB17	-6905	-254	85	GND	-2450	-254	145	VCI	1750	-254	205	DUMMY13	5950	-254	265	G280	8323	245
26	DB16	-6825	-254	86	GND	-2380	-254	146	VCI	1820	-254	206	C13-	6020	-254	266	G278	8307	128
27	DB15	-6745	-254	87	GND	-2310	-254	147	VCI	1890	-254	207	C13-	6090	-254	267	G276	8291	245
28	DB14	-6665	-254	88	GND	-2240	-254	148	VCI	1960	-254	208	C13-	6160	-254	268	G274	8275	128
29	DB13	-6585	-254	89	GND	-2170	-254	149	VCI	2030	-254	209	C13-	6230	-254	269	G272	8259	245
30	TESTO11	-6495	-254	90	GND	-2100	-254	150	VCI	2100	-254	210	C13+	6300	-254	270	G270	8243	128
31	DB12	-6405	-254	91	GND	-2030	-254	151	VCI	2170	-254	211	C13+	6370	-254	271	G268	8227	245
32	DB11	-6325	-254	92	GND	-1960	-254	152	VCI	2240	-254	212	C13+	6440	-254	272	G266	8211	128
33	DB10	-6245	-254	93	VGS	-1890	-254	153	VCI	2310	-254	213	C13+	6510	-254	273	G264	8195	245
34	DB9	-6165	-254	94	VGS	-1820	-254	154	VCI	2380	-254	214	C21-	6580	-254	274	G262	8179	128
35	DB8	-6085	-254	95	GND	-1750	-254	155	VCI	2450	-254	215	C21-	6650	-254	275	G260	8163	245
36	TEST3	-5990	-254	96	GND	-1680	-254	156	VCI	2520	-254	216	C21-	6720	-254	276	G258	8147	128
37	TESTO12	-5920	-254	97	GND	-1610	-254	157	VCI	2590	-254	217	C21-	6790	-254	277	G256	8131	245
38	DB7	-5825	-254	98	GND	-1540	-254	158	VCI	2660	-254	218	C21-	6860	-254	278	G254	8115	128
39	DB6	-5745	-254	99	GND	-1470	-254	159	VCI	2730	-254	219	C21-	6930	-254	279	G252	8099	245
40	DB5	-5665	-254	100	GND	-1400	-254	160	VCI	2800	-254	220	C21-	7000	-254	280	G250	8083	128
41	DB4	-5585	-254	101	GND	-1330	-254	161	VCI	2870	-254	221	C21+	7070	-254	281	G248	8067	245
42	DB3	-5505	-254	102	GND	-1260	-254	162	VCI	2940	-254	222	C21+	7140	-254	282	G246	8051	128
43	DB2	-5425	-254	103	GND	-1190	-254	163	DUMMY10	3010	-254	223	C21+	7210	-254	283	G244	8035	245
44	DB1	-5345	-254	104	GND	-1120	-254	164	DUMMY11	3080	-254	224	C21+	7280	-254	284	G242	8019	128
45	DB0	-5265	-254	105	DUMMY4	-1050	-254	165	C12-	3150	-254	225	C21+	7350	-254	285	G240	8003	245
46	TESTO13	-5180	-254	106	DUMMY5	-980	-254	166	C12-	3220	-254	226	C21+	7420	-254	286	G238	7987	128
47	SDO	-5110	-254	107	DUMMY6	-910	-254	167	C12-	3290	-254	227	C21+	7490	-254	287	G236	7971	245
48	SDI	-5040	-254	108	VCOM	-840	-254	168	C12-	3360	-254	228	C22-	7560	-254	288	G234	7955	128
49	nRD	-4970	-254	109	VCOM	-770	-254	169	C12-	3430	-254	229	C22-	7630	-254	289	G232	7939	245
50	nWR/SCL	-4900	-254	110	VCOM	-700	-254	170	C12+	3500	-254	230	C22-	7700	-254	290	G230	7923	128
51	RS	-4830	-254	111	VCOM	-630	-254	171	C12+	3570	-254	231	C22-	7770	-254	291	G228	7907	245
52	nCS	-4760	-254	112	VCOM	-560	-254	172	C12+	3640	-254	232	C22-	7840	-254	292	G226	7891	128
53	TESTO14	-4690	-254	113	VCOM	-490	-254	173	C12+	3710	-254	233	C22-	7910	-254	293	G224	7875	245
54	TESTO15	-4620	-254	114	VCOM	-420	-254	174	C12+	3780	-254	234	C22-	7980	-254	294	G222	7859	128
55	FMARK	-4550	-254	115	VCOMH	-350	-254	175	C11-	3850	-254	235	C22+	8050	-254	295	G220	7843	245
56	TESTO16	-4480	-254	116	VCOMH	-280	-254	176	C11-	3920	-254	236	C22+	8120	-254	296	G218	7827	128
57	TS8	-4410	-254	117	VCOMH	-210	-254	177	C11-	3990	-254	237	C22+	8190	-254	297	G216	7811	245
58	TS7	-4340	-254	118	VCOMH	-140	-254	178	C11-	4060	-254	238	C22+	8260	-254	298	G214	7795	128
59	TS6	-4270	-254	119	VCOMH	-70	-254	179	C11-	4130	-254	239	C22+	8330	-254	299	G212	7779	245
60	TS5	-4200	-254	120	VCOMH	0	-254	180	C11+	4200	-254	240	C22+	8400	-254	300	G210	7763	128

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301	G208	7747	245	361	G88	6787	245	421	S706	5807	128	481	S646	4847	128	541	S586	3887	128
302	G206	7731	128	362	G86	6771	128	422	S705	5791	245	482	S645	4831	245	542	S585	3871	245
303	G204	7715	245	363	G84	6755	245	423	S704	5775	128	483	S644	4815	128	543	S584	3855	128
304	G202	7699	128	364	G82	6739	128	424	S703	5759	245	484	S643	4799	245	544	S583	3839	245
305	G200	7683	245	365	G80	6723	245	425	S702	5743	128	485	S642	4783	128	545	S582	3823	128
306	G198	7667	128	366	G78	6707	128	426	S701	5727	245	486	S641	4767	245	546	S581	3807	245
307	G196	7651	245	367	G76	6691	245	427	S700	5711	128	487	S640	4751	128	547	S580	3791	128
308	G194	7635	128	368	G74	6675	128	428	S699	5695	245	488	S639	4735	245	548	S579	3775	245
309	G192	7619	245	369	G72	6659	245	429	S698	5679	128	489	S638	4719	128	549	S578	3759	128
310	G190	7603	128	370	G70	6643	128	430	S697	5663	245	490	S637	4703	245	550	S577	3743	245
311	G188	7587	245	371	G68	6627	245	431	S696	5647	128	491	S636	4687	128	551	S576	3727	128
312	G186	7571	128	372	G66	6611	128	432	S695	5631	245	492	S635	4671	245	552	S575	3711	245
313	G184	7555	245	373	G64	6595	245	433	S694	5615	128	493	S634	4655	128	553	S574	3695	128
314	G182	7539	128	374	G62	6579	128	434	S693	5599	245	494	S633	4639	245	554	S573	3679	245
315	G180	7523	245	375	G60	6563	245	435	S692	5583	128	495	S632	4623	128	555	S572	3663	128
316	G178	7507	128	376	G58	6547	128	436	S691	5567	245	496	S631	4607	245	556	S571	3647	245
317	G176	7491	245	377	G56	6531	245	437	S690	5551	128	497	S630	4591	128	557	S570	3631	128
318	G174	7475	128	378	G54	6515	128	438	S689	5535	245	498	S629	4575	245	558	S569	3615	245
319	G172	7459	245	379	G52	6499	245	439	S688	5519	128	499	S628	4559	128	559	S568	3599	128
320	G170	7443	128	380	G50	6483	128	440	S687	5503	245	500	S627	4543	245	560	S567	3583	245
321	G168	7427	245	381	G48	6467	245	441	S686	5487	128	501	S626	4527	128	561	S566	3567	128
322	G166	7411	128	382	G46	6451	128	442	S685	5471	245	502	S625	4511	245	562	S565	3551	245
323	G164	7395	245	383	G44	6435	245	443	S684	5455	128	503	S624	4495	128	563	S564	3535	128
324	G162	7379	128	384	G42	6419	128	444	S683	5439	245	504	S623	4479	245	564	S563	3519	245
325	G160	7363	245	385	G40	6403	245	445	S682	5423	128	505	S622	4463	128	565	S562	3503	128
326	G158	7347	128	386	G38	6387	128	446	S681	5407	245	506	S621	4447	245	566	S561	3487	245
327	G156	7331	245	387	G36	6371	245	447	S680	5391	128	507	S620	4431	128	567	S560	3471	128
328	G154	7315	128	388	G34	6355	128	448	S679	5375	245	508	S619	4415	245	568	S559	3455	245
329	G152	7299	245	389	G32	6339	245	449	S678	5359	128	509	S618	4399	128	569	S558	3439	128
330	G150	7283	128	390	G30	6323	128	450	S677	5343	245	510	S617	4383	245	570	S557	3423	245
331	G148	7267	245	391	G28	6307	245	451	S676	5327	128	511	S616	4367	128	571	S556	3407	128
332	G146	7251	128	392	G26	6291	128	452	S675	5311	245	512	S615	4351	245	572	S555	3391	245
333	G144	7235	245	393	G24	6275	245	453	S674	5295	128	513	S614	4335	128	573	S554	3375	128
334	G142	7219	128	394	G22	6259	128	454	S673	5279	245	514	S613	4319	245	574	S553	3359	245
335	G140	7203	245	395	G20	6243	245	455	S672	5263	128	515	S612	4303	128	575	S552	3343	128
336	G138	7187	128	396	G18	6227	128	456	S671	5247	245	516	S611	4287	245	576	S551	3327	245
337	G136	7171	245	397	G16	6211	245	457	S670	5231	128	517	S610	4271	128	577	S550	3311	128
338	G134	7155	128	398	G14	6195	128	458	S669	5215	245	518	S609	4255	245	578	S549	3295	245
339	G132	7139	245	399	G12	6179	245	459	S668	5199	128	519	S608	4239	128	579	S548	3279	128
340	G130	7123	128	400	G10	6163	128	460	S667	5183	245	520	S607	4223	245	580	S547	3263	245
341	G128	7107	245	401	G8	6147	245	461	S666	5167	128	521	S606	4207	128	581	S546	3247	128
342	G126	7091	128	402	G6	6131	128	462	S665	5151	245	522	S605	4191	245	582	S545	3231	245
343	G124	7075	245	403	G4	6115	245	463	S664	5135	128	523	S604	4175	128	583	S544	3215	128
344	G122	7059	128	404	G2	6099	128	464	S663	5119	245	524	S603	4159	245	584	S543	3199	245
345	G120	7043	245	405	DUMMY21	6083	245	465	S662	5103	128	525	S602	4143	128	585	S542	3183	128
346	G118	7027	128	406	DUMMY22	6047	245	466	S661	5087	245	526	S601	4127	245	586	S541	3167	245
347	G116	7011	245	407	S720	6031	128	467	S660	5071	128	527	S600	4111	128	587	S540	3151	128
348	G114	6995	128	408	S719	6015	245	468	S659	5055	245	528	S599	4095	245	588	S539	3135	245
349	G112	6979	245	409	S718	5999	128	469	S658	5039	128	529	S598	4079	128	589	S538	3119	128
350	G110	6963	128	410	S717	5983	245	470	S657	5023	245	530	S597	4063	245	590	S537	3103	245
351	G108	6947	245	411	S716	5967	128	471	S656	5007	128	531	S596	4047	128	591	S536	3087	128
352	G106	6931	128	412	S715	5951	245	472	S655	4991	245	532	S595	4031	245	592	S535	3071	245
353	G104	6915	245	413	S714	5935	128	473	S654	4975	128	533	S594	4015	128	593	S534	3055	128
354	G102	6899	128	414	S713	5919	245	474	S653	4959	245	534	S593	3999	245	594	S533	3039	245
355	G100	6883	245	415	S712	5903	128	475	S652	4943	128	535	S592	3983	128	595	S532	3023	128
356	G98	6867	128	416	S711	5887	245	476	S651	4927	245	536	S591	3967	245	596	S531	3007	245
357	G96	6851	245	417	S710	5871	128	477	S650	4911	128	537	S590	3951	128	597	S530	2991	128
358	G94	6835	128	418	S709	5855	245	478	S649	4895	245	538	S589	3935	245	598	S529	2975	245
359	G92	6819	245	419	S708	5839	128	479	S648	4879	128	539	S588	3919	128	599	S528	2959	128
360	G90	6803	128	420	S707	5823	245	480	S647	4863	245	540	S587	3903	245	600	S527	2943	245

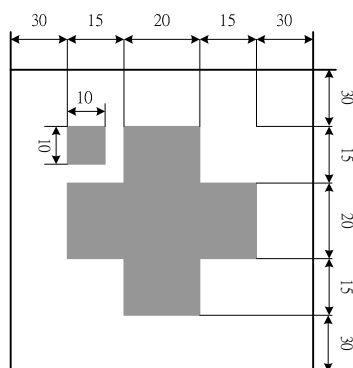
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601	S526	2927	128	661	S466	1967	128	721	S406	1007	128	781	S348	-479	245	841	S288	-1439	245
602	S525	2911	245	662	S465	1951	245	722	S405	991	245	782	S347	-495	128	842	S287	-1455	128
603	S524	2895	128	663	S464	1935	128	723	S404	975	128	783	S346	-511	245	843	S286	-1471	245
604	S523	2879	245	664	S463	1919	245	724	S403	959	245	784	S345	-527	128	844	S285	-1487	128
605	S522	2863	128	665	S462	1903	128	725	S402	943	128	785	S344	-543	245	845	S284	-1503	245
606	S521	2847	245	666	S461	1887	245	726	S401	927	245	786	S343	-559	128	846	S283	-1519	128
607	S520	2831	128	667	S460	1871	128	727	S400	911	128	787	S342	-575	245	847	S282	-1535	245
608	S519	2815	245	668	S459	1855	245	728	S399	895	245	788	S341	-591	128	848	S281	-1551	128
609	S518	2799	128	669	S458	1839	128	729	S398	879	128	789	S340	-607	245	849	S280	-1567	245
610	S517	2783	245	670	S457	1823	245	730	S397	863	245	790	S339	-623	128	850	S279	-1583	128
611	S516	2767	128	671	S456	1807	128	731	S396	847	128	791	S338	-639	245	851	S278	-1599	245
612	S515	2751	245	672	S455	1791	245	732	S395	831	245	792	S337	-655	128	852	S277	-1615	128
613	S514	2735	128	673	S454	1775	128	733	S394	815	128	793	S336	-671	245	853	S276	-1631	245
614	S513	2719	245	674	S453	1759	245	734	S393	799	245	794	S335	-687	128	854	S275	-1647	128
615	S512	2703	128	675	S452	1743	128	735	S392	783	128	795	S334	-703	245	855	S274	-1663	245
616	S511	2687	245	676	S451	1727	245	736	S391	767	245	796	S333	-719	128	856	S273	-1679	128
617	S510	2671	128	677	S450	1711	128	737	S390	751	128	797	S332	-735	245	857	S272	-1695	245
618	S509	2655	245	678	S449	1695	245	738	S389	735	245	798	S331	-751	128	858	S271	-1711	128
619	S508	2639	128	679	S448	1679	128	739	S388	719	128	799	S330	-767	245	859	S270	-1727	245
620	S507	2623	245	680	S447	1663	245	740	S387	703	245	800	S329	-783	128	860	S269	-1743	128
621	S506	2607	128	681	S446	1647	128	741	S386	687	128	801	S328	-799	245	861	S268	-1759	245
622	S505	2591	245	682	S445	1631	245	742	S385	671	245	802	S327	-815	128	862	S267	-1775	128
623	S504	2575	128	683	S444	1615	128	743	S384	655	128	803	S326	-831	245	863	S266	-1791	245
624	S503	2559	245	684	S443	1599	245	744	S383	639	245	804	S325	-847	128	864	S265	-1807	128
625	S502	2543	128	685	S442	1583	128	745	S382	623	128	805	S324	-863	245	865	S264	-1823	245
626	S501	2527	245	686	S441	1567	245	746	S381	607	245	806	S323	-879	128	866	S263	-1839	128
627	S500	2511	128	687	S440	1551	128	747	S380	591	128	807	S322	-895	245	867	S262	-1855	245
628	S499	2495	245	688	S439	1535	245	748	S379	575	245	808	S321	-911	128	868	S261	-1871	128
629	S498	2479	128	689	S438	1519	128	749	S378	559	128	809	S320	-927	245	869	S260	-1887	245
630	S497	2463	245	690	S437	1503	245	750	S377	543	245	810	S319	-943	128	870	S259	-1903	128
631	S496	2447	128	691	S436	1487	128	751	S376	527	128	811	S318	-959	245	871	S258	-1919	245
632	S495	2431	245	692	S435	1471	245	752	S375	511	245	812	S317	-975	128	872	S257	-1935	128
633	S494	2415	128	693	S434	1455	128	753	S374	495	128	813	S316	-991	245	873	S256	-1951	245
634	S493	2399	245	694	S433	1439	245	754	S373	479	245	814	S315	-1007	128	874	S255	-1967	128
635	S492	2383	128	695	S432	1423	128	755	S372	463	128	815	S314	-1023	245	875	S254	-1983	245
636	S491	2367	245	696	S431	1407	245	756	S371	447	245	816	S313	-1039	128	876	S253	-1999	128
637	S490	2351	128	697	S430	1391	128	757	S370	431	128	817	S312	-1055	245	877	S252	-2015	245
638	S489	2335	245	698	S429	1375	245	758	S369	415	245	818	S311	-1071	128	878	S251	-2031	128
639	S488	2319	128	699	S428	1359	128	759	S368	399	128	819	S310	-1087	245	879	S250	-2047	245
640	S487	2303	245	700	S427	1343	245	760	S367	383	245	820	S309	-1103	128	880	S249	-2063	128
641	S486	2287	128	701	S426	1327	128	761	S366	367	128	821	S308	-1119	245	881	S248	-2079	245
642	S485	2271	245	702	S425	1311	245	762	S365	351	245	822	S307	-1135	128	882	S247	-2095	128
643	S484	2255	128	703	S424	1295	128	763	S364	335	128	823	S306	-1151	245	883	S246	-2111	245
644	S483	2239	245	704	S423	1279	245	764	S363	319	245	824	S305	-1167	128	884	S245	-2127	128
645	S482	2223	128	705	S422	1263	128	765	S362	303	128	825	S304	-1183	245	885	S244	-2143	245
646	S481	2207	245	706	S421	1247	245	766	S361	287	245	826	S303	-1199	128	886	S243	-2159	128
647	S480	2191	128	707	S420	1231	128	767	DUMMY23	271	128	827	S302	-1215	245	887	S242	-2175	245
648	S479	2175	245	708	S419	1215	245	768	DUMMY24	-271	128	828	S301	-1231	128	888	S241	-2191	128
649	S478	2159	128	709	S418	1199	128	769	S360	-287	245	829	S300	-1247	245	889	S240	-2207	245
650	S477	2143	245	710	S417	1183	245	770	S359	-303	128	830	S299	-1263	128	890	S239	-2223	128
651	S476	2127	128	711	S416	1167	128	771	S358	-319	245	831	S298	-1279	245	891	S238	-2239	245
652	S475	2111	245	712	S415	1151	245	772	S357	-335	128	832	S297	-1295	128	892	S237	-2255	128
653	S474	2095	128	713	S414	1135	245	773	S356	-351	245	833	S296	-1311	245	893	S236	-2271	245
654	S473	2079	245	714	S413	1119	245	774	S355	-367	128	834	S295	-1327	128	894	S235	-2287	128
655	S472	2063	128	715	S412	1103	128	775	S354	-383	245	835	S294	-1343	245	895	S234	-2303	245
656	S471	2047	245	716	S411	1087	245	776	S353	-399	128	836	S293	-1359	128	896	S233	-2319	128
657	S470	2031	128	717	S410	1071	128	777	S352	-415	245	837	S292	-1375	245	897	S232	-2335	245
658	S469	2015	245	718	S409	1055	245	778	S351	-431	128	838	S291	-1391	128	898	S231	-2351	128
659	S468	1999	128	719	S408	1039	128	779	S350	-447	245	839	S290	-1407	245	899	S230	-2367	245
660	S467	1983	245	720	S407	1023	245	780	S349	-463	128	840	S289	-1423	128	900	S229	-2383	128

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
901	S228	-2399	245	961	S168	-3359	245	1021	S108	-4319	245	1081	S48	-5279	245	1141	G21	-6259	128
902	S227	-2415	128	962	S167	-3375	128	1022	S107	-4335	128	1082	S47	-5295	128	1142	G23	-6275	245
903	S226	-2431	245	963	S166	-3391	245	1023	S106	-4351	245	1083	S46	-5311	245	1143	G25	-6291	128
904	S225	-2447	128	964	S165	-3407	128	1024	S105	-4367	128	1084	S45	-5327	128	1144	G27	-6307	245
905	S224	-2463	245	965	S164	-3423	245	1025	S104	-4383	245	1085	S44	-5343	245	1145	G29	-6323	128
906	S223	-2479	128	966	S163	-3439	128	1026	S103	-4399	128	1086	S43	-5359	128	1146	G31	-6339	245
907	S222	-2495	245	967	S162	-3455	245	1027	S102	-4415	245	1087	S42	-5375	245	1147	G33	-6355	128
908	S221	-2511	128	968	S161	-3471	128	1028	S101	-4431	128	1088	S41	-5391	128	1148	G35	-6371	245
909	S220	-2527	245	969	S160	-3487	245	1029	S100	-4447	245	1089	S40	-5407	245	1149	G37	-6387	128
910	S219	-2543	128	970	S159	-3503	128	1030	S99	-4463	128	1090	S39	-5423	128	1150	G39	-6403	245
911	S218	-2559	245	971	S158	-3519	245	1031	S98	-4479	245	1091	S38	-5439	245	1151	G41	-6419	128
912	S217	-2575	128	972	S157	-3535	128	1032	S97	-4495	128	1092	S37	-5455	128	1152	G43	-6435	245
913	S216	-2591	245	973	S156	-3551	245	1033	S96	-4511	245	1093	S36	-5471	245	1153	G45	-6451	128
914	S215	-2607	128	974	S155	-3567	128	1034	S95	-4527	128	1094	S35	-5487	128	1154	G47	-6467	245
915	S214	-2623	245	975	S154	-3583	245	1035	S94	-4543	245	1095	S34	-5503	245	1155	G49	-6483	128
916	S213	-2639	128	976	S153	-3599	128	1036	S93	-4559	128	1096	S33	-5519	128	1156	G51	-6499	245
917	S212	-2655	245	977	S152	-3615	245	1037	S92	-4575	245	1097	S32	-5535	245	1157	G53	-6515	128
918	S211	-2671	128	978	S151	-3631	128	1038	S91	-4591	128	1098	S31	-5551	128	1158	G55	-6531	245
919	S210	-2687	245	979	S150	-3647	245	1039	S90	-4607	245	1099	S30	-5567	245	1159	G57	-6547	128
920	S209	-2703	128	980	S149	-3663	128	1040	S89	-4623	128	1100	S29	-5583	128	1160	G59	-6563	245
921	S208	-2719	245	981	S128	-3679	245	1041	S88	-4639	245	1101	S28	-5599	245	1161	G61	-6579	128
922	S207	-2735	128	982	S147	-3695	128	1042	S87	-4655	128	1102	S27	-5615	128	1162	G63	-6595	245
923	S206	-2751	245	983	S146	-3711	245	1043	S86	-4671	245	1103	S26	-5631	245	1163	G65	-6611	128
924	S205	-2767	128	984	S145	-3727	128	1044	S85	-4687	128	1104	S25	-5647	128	1164	G67	-6627	245
925	S204	-2783	245	985	S144	-3743	245	1045	S84	-4703	245	1105	S24	-5663	245	1165	G69	-6643	128
926	S203	-2799	128	986	S143	-3759	128	1046	S83	-4719	128	1106	S23	-5679	128	1166	G71	-6659	245
927	S202	-2815	245	987	S142	-3775	245	1047	S82	-4735	245	1107	S22	-5695	245	1167	G73	-6675	128
928	S201	-2831	128	988	S141	-3791	128	1048	S81	-4751	128	1108	S21	-5711	128	1168	G75	-6691	245
929	S200	-2847	245	989	S140	-3807	245	1049	S80	-4767	245	1109	S20	-5727	245	1169	G77	-6707	128
930	S199	-2863	128	990	S139	-3823	128	1050	S79	-4783	128	1110	S19	-5743	128	1170	G79	-6723	245
931	S198	-2879	245	991	S138	-3839	245	1051	S78	-4799	245	1111	S18	-5759	245	1171	G81	-6739	128
932	S197	-2895	128	992	S137	-3855	128	1052	S77	-4815	128	1112	S17	-5775	128	1172	G83	-6755	245
933	S196	-2911	245	993	S136	-3871	245	1053	S76	-4831	245	1113	S16	-5791	245	1173	G85	-6771	128
934	S195	-2927	128	994	S135	-3887	128	1054	S75	-4847	128	1114	S15	-5807	128	1174	G87	-6787	245
935	S194	-2943	245	995	S134	-3903	245	1055	S74	-4863	245	1115	S14	-5823	245	1175	G89	-6803	128
936	S193	-2959	128	996	S133	-3919	128	1056	S73	-4879	128	1116	S13	-5839	128	1176	G91	-6819	245
937	S192	-2975	245	997	S132	-3935	245	1057	S72	-4895	245	1117	S12	-5855	245	1177	G93	-6835	128
938	S191	-2991	128	998	S131	-3951	128	1058	S71	-4911	128	1118	S11	-5871	128	1178	G95	-6851	245
939	S190	-3007	245	999	S130	-3967	245	1059	S70	-4927	245	1119	S10	-5887	245	1179	G97	-6867	128
940	S189	-3023	128	1000	S129	-3983	128	1060	S69	-4943	128	1120	S9	-5903	128	1180	G99	-6883	245
941	S188	-3039	245	1001	S128	-3999	245	1061	S68	-4959	245	1121	S8	-5919	245	1181	G101	-6899	128
942	S187	-3055	128	1002	S127	-4015	128	1062	S67	-4975	128	1122	S7	-5935	128	1182	G103	-6915	245
943	S186	-3071	245	1003	S126	-4031	245	1063	S66	-4991	245	1123	S6	-5951	245	1183	G105	-6931	128
944	S185	-3087	128	1004	S125	-4047	128	1064	S65	-5007	128	1124	S5	-5967	128	1184	G107	-6947	245
945	S184	-3103	245	1005	S124	-4063	245	1065	S64	-5023	245	1125	S4	-5983	245	1185	G109	-6963	128
946	S183	-3119	128	1006	S123	-4079	128	1066	S63	-5039	128	1126	S3	-5999	128	1186	G111	-6979	245
947	S182	-3135	245	1007	S122	-4095	245	1067	S62	-5055	245	1127	S2	-6015	245	1187	G113	-6995	128
948	S181	-3151	128	1008	S121	-4111	128	1068	S61	-5071	128	1128	S1	-6031	128	1188	G115	-7011	245
949	S180	-3167	245	1009	S120	-4127	245	1069	S60	-5087	245	1129	DUMMY25	-6047	245	1189	G117	-7027	128
950	S179	-3183	128	1010	S119	-4143	128	1070	S59	-5103	128	1130	DUMMY26	-6083	245	1190	G119	-7043	245
951	S178	-3199	245	1011	S118	-4159	245	1071	S58	-5119	245	1131	G1	-6099	128	1191	G121	-7059	128
952	S177	-3215	128	1012	S117	-4175	128	1072	S57	-5135	128	1132	G3	-6115	245	1192	G123	-7075	245
953	S176	-3231	245	1013	S116	-4191	245	1073	S56	-5151	245	1133	G5	-6131	128	1193	G125	-7091	128
954	S175	-3247	128	1014	S115	-4207	128	1074	S55	-5167	128	1134	G7	-6147	245	1194	G127	-7107	245
955	S174	-3263	245	1015	S114	-4223	245	1075	S54	-5183	245	1135	G9	-6163	128	1195	G129	-7123	128
956	S173	-3279	128	1016	S113	-4239	128	1076	S53	-5199	128	1136	G11	-6179	245	1196	G131	-7139	245
957	S172	-3295	245	1017	S112	-4255	245	1077	S52	-5215	245	1137	G13	-6195	128	1197	G133	-7155	128
958	S171	-3311	128	1018	S111	-4271	128	1078	S51	-5231	128	1138	G15	-6211	245	1198	G135	-7171	245
959	S170	-3327	245	1019	S110	-4287	245	1079	S50	-5247	245	1139	G17	-6227	128	1199	G137	-7187	128
960	S169	-3343	128	1020	S109	-4303	128	1080	S49	-5263	128	1140	G19	-6243	245	1200	G139	-7203	245

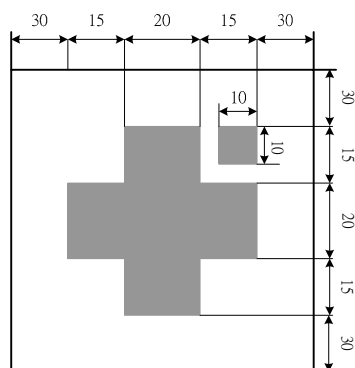
No.	Name	X	Y	No.	Name	X	Y
1201	G141	-7219	128	1261	G261	-8179	128
1202	G143	-7235	245	1262	G263	-8195	245
1203	G145	-7251	128	1263	G265	-8211	128
1204	G147	-7267	245	1264	G267	-8227	245
1205	G149	-7283	128	1265	G269	-8243	128
1206	G151	-7299	245	1266	G271	-8259	245
1207	G153	-7315	128	1267	G273	-8275	128
1208	G155	-7331	245	1268	G275	-8291	245
1209	G157	-7347	128	1269	G277	-8307	128
1210	G159	-7363	245	1270	G279	-8323	245
1211	G161	-7379	128	1271	G281	-8339	128
1212	G163	-7395	245	1272	G283	-8355	245
1213	G165	-7411	128	1273	G285	-8371	128
1214	G167	-7427	245	1274	G287	-8387	245
1215	G169	-7443	128	1275	G289	-8403	128
1216	G171	-7459	245	1276	G291	-8419	245
1217	G173	-7475	128	1277	G293	-8435	128
1218	G175	-7491	245	1278	G295	-8451	245
1219	G177	-7507	128	1279	G297	-8467	128
1220	G179	-7523	245	1280	G299	-8483	245
1221	G181	-7539	128	1281	G301	-8499	128
1222	G183	-7555	245	1282	G303	-8515	245
1223	G185	-7571	128	1283	G305	-8531	128
1224	G187	-7587	245	1284	G307	-8547	245
1225	G189	-7603	128	1285	G309	-8563	128
1226	G191	-7619	245	1286	G311	-8579	245
1227	G193	-7635	128	1287	G313	-8595	128
1228	G195	-7651	245	1288	G315	-8611	245
1229	G197	-7667	128	1289	G317	-8627	128
1230	G199	-7683	245	1290	G319	-8643	245
1231	G201	-7699	128	1291	DUMMY27	-8659	128
1232	G203	-7715	245				
1233	G205	-7731	128				
1234	G207	-7747	245				
1235	G209	-7763	128				
1236	G211	-7779	245				
1237	G213	-7795	128				
1238	G215	-7811	245				
1239	G217	-7827	128				
1240	G219	-7843	245				
1241	G221	-7859	128				
1242	G223	-7875	245				
1243	G225	-7891	128				
1244	G227	-7907	245				
1245	G229	-7923	128				
1246	G231	-7939	245				
1247	G233	-7955	128				
1248	G235	-7971	245				
1249	G237	-7987	128				
1250	G239	-8003	245				
1251	G241	-8019	128				
1252	G243	-8035	245				
1253	G245	-8051	128				
1254	G247	-8067	245				
1255	G249	-8083	128				
1256	G251	-8099	245				
1257	G253	-8115	128				
1258	G255	-8131	245				
1259	G257	-8147	128				
1260	G259	-8163	245				

<p>S1 ~ S720 G1 ~ G320 DUMMY20~27 (No. 244 ~ 1291)</p>	 <p>Unit: um</p>
<p>I/O Pads (No. 1 ~ 243)</p>	 <p>X=20, 30, 35 Y=70, 80, 85</p> <p>Unit: um</p>

Alignment mark



Alignment Mark: 1



Alignment Mark: 2

Alignment mark	X	Y
1	-8751	214.5
2	8751	214.5

6. Block Description

MPU System Interface

ILI9325D supports two system high-speed interfaces: i80-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and serial peripheral interface (SPI). The interface mode is selected by setting the IM[3:0] pins.

ILI9325D has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the ILI9325D read the first data from the internal GRAM. Valid data are read out after the ILI9325D performs the second read operation.

Registers are written consecutively as the register execution time.

Registers selection by system interface (8-/9-/16-/18-bit bus width)		I80	
Function	RS	nWR	nRD
Write an index to IR register	0	0	1
Write to control registers or the internal GRAM by WDR register.	1	0	1
Read from the internal GRAM by RDR register.	1	1	0

Registers selection by the SPI system interface		
Function	R/W	RS
Write an index to IR register	0	0
Write to control registers or the internal GRAM by WDR register.	0	1
Read from the internal GRAM by RDR register.	1	1

Parallel RGB Interface

ILI9325D supports the RGB interface and the VSYNC interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB17-0) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the "External Display Interface" section. The ILI9325D allows for switching between the external display interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

Graphics RAM (GRAM)

GRAM is graphics RAM storing bit-pattern data of 172,800 (240 x 320x 18/8) bytes with 18 bits per pixel.

Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the γ -correction register to display in 262,144 colors. For details, see the “ γ -Correction Register” section.

Timing Controller

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

Oscillator (OSC)

ILI9325D generates RC oscillation with an internal oscillation resistor. The frame rate is adjusted by the register setting.

LCD Driver Circuit

The LCD driver circuit of ILI9325D consists of a 720-output source driver (S1 ~ S720) and a 320-output gate driver (G1~G320). Display pattern data are latched when the 720th bit data are input. The latched data control the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720 source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

LCD Driver Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels VREG1OUT, VGH, VGL and Vcom for driving an LCD

7. System Interface

7.1. Interface Specifications

ILI9325D has the system interface to read/write the control registers and display graphics memory (GRAM), and the RGB Input Interface for displaying a moving picture. User can select an optimum interface to display the moving or still picture with efficient data transfer. All display data are stored in the GRAM to reduce the data transfer efforts and only the updating data is necessary to be transferred. User can only update a sub-range of GRAM by using the window address function.

ILI9325D also has the RGB interface and VSYNC interface to transfer the display data without flicker the moving picture on the screen. In RGB interface mode, the display data is written into the GRAM through the control signals of ENABLE, VSYNC, HSYNC, DOTCLK and data bus DB[17:0].

In VSYNC interface mode, the internal display timing is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface mode enables to display the moving picture display through the system interface. In this case, there are some constraints of speed and method to write data to the internal RAM.

ILI9325D operates in one of the following 4 modes. The display mode can be switched by the control register. When switching from one mode to another, refer to the sequences mentioned in the sections of RGB and VSYNC interfaces.

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM[1:0])
Internal operating clock only (Displaying still pictures)	System interface (RM = 0)	Internal operating clock (DM[1:0] = 00)
RGB interface (1) (Displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
RGB interface (2) (Rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM[1:0] = 01)
VSYNC interface (Displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM[1:0] = 10)

Note 1) Registers are set only via the system interface.

Note 2) The RGB-I/F and the VSYNC-I/F are not available simultaneously.

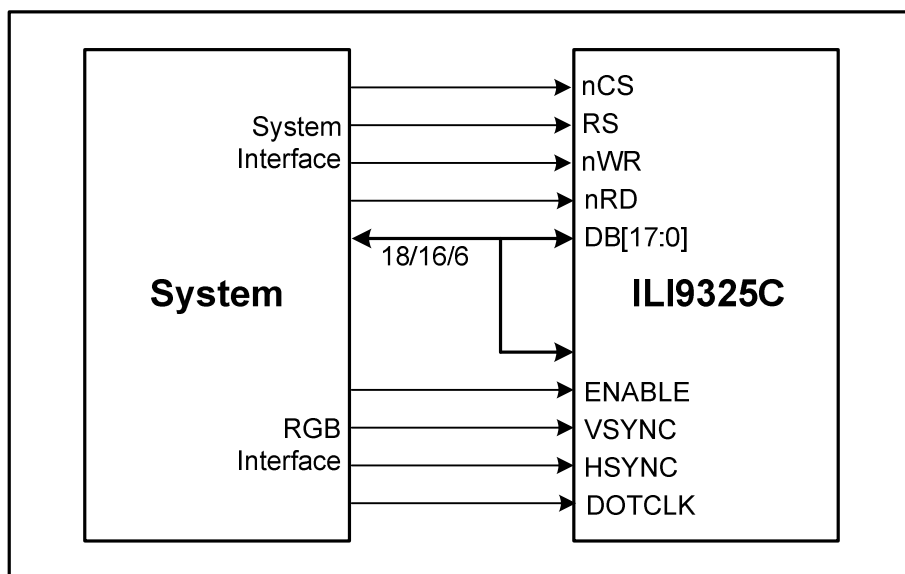


Figure 1 System Interface and RGB Interface connection

7.2. Input Interfaces

The following are the system interfaces available with the ILI9325D. The interface is selected by setting the IM[3:0] pins. The system interface is used for setting registers and GRAM access.

IM3	IM2	IM1	IM0/ID	Interface Mode	DB Pin
0	0	0	0	Setting invalid	
0	0	0	1	Setting invalid	
0	0	1	0	i80-system 16-bit interface	DB[17:10], DB[8:1]
0	0	1	1	i80-system 8-bit interface	DB[17:10]
0	1	0	ID	Serial Peripheral Interface (SPI)	SDI, SDO (DB[1:0])
0	1	1	0	9-bit 3 wires Serial Peripheral Interface	SDA, SCL, nCS
0	1	1	1	8-bit 4 wires Serial Peripheral Interface	SDA, SCL, nCS, RS (D/CX)
1	0	0	0	Setting invalid	
1	0	0	1	Setting invalid	
1	0	1	0	i80-system 18-bit interface	DB[17:0]
1	0	1	1	i80-system 9-bit interface	DB[17:9]
1	1	*	*	Setting invalid	

7.2.1. i80/18-bit System Interface

The i80/18-bit system interface is selected by setting the IM[3:0] as "1010" levels.

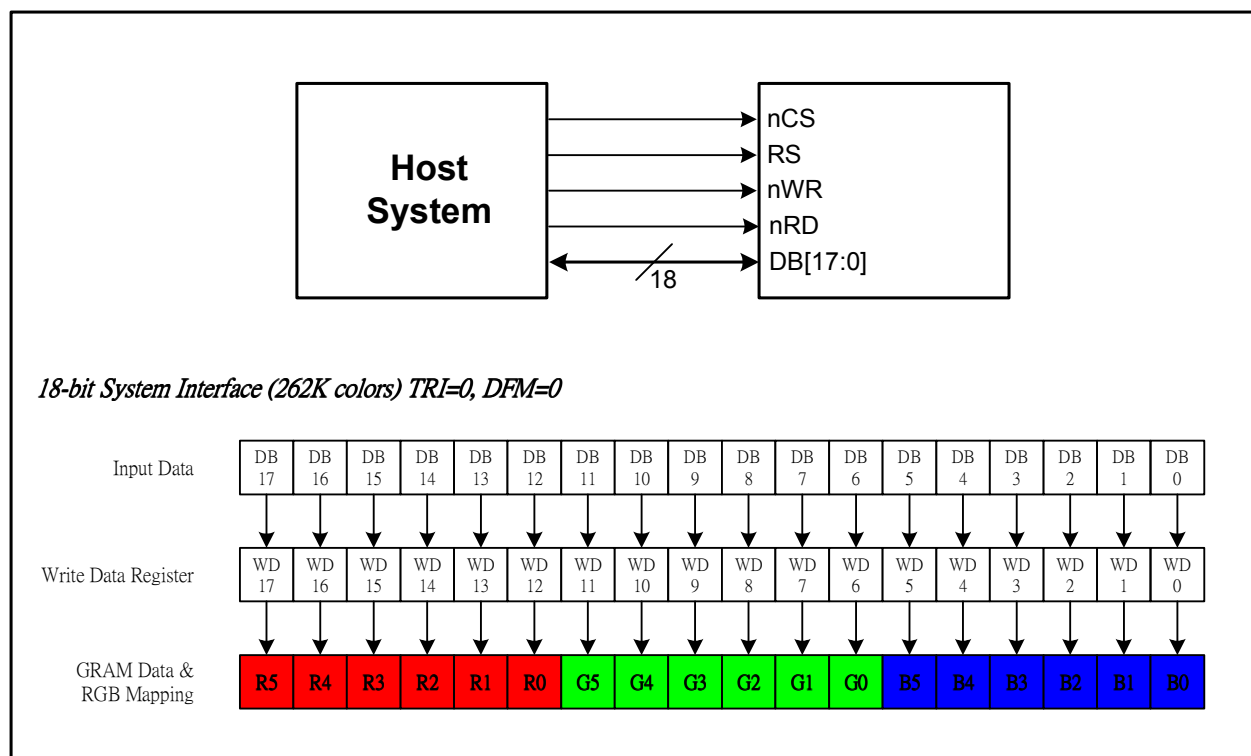


Figure 2 18-bit System Interface Data Format

7.2.2. i80/16-bit System Interface

The i80/16-bit system interface is selected by setting the IM[3:0] as "0010" levels. The 262K or 65K color can be display through the 16-bit MPU interface. When the 262K color is displayed, two transfers (1st transfer: 2 bits, 2nd transfer: 16 bits or 1st transfer: 16 bits, 2nd transfer: 2 bits) are necessary for the 16-bit CPU interface.

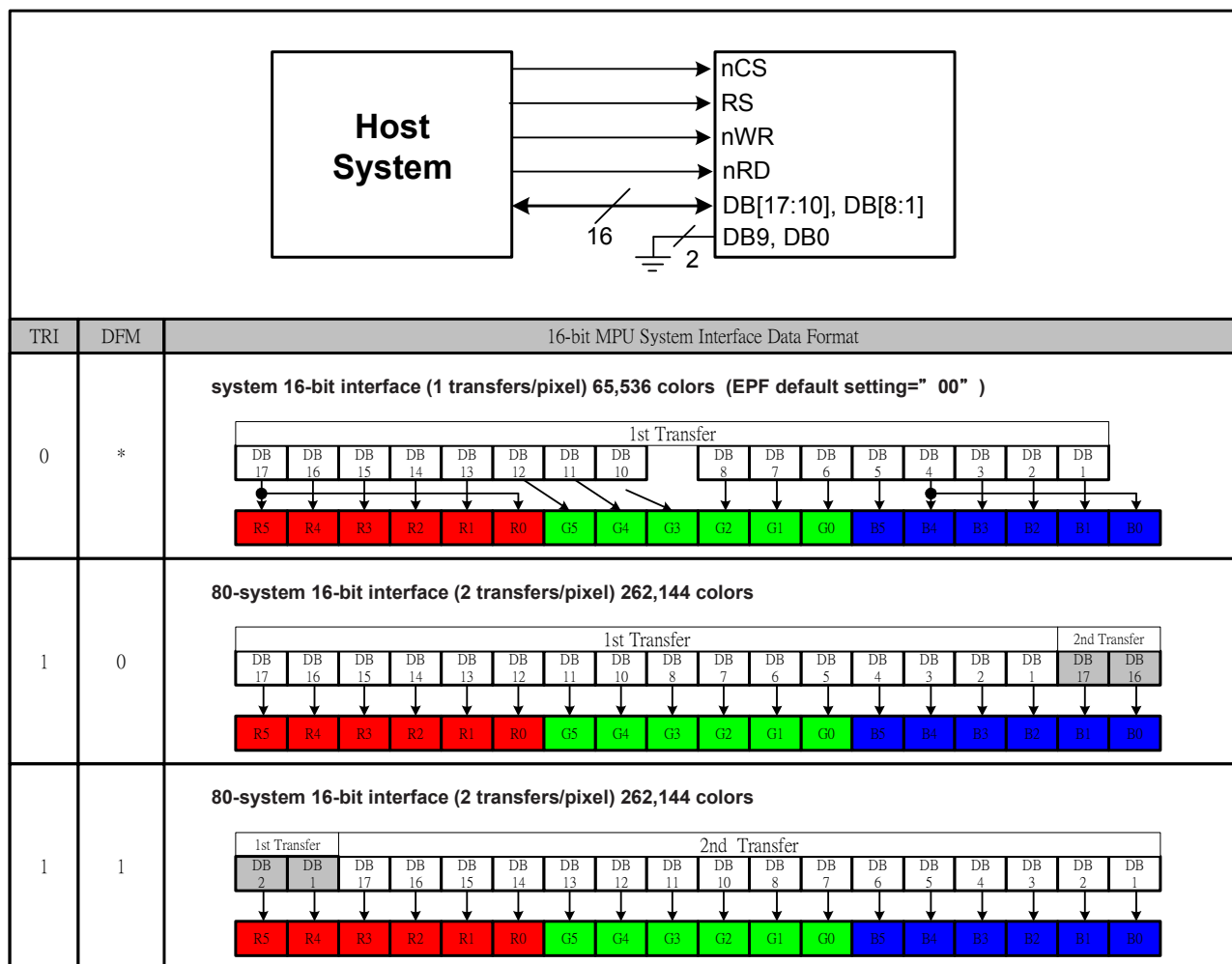


Figure 3 16-bit System Interface Data Format

7.2.3. i80/9-bit System Interface

The i80/9-bit system interface is selected by setting the IM[3:0] as “1011” and the DB17~DB9 pins are used to transfer the data. When writing the 18-bit register, the data is divided into upper byte (9 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (9 bits) and lower byte, and the upper byte is transferred first. The unused DB[8:0] pins must be tied to GND.

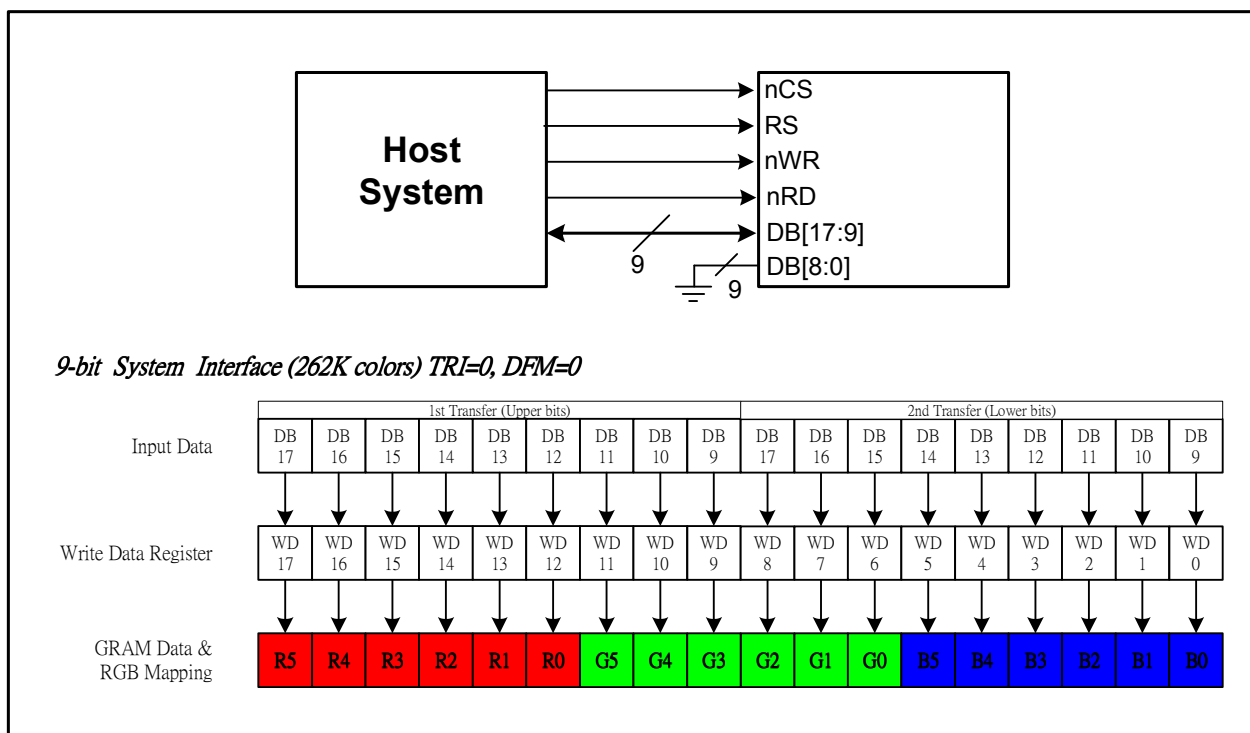


Figure 4 9-bit System Interface Data Format

7.2.4. i80/8-bit System Interface

The i80/8-bit system interface is selected by setting the IM[3:0] as "0011" and the DB17~DB10 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (8 bits) and lower byte, and the upper byte is transferred first. The written data is expanded into 18 bits internally (see the figure below) and then written into GRAM. The unused DB[9:0] pins must be tied to GND.

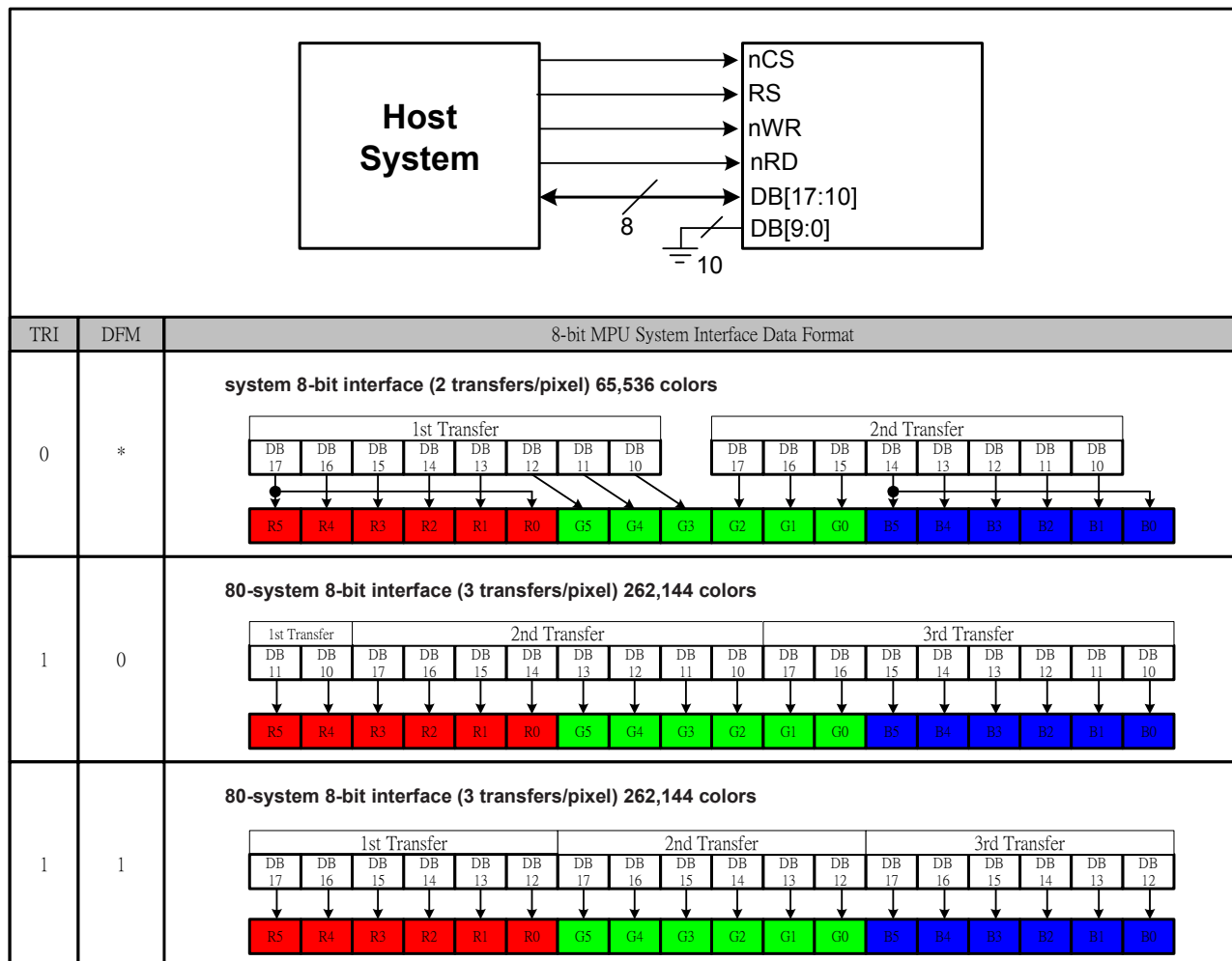


Figure 5 8-bit System Interface Data Format

7.3. Serial Peripheral Interface (SPI)

7.3.1. 16-bit 4 wires Serial Peripheral Interface

The Serial Peripheral Interface (SPI) is selected by setting the IM[3:0] pins as "010x" level. The chip select pin (nCS), the serial transfer clock pin (SCL), the serial data input pin (SDI) and the serial data output pin (SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[17:0] pins, which are not used, must be tied to GND.

The SPI interface operation enables from the falling edge of nCS and ends of data transfer on the rising edge of nCS. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by ILI9325D.

The seventh bit of start byte is RS bit. When RS = "0", either index write operation or status read operation is executed. When RS = "1", either register write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is "0" and read back when the R/W bit is "1".

After receiving the start byte, ILI9325D starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the ILI9325D are 16-bit format and receive the first and the second byte data as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 5 bytes dummy read is necessary and the valid data starts from 6th byte of read back data.

Start Byte Format

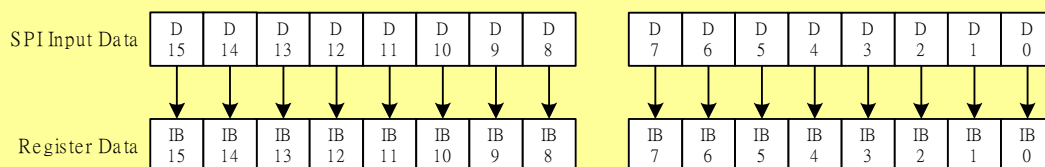
Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID	1/0	1/0

Note: ID bit is selected by setting the IM0/ID pin.

RS and R/W Bit Function

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write a register or GRAM data
1	1	Read a register or GRAM data

Serial Peripheral Interface for register access



Serial Peripheral Interface 65K colors

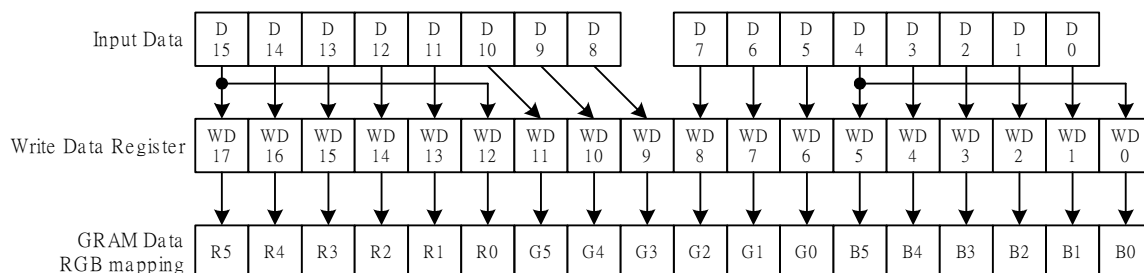
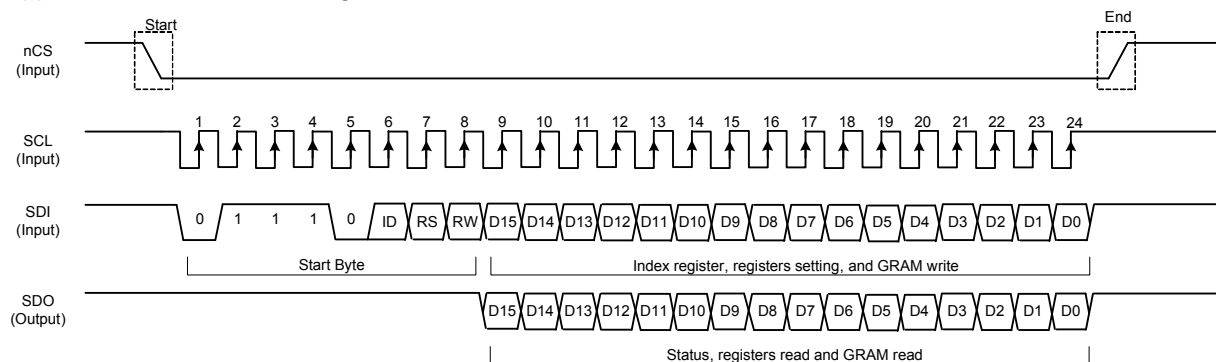
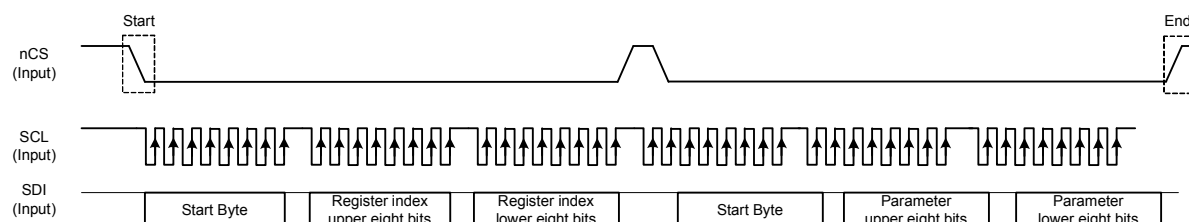


Figure 6 Data Format of SPI Interface

(a) Basic data transmission through SPI

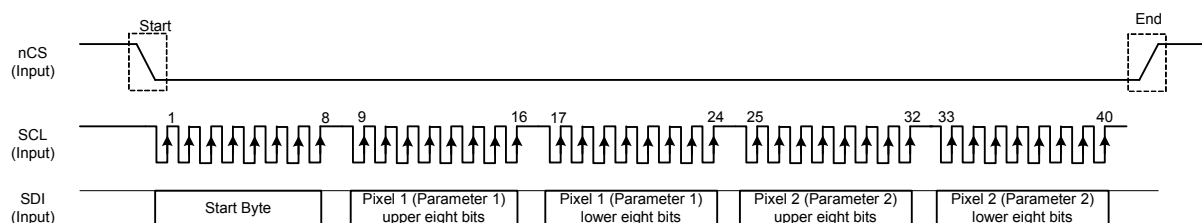


(b) Register write through SPI



Note: The first byte after the start byte is always the upper eight bits.

(c) Consecutive data transmission through SPI



Note: The first byte after the start byte is always the upper eight bits.

Figure 7 Data transmission through serial peripheral interface (SPI) (1)

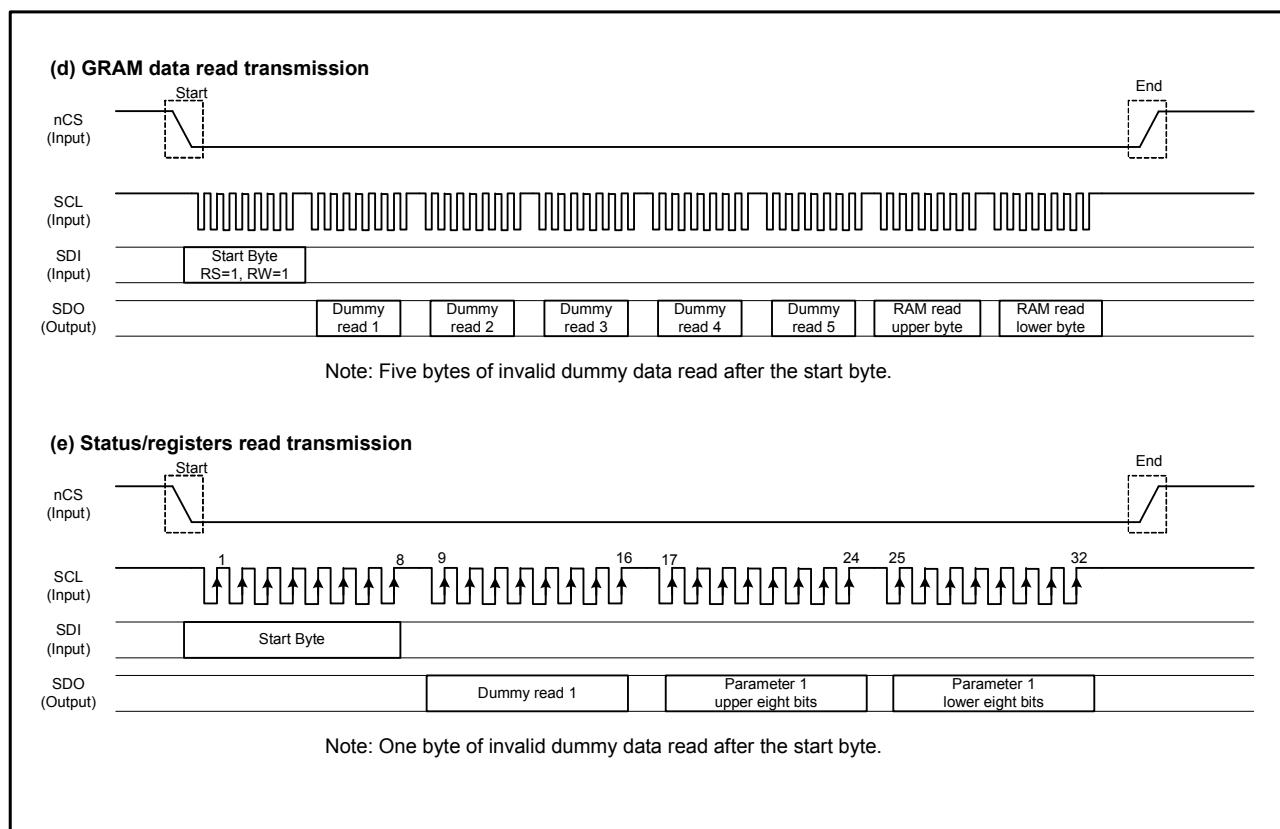


Figure 8 Data transmission through serial peripheral interface (SPI) (2)

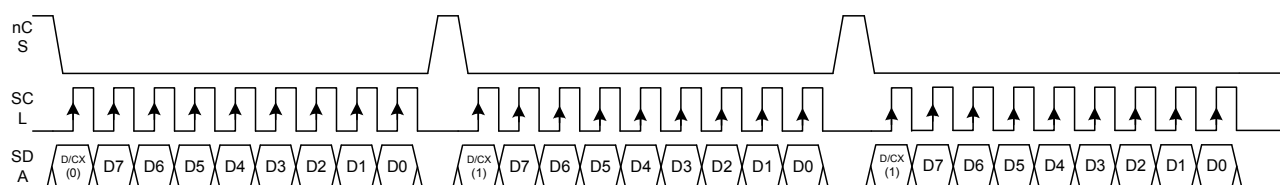
7.3.2. 3-wire 9-bit Serial Interface

This SPI mode uses a 3-wire 9-bit serial interface. The chip-select **nCS** (active low) enables and disables the serial interface. **SCL** is the serial data clock and **SDA** is serial data.

Serial data must be input to **SDA** in the sequence D/CX, D7 to D0. The ILI9325D reads the data at the rising edge of **SCL** signal. The first bit of serial data D/CX is data/command flag. When D/CX = "1", D7 to D0 bits are display RAM data or command parameters. When D/CX = "0" D7 to D0 bits are commands.

Register Write Mode:

Using the 9-bit serial interface to write register parameter or GRAM data, the register R66h must be set as "0" (R66h default = 0).



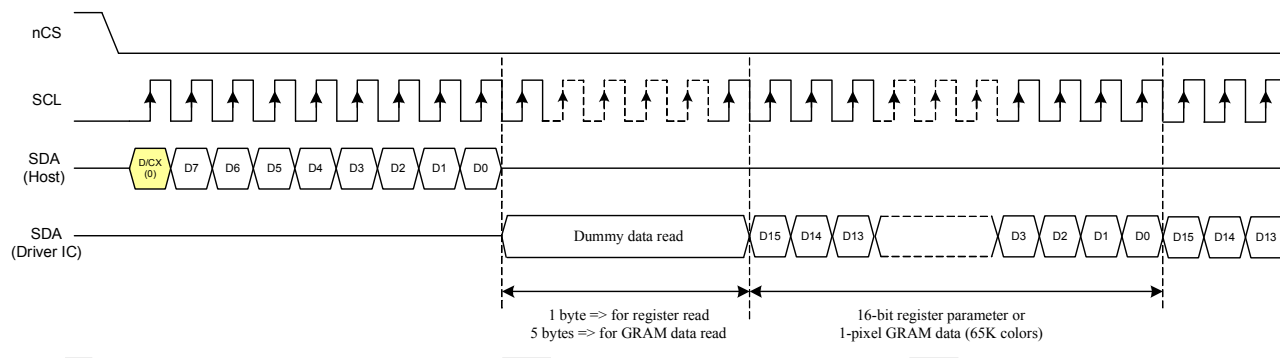
D/CX=0: Register Index (command).

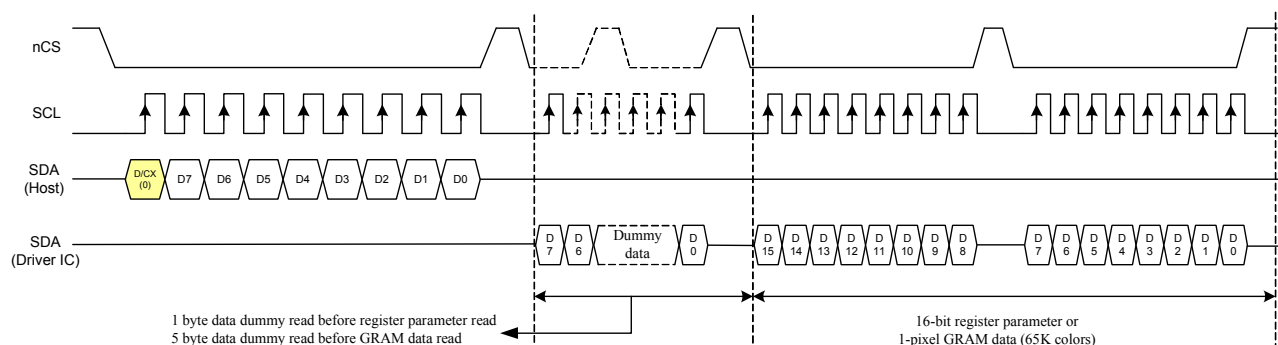
D/CX=1: Register parameter or GRAM data.



Register Read Mode:

When users need to read back the register parameter or GRAM data, the register R66h must be set as "1" first, and then write the register index to read back the register parameter or GRAM data. The following timing diagrams show 2 examples to read back the register parameter.

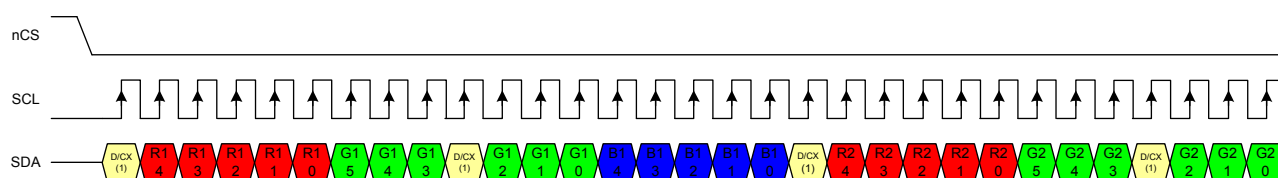




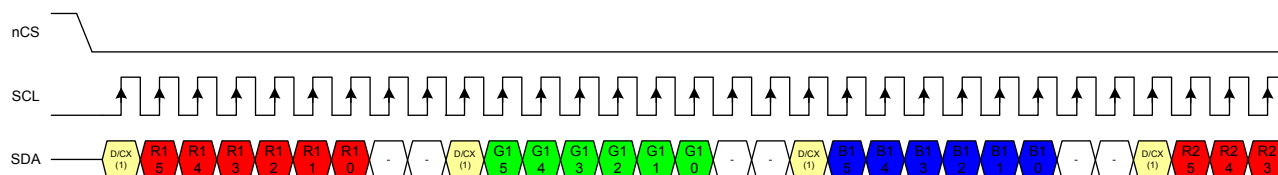
Note: One byte of invalid dummy data read is needed before register parameter read.

Five bytes of invalid dummy data read is needed before GRAM data read.

3-Wire Serial Interface and GRAM Data Stream (65K colors) (Set TRI = 0, DFM = 0)



3-Wire Serial Interface and GRAM Data Stream (262K colors) (Set TRI = 1, DFM = 0)



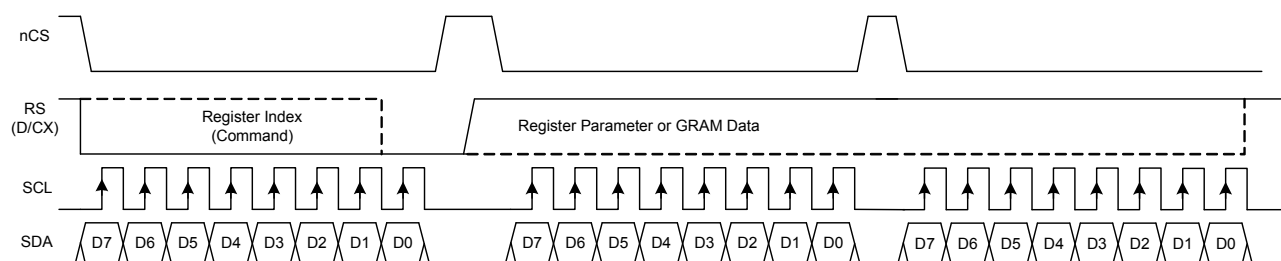
7.3.3. 4-wire 8-bit Serial Interface

This SPI mode uses a 4-wire 8-bit serial interface. The chip-select **nCS** (active low) enables and disables the serial interface. **D/CX** is the command or data select signal, **SCL** is the serial data clock and **SDA** is serial data.

Serial data must be input to **SDA** in the sequence D7 to D0. The ILI9325D reads the data at the rising edge of **SCL** signal. The **D/CX** signal indicates data/command. When D/CX = "1", D7 to D0 bits are display RAM data or command parameters. When D/CX = "0" D7 to D0 bits are commands.

Register Write Mode:

Using the 8-bit serial interface to write register parameter or GRAM data, the register R66h must be set as "0" (R66h default = 0).

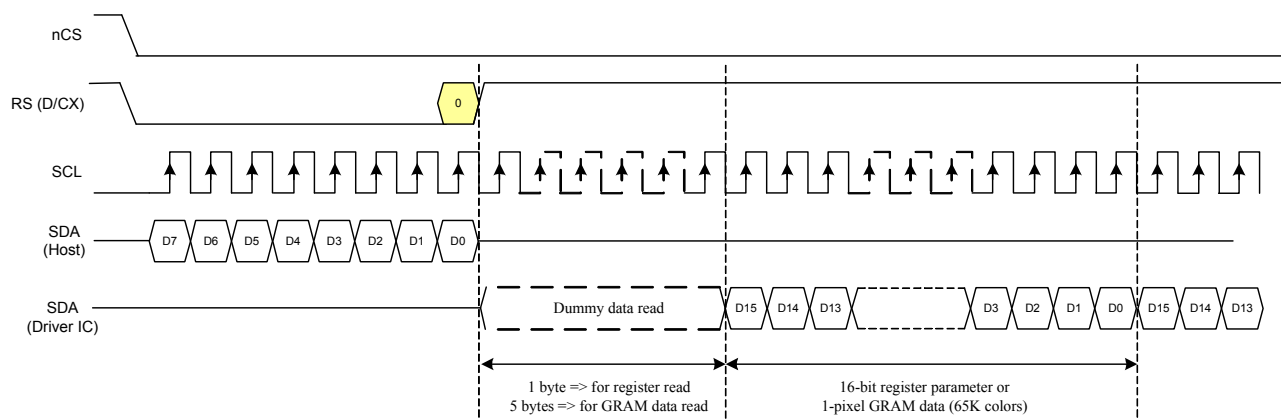


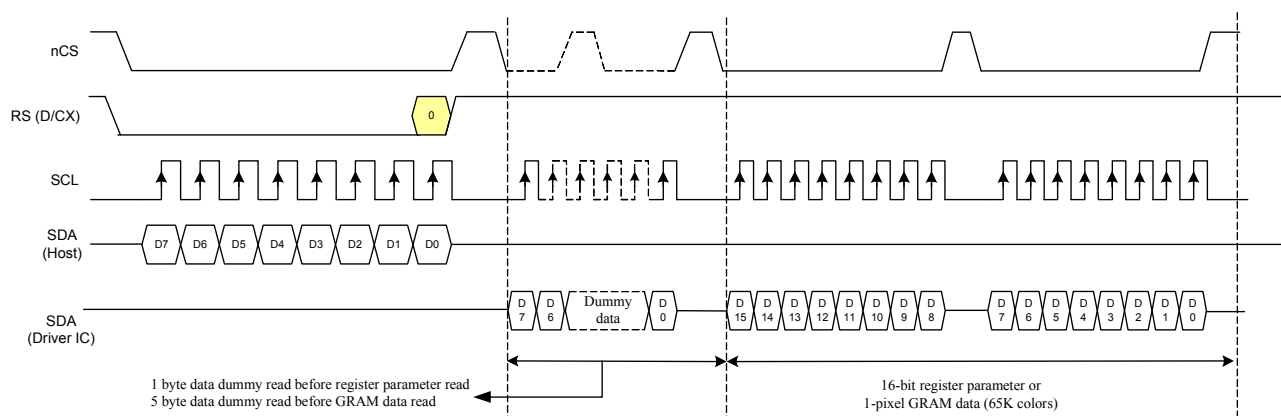
RS(D/CX) = 0 (low): Register Index (command).

RS(D/CX) = 1 (high): Register parameter or GRAM data.

Register Read Mode:

When users need to read back the register or GRAM data, the register R66h must be set as "1" first, and then write the register index to read back the register or GRAM data. The following timing diagrams show 2 examples to read back the register parameter or GRAM data.

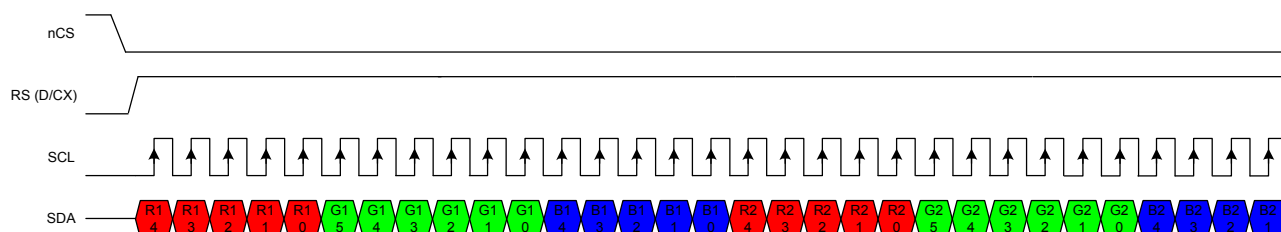




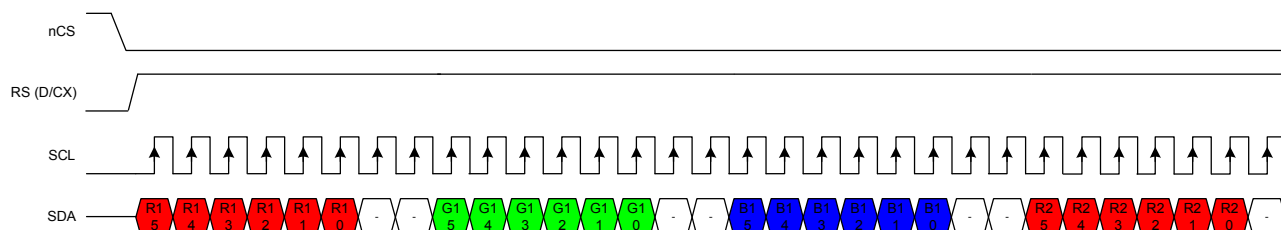
Note: One byte of invalid dummy data read is needed before register parameter read.

Five bytes of invalid dummy data read is needed before GRAM data read.

4-Wire Serial Interface and GRAM Data Stream (65K colors) (TRI = 0, DFM = 0)



4-Wire Serial Interface and GRAM Data Stream (262K colors) (TRI = 1, DFM = 0)



7.4. VSYNC Interface

ILI9325D supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the i80 system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = "10" and RM = "0".

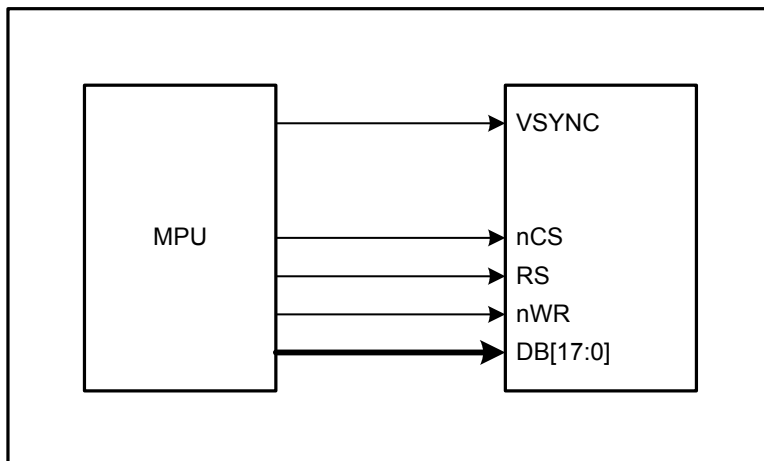


Figure 9 Data transmission through VSYNC interface)

In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.

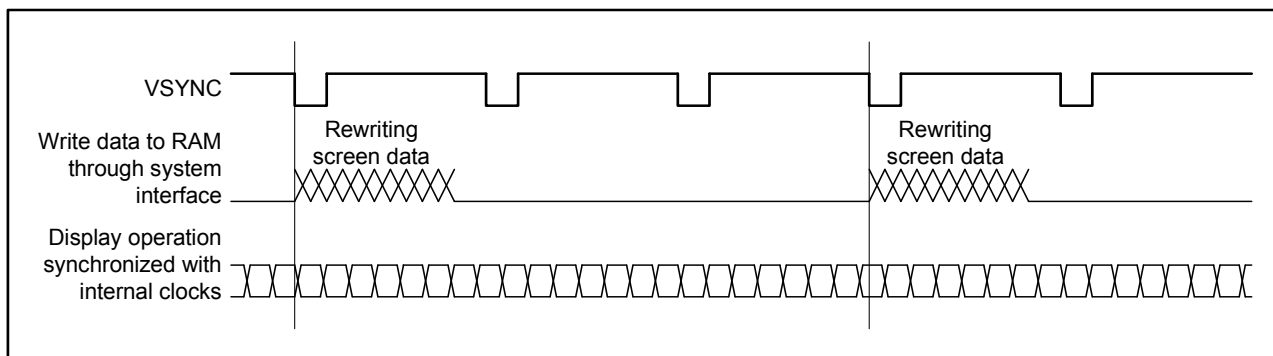


Figure 10 Moving picture data transmission through VSYNC interface

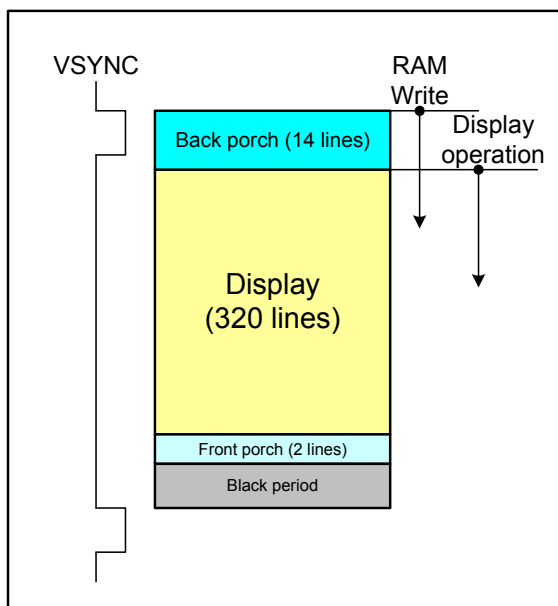


Figure 11 Operation through VSYNC Interface

The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (FP) + BackPorch (BP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.

$$\text{Minimum RAM write speed (HZ)} > \frac{240 \times \text{DisplayLines (NL)}}{[(\text{BackPorch(BP)} + \text{DisplayLines(NL)} - \text{margins}) \times 16 (\text{clocks}) \times 1/\text{fosc}]}$$

Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

[Example]

Display size: 240 RGB × 320 lines

Lines: 320 lines (NL = 100111)

Back porch: 14 lines (BP = 1110)

Front porch: 2 lines (FP = 0010)

Frame frequency: 60 Hz

Frequency fluctuation: 10%

$$\text{Internal oscillator clock (fosc.) [Hz]} = 60 \times [320 + 2 + 14] \times 16 \text{ clocks} \times (1.1/0.9) \doteq 394\text{KHz}$$

When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with $\pm 10\%$ margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

$$\text{Minimum speed for RAM writing [Hz]} > 240 \times 320 \times 394\text{K} / [(14 + 320 - 2)\text{lines} \times 16\text{clocks}] \doteq 5.7 \text{ MHz}$$

The above theoretical value is calculated based on the premise that the ILI9325D starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 5.7MHz or more will guarantee the completion of GRAM write operation before the ILI9325D starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes in using the VSYNC interface

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = "00") to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode and set the AM bit to "0" to transfer display data.

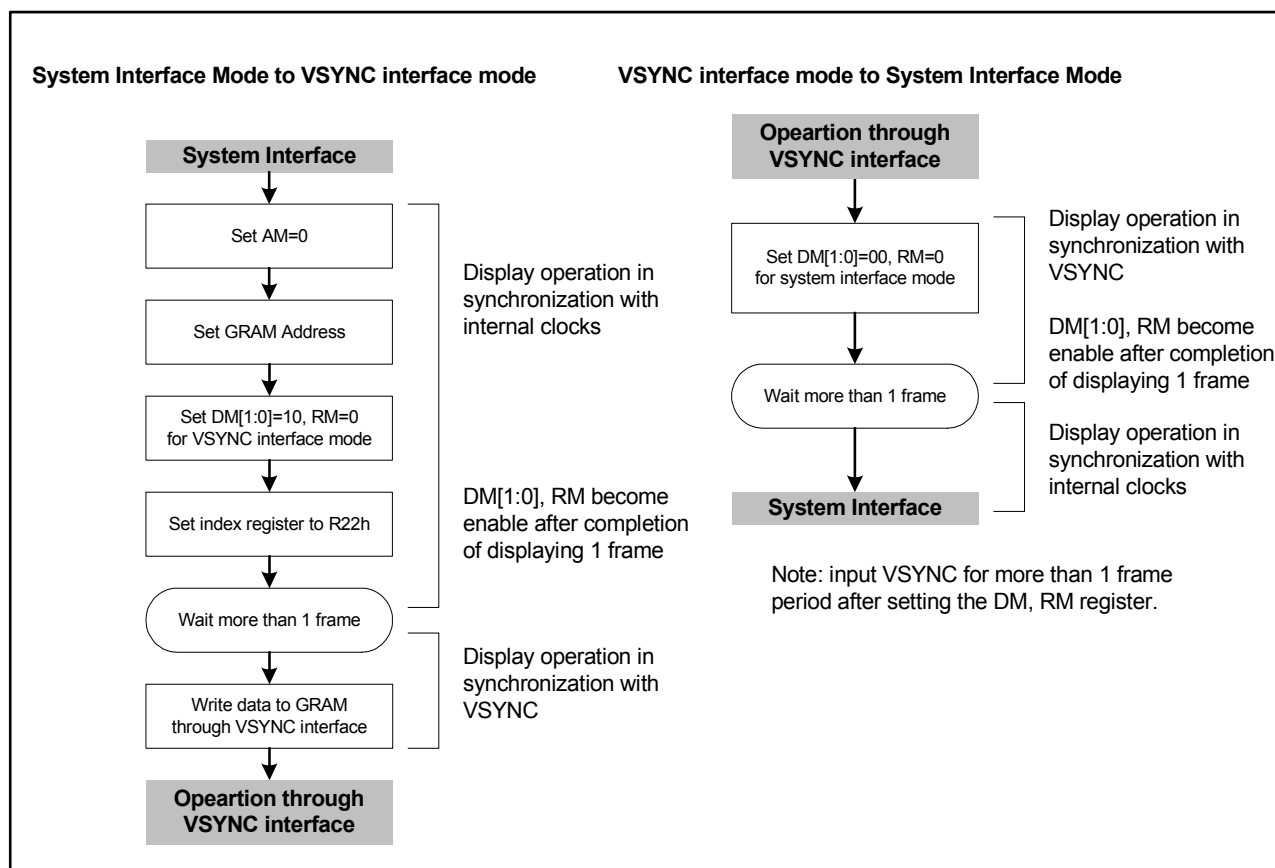


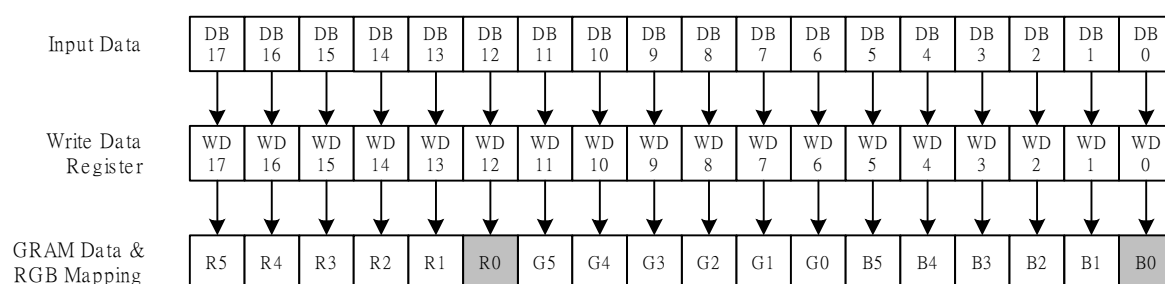
Figure 12 Transition flow between VSYNC and internal clock operation modes

7.5. RGB Input Interface

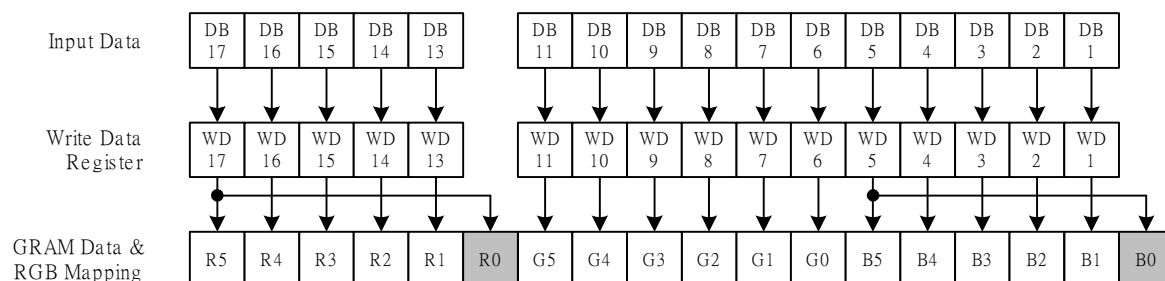
The RGB Interface mode is available for ILI9325D and the interface is selected by setting the RIM[1:0] bits as following table.

RIM1	RIM0	RGB Interface	DB pins
0	0	18-bit RGB Interface	DB[17:0]
0	1	16-bit RGB Interface	DB[17:13], DB[11:1]
1	0	6-bit RGB Interface	DB[17:12]
1	1	Setting prohibited	

18-bit RGB Interface (262K colors)



16-bit RGB Interface (65K colors)



6-bit RGB Interface (262K colors)

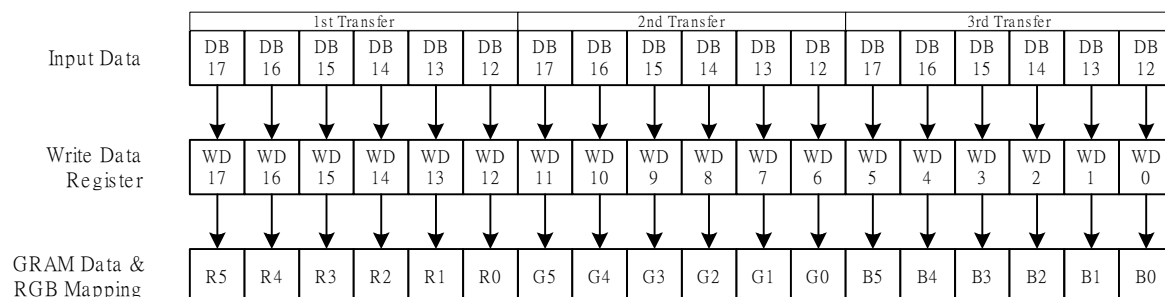


Figure 13 RGB Interface Data Format

7.5.1. RGB Interface

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The RGB interface transfers the updated data to GRAM and the update area is defined by the window address function. The back porch and front porch are used to set the RGB interface timing.

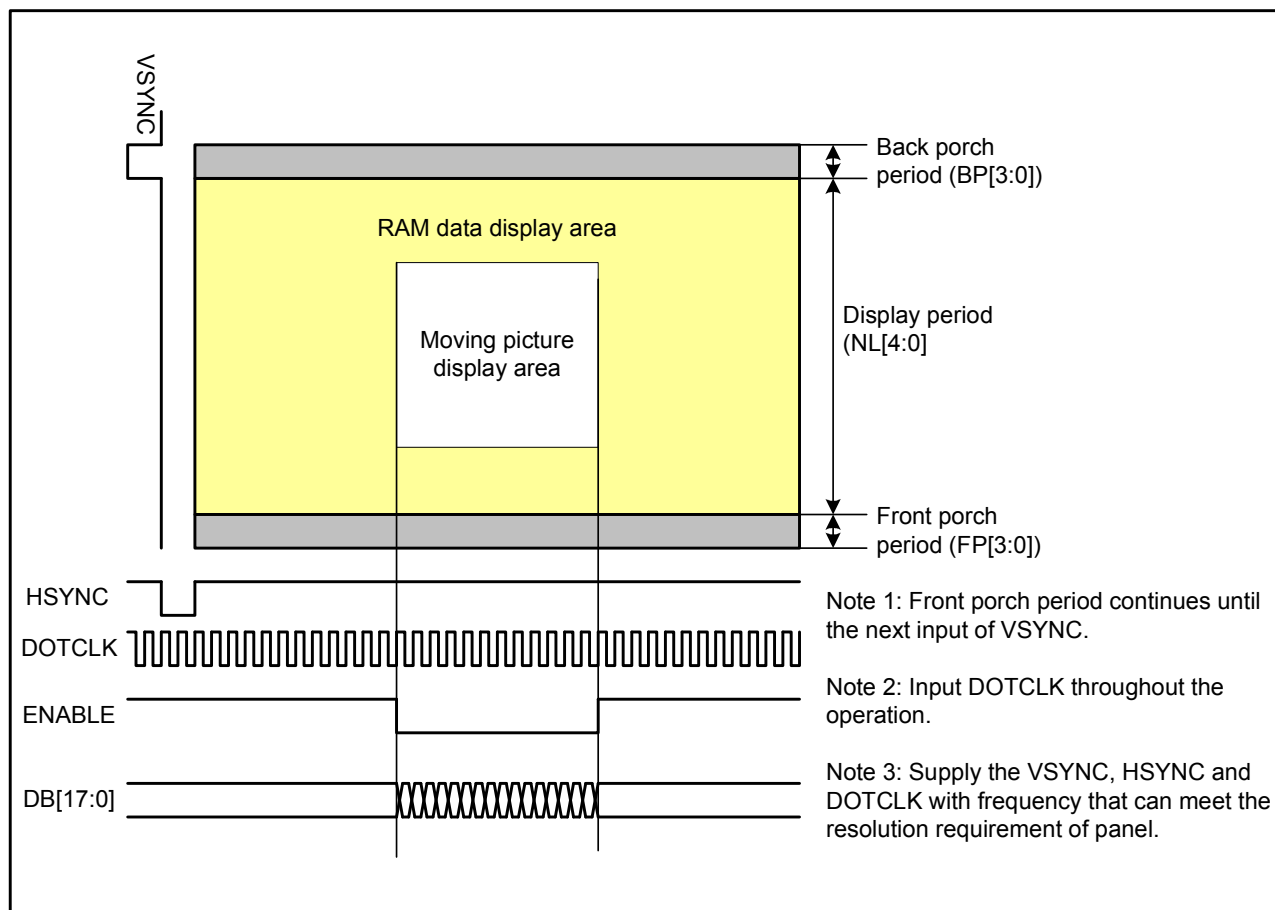


Figure 14 GRAM Access Area by RGB Interface

7.5.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as follows.

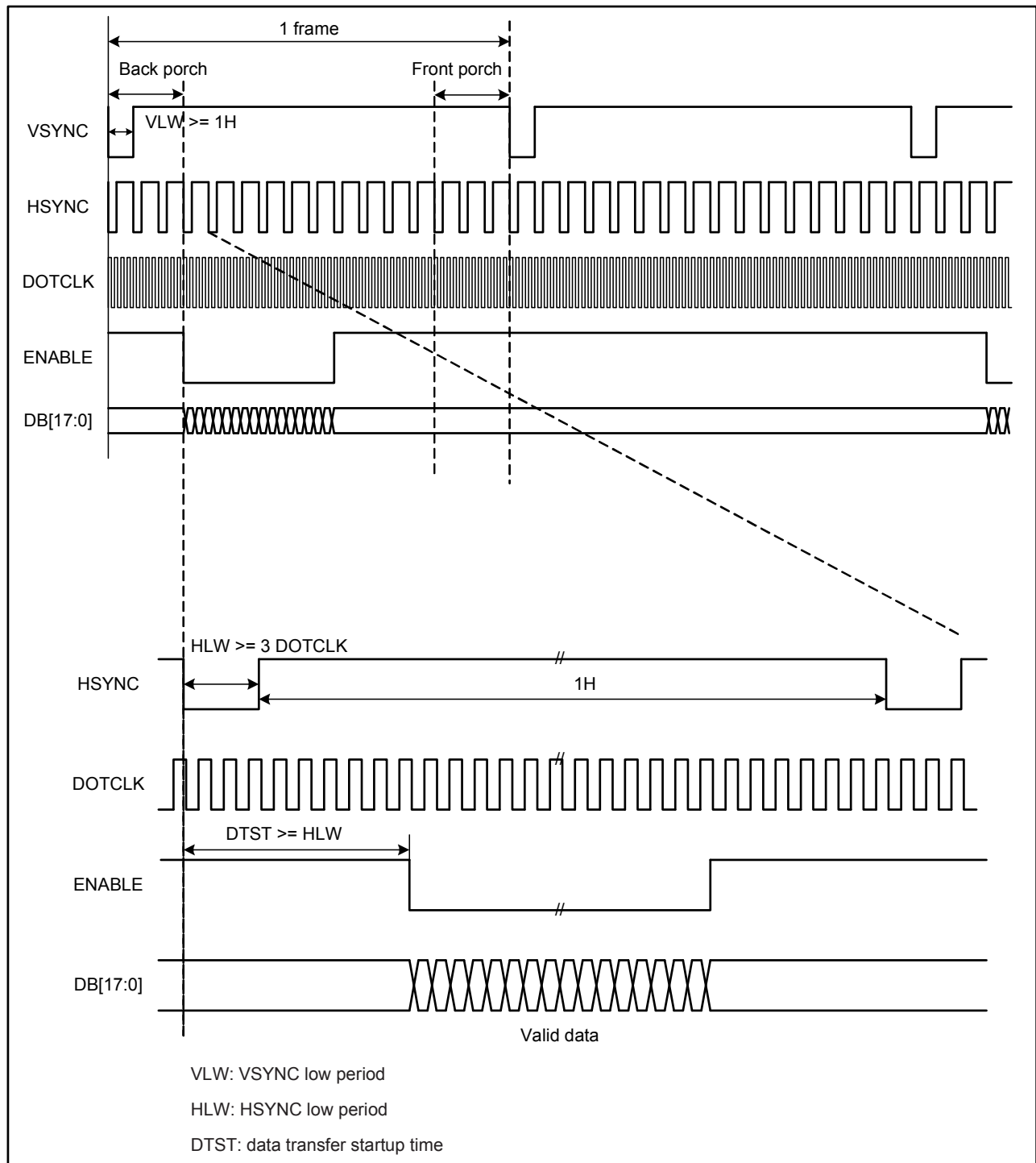


Figure 15 Timing Chart of Signals in 18-/16-bit RGB Interface Mode

The timing chart of 6-bit RGB interface mode is shown as follows.

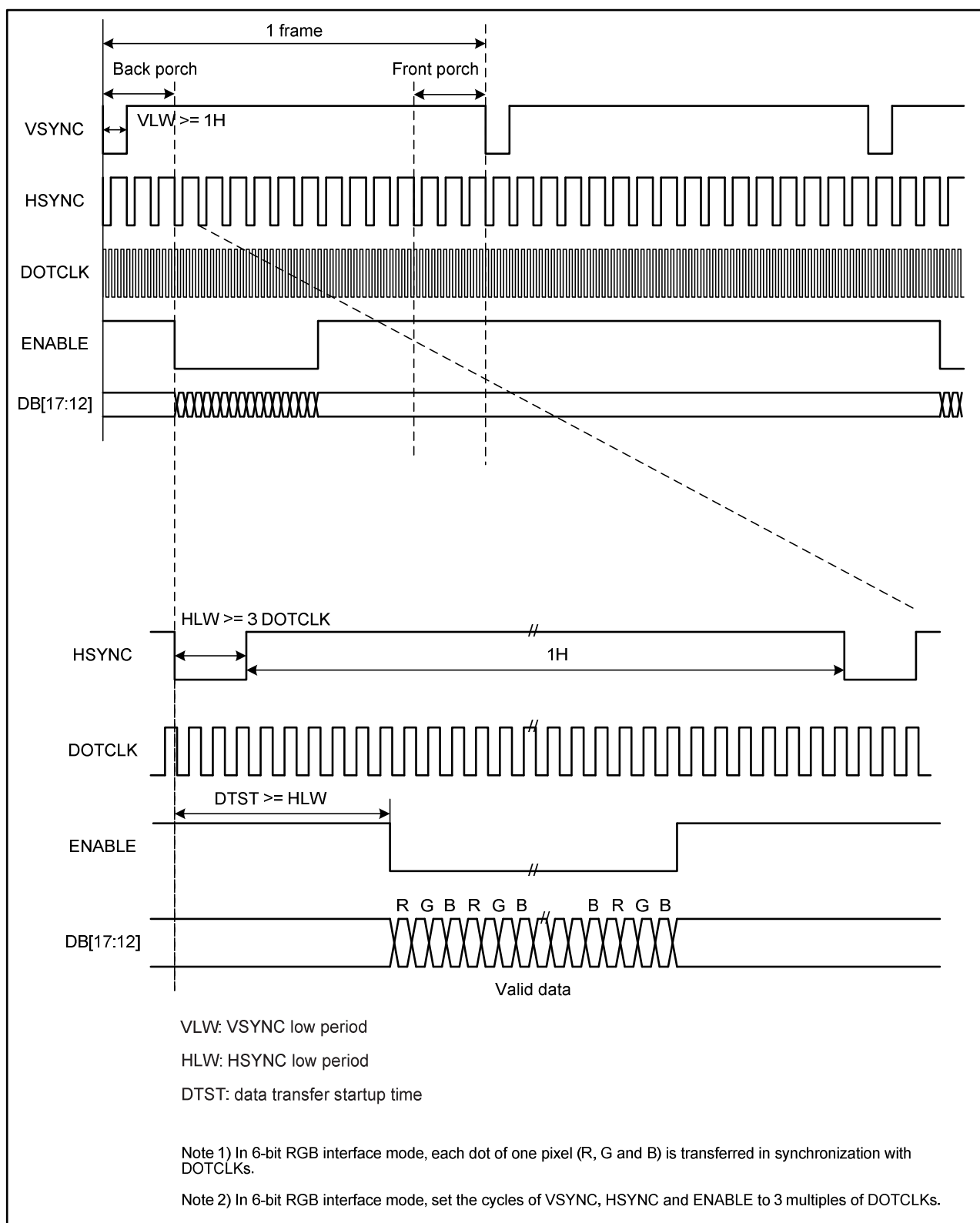


Figure 16 Timing chart of signals in 6-bit RGB interface mode

7.5.3. Moving Picture Mode

ILI9325D has the RGB interface to display moving picture and incorporates GRAM to store display data, which has following merits in displaying a moving picture.

- The window address function defined the update area of GRAM.
- Only the moving picture area of GRAM is updated.
- When display the moving picture in RGB interface mode, the DB[17:0] can be switched as system interface to update still picture area and registers, such as icons.

RAM access via a system interface in RGB-I/F mode

ILI9325D allows GRAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal GRAM in synchronization with DOTCLK and ENABLE signals. When write data to the internal GRAM by the system interface, set ENABLE to terminate the RGB interface and switch to the system interface to update the registers (RM = "0") and the still picture of GRAM. When restart RAM access in RGB interface mode, wait one read/write cycle and then set RM = "1" and the index register to R22h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal GRAM.

The following figure illustrates the operation of the ILI9325D when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.

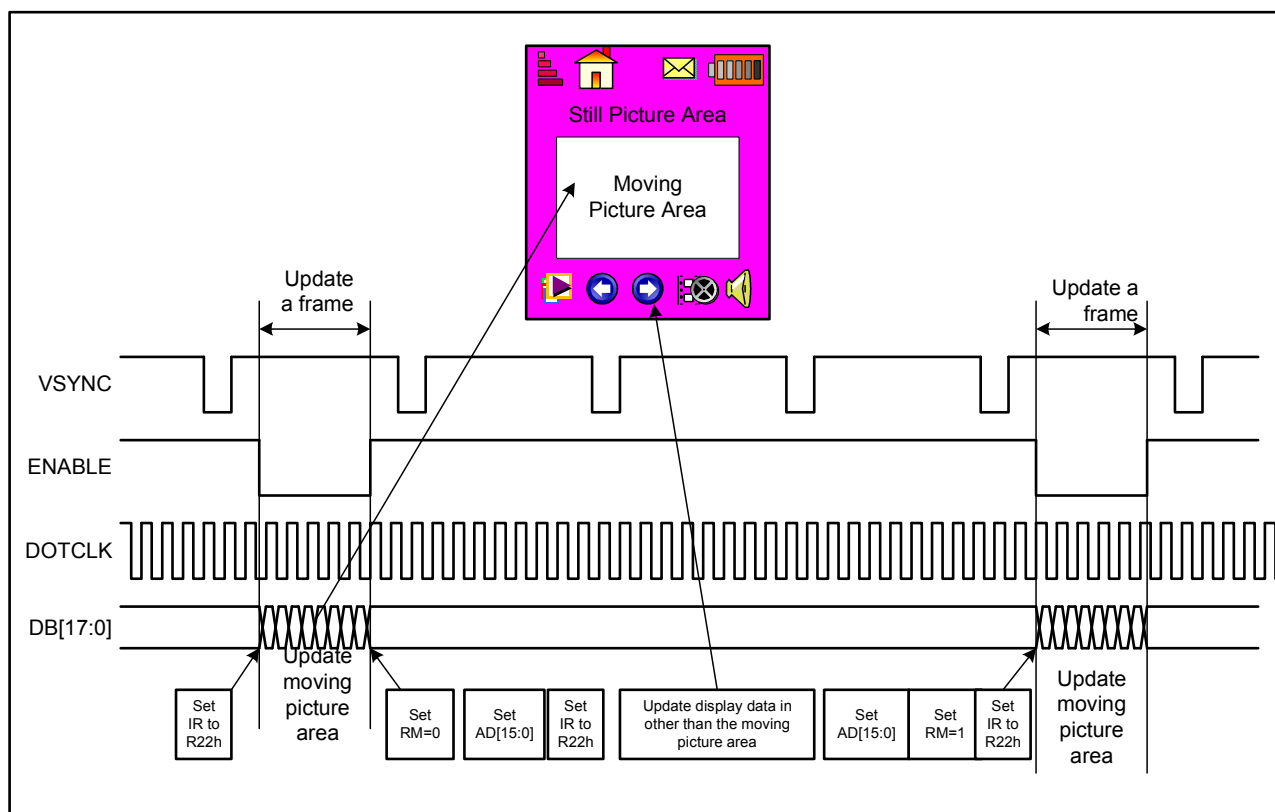
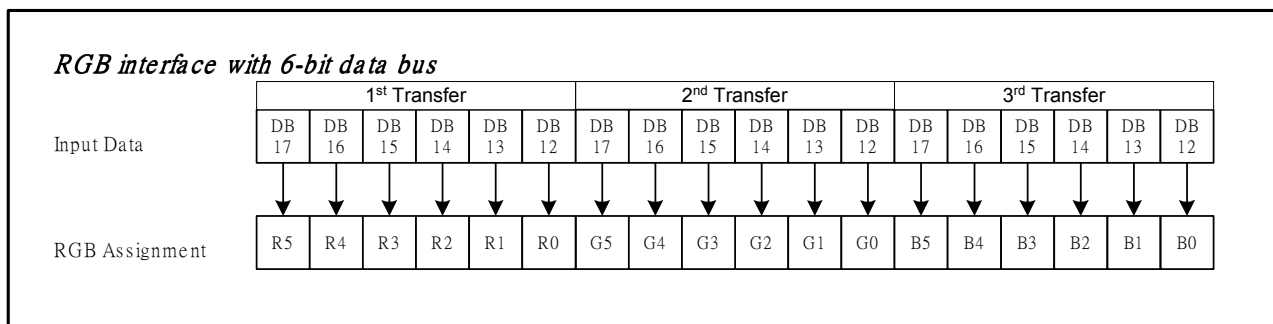


Figure 17 Example of update the still and moving picture

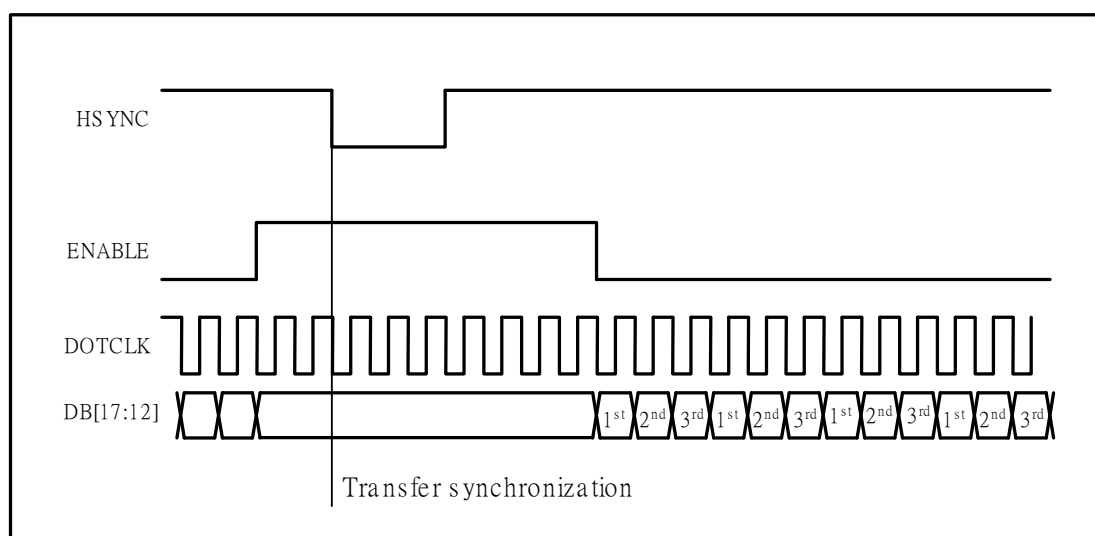
7.5.4. 6-bit RGB Interface

The 6-bit RGB interface is selected by setting the RIM[1:0] bits to “10”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (DB[17:12]) according to the data enable signal (ENABLE). Unused pins (DB[11:0]) must be fixed at GND level. Registers can be set by the system interface (i80/SPI).



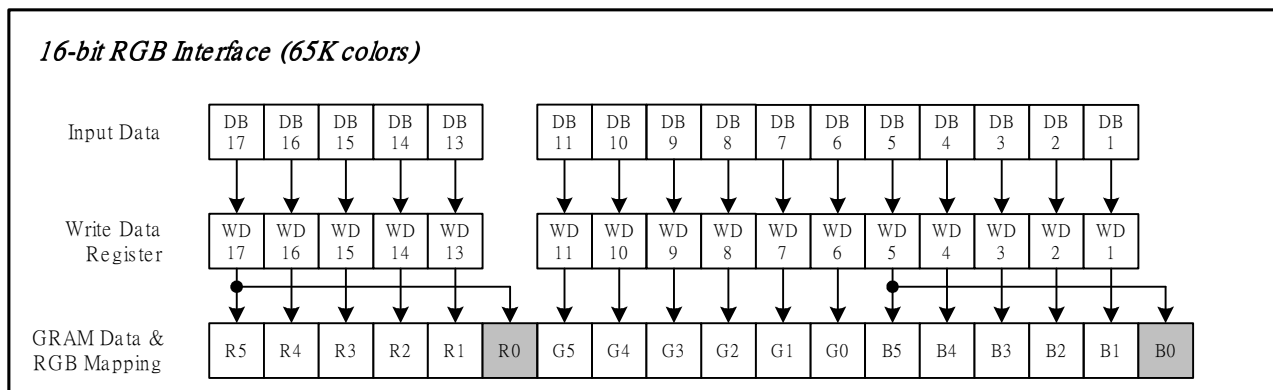
Data transfer synchronization in 6-bit RGB interface mode

ILI9325D has data transfer counters to count the first, second, third data transfers in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state. Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.



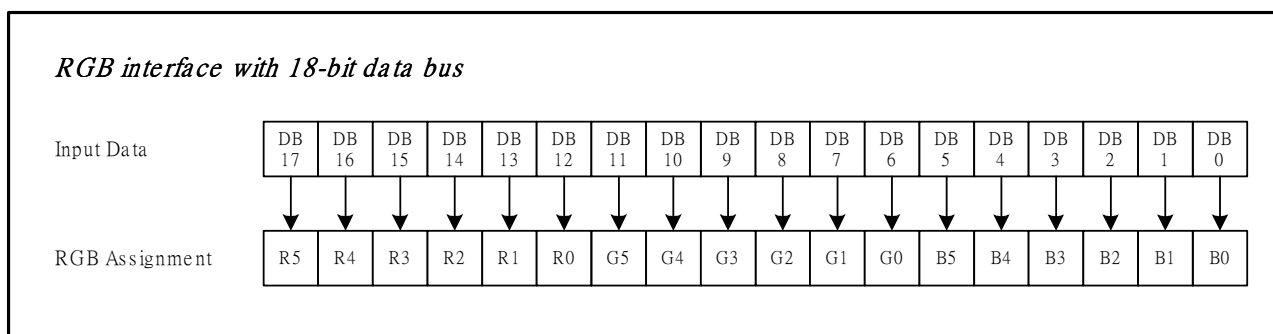
7.5.5. 16-bit RGB Interface

The 16-bit RGB interface is selected by setting the RIM[1:0] bits to "01". The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus (DB17-13, DB11-1) according to the data enable signal (ENABLE). Registers are set only via the system interface.



7.5.6. 18-bit RGB Interface

The 18-bit RGB interface is selected by setting the RIM[1:0] bits to "00". The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE). Registers are set only via the system interface.



Notes in using the RGB Input Interface

1. The following are the functions not available in RGB Input Interface mode.

Function	RGB interface	I80 system interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

2. VSYNC, HSYNC, and DOTCLK signals must be supplied throughout a display operation period.
3. The periods set with the NOWE[2:0] bits (gate output non-overlap period), are not based on the internal clock but based on DOTCLK in RGB interface mode.
4. In 6-bit RGB interface mode, each of RGB dots is transferred in synchronization with a DOTCLK input. In

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- other words, it takes 3 DOTCLK inputs to transfer one pixel. Be sure to complete data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode.
- In 6-bit RGB interface mode, data of one pixel, which consists of RGB dots, are transferred in units of 3 DOTCLK. Accordingly, set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC, ENABLE, DB[17:0]) to contain DOTCLK inputs of a multiple of 3 to complete data transfer in units of pixels.
 - When switching from the internal operation mode to the RGB Input Interface mode or the other way around, must follow the sequence below, and the new operation mode will be valid after one frame display is completed.
 - In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
 - In RGB interface mode, a RAM address (AD[16:0]) is set in the address counter every frame on the falling edge of VSYNC.

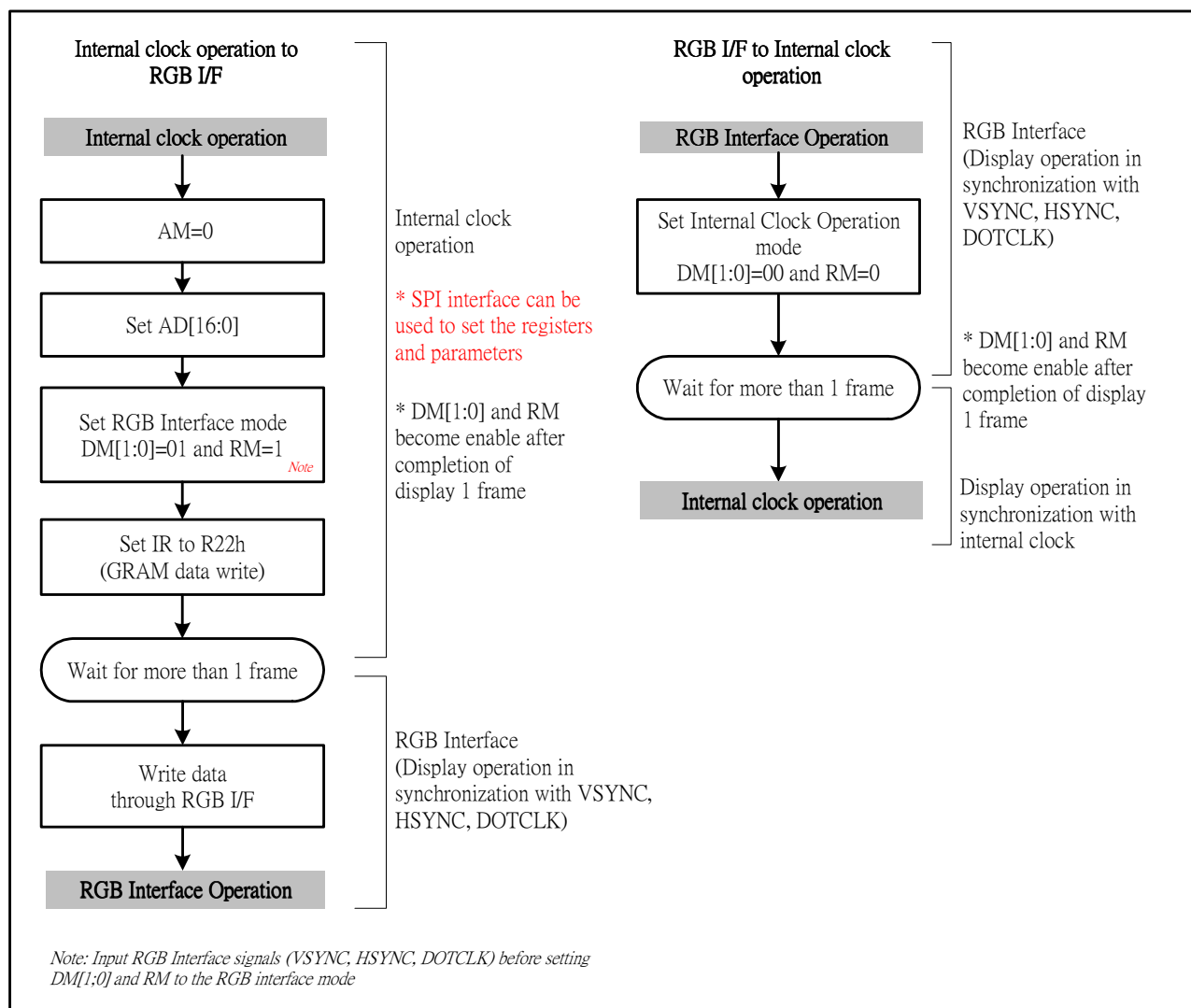


Figure 18 Internal clock operation/RGB interface mode switching

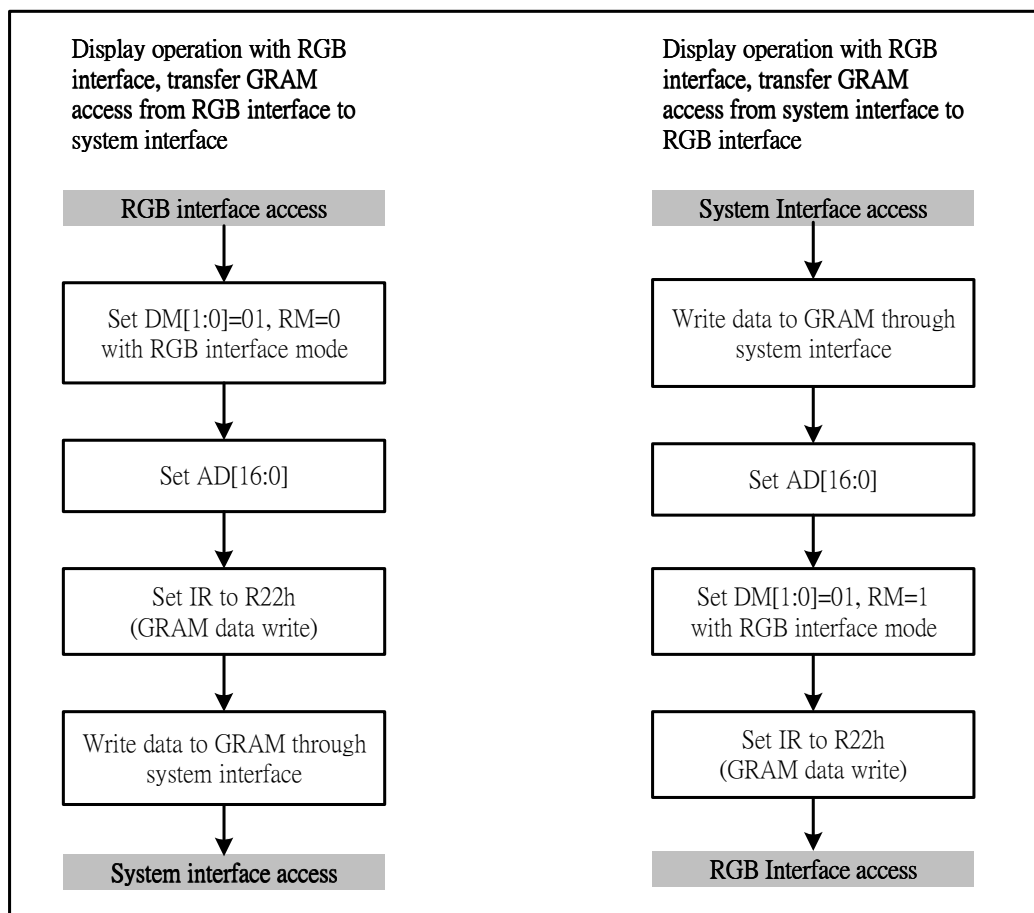


Figure 19 Transition of GRAM access between system interface and RGB interface

7.6. Interface Timing

The following are diagrams of interfacing timing with LCD panel control signals in internal operation and RGB interface modes.

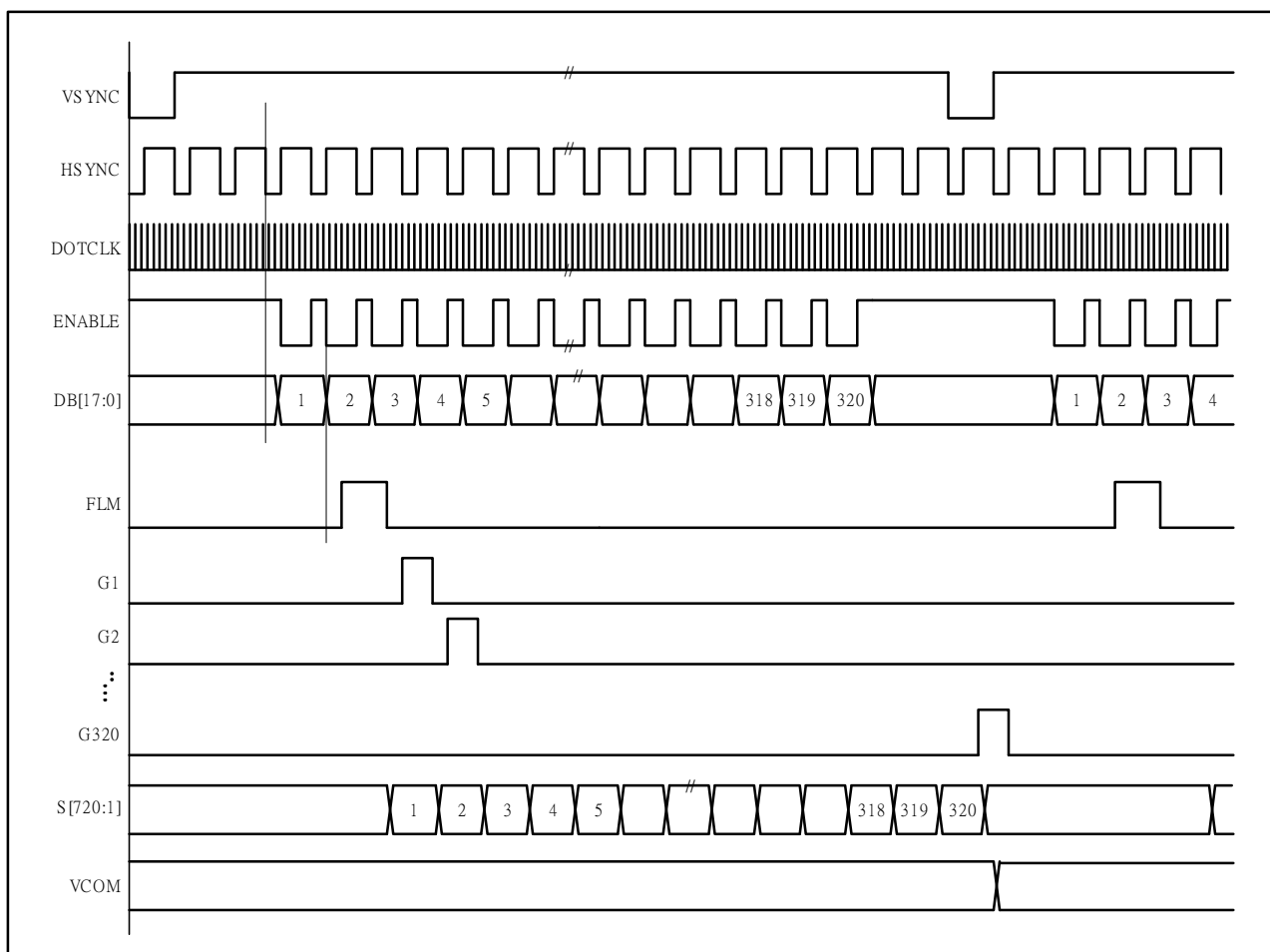
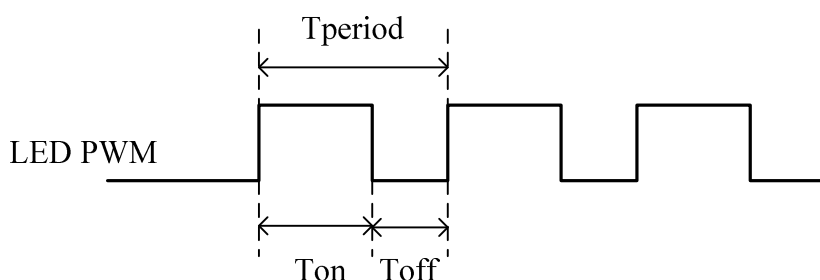


Figure 20 Relationship between RGB I/F signals and LCD Driving Signals for Panel

7.7. CABC (Content Adaptive Brightness Control)

ILI9325D provide a dynamic backlight control function as CABC (Content adaptive brightness control) to reduce the power consumption of the luminance source. ILI9325D will refer to the gray scale content of display image to output a PWM waveform to LED driver for backlight brightness control. Content adaptation means that the content of gray sale can be increased while simultaneously lowering brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and thus the power consumption reduction depend on the content of the image.

ILI9325D can calculate the backlight brightness level and send a PWM pulse to LED driver via LEDPWM pin for backlight brightness control purpose. The figure in the following is the basic timing diagram which is applied ILI9325D to control LED driver.



The period T_{period} of PWM pulse can be changed by the PWM_DIV[7:0] bits of the command "PWM_DIV (C8h)". The LED-on time T_{on} and the LED-off time T_{off} are decided by the backlight brightness level which is calculated with CABC in ILI9325D. If CABC is off, then LEDPWM will forced to "H" level.

The PWM period value will be calculated via the equation as below.

$$f_{\text{PWM_OUT}} = \frac{5.8\text{MHz}}{(\text{PWM_DIV}[7:0] + 1) \times 255}$$

8. Register Descriptions

8.1. Registers Access

ILI9325D adopts 18-bit bus interface architecture for high-performance microprocessor. All the functional blocks of ILI9325D starts to work after receiving the correct instruction from the external microprocessor by the 18-, 16-, 9-, 8-bit interface. The index register (IR) stores the register address to which the instructions and display data will be written. The register selection signal (RS), the read/write signals (nRD/nWR) and data bus D17-0 are used to read/write the instructions and data of ILI9325D. The registers of the ILI9325D are categorized into the following groups.

1. Specify the index of register (IR)
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address (AC)
7. Transfer data to/from the internal GRAM (R22)
8. Internal grayscale γ -correction (R30 ~ R39)

Normally, the display data (GRAM) is most often updated, and in order since the ILI9325D can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there are fewer loads on the program in the microprocessor. As the following figure shows, the way of assigning data to the 16 register bits (D[15:0]) varies for each interface. Send registers in accordance with the following data transfer format.

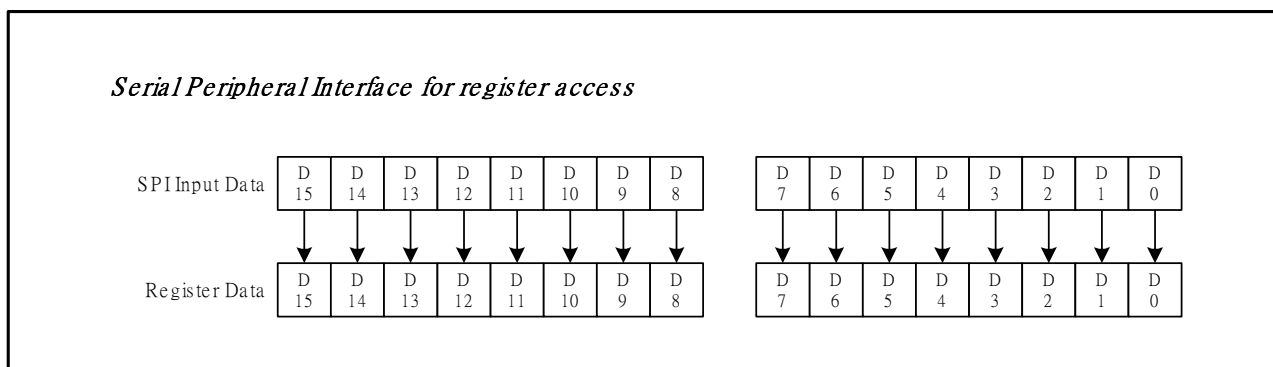
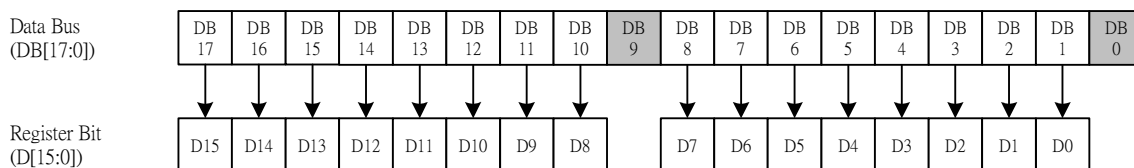
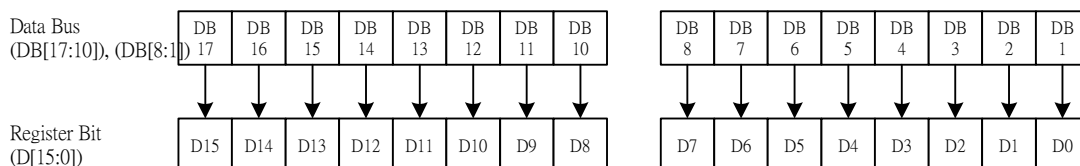


Figure 21 Register Setting with Serial Peripheral Interface (SPI)

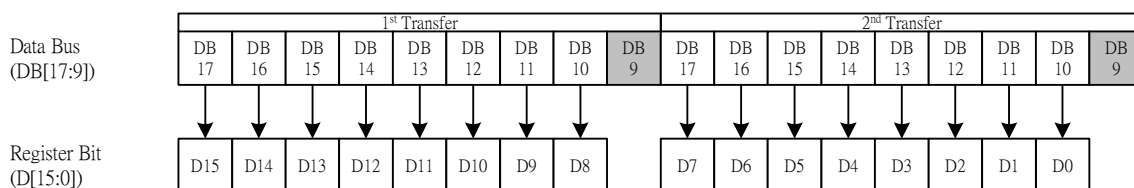
i80 system 18-bit data bus interface



i80 system 16-bit data bus interface



i80 system 9-bit data bus interface



i80 system 8-bit data bus interface

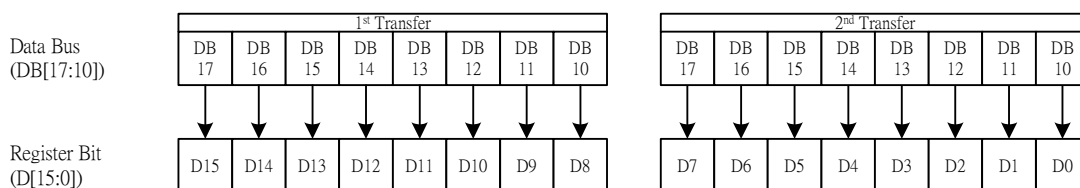
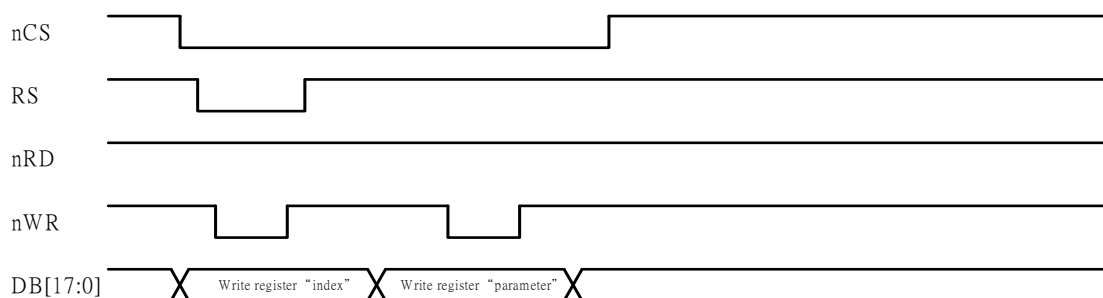


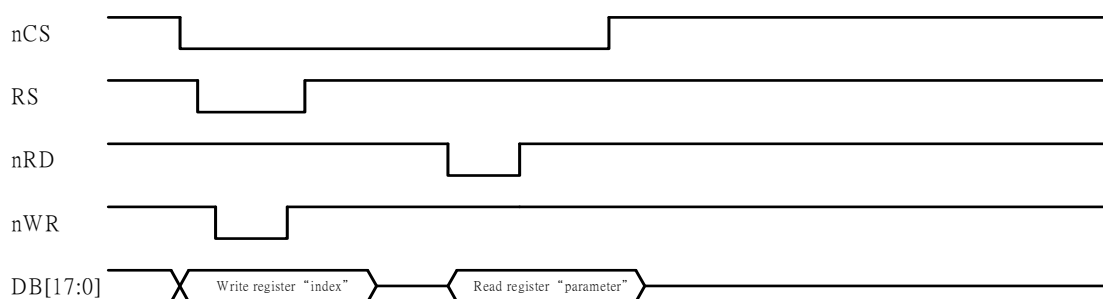
Figure 22 Register setting with i80 System Interface

i80 18-/16-bit System Bus Interface Timing

(a) Write to register

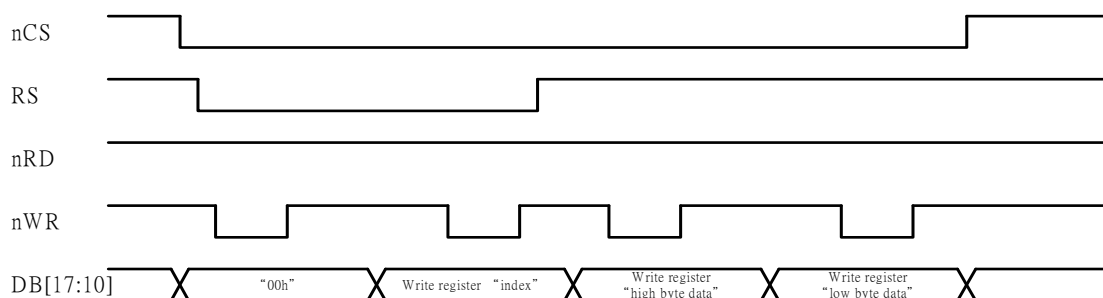


(b) Read from register



i80 9-/8-bit System Bus Interface Timing

(a) Write to register



(b) Read from register

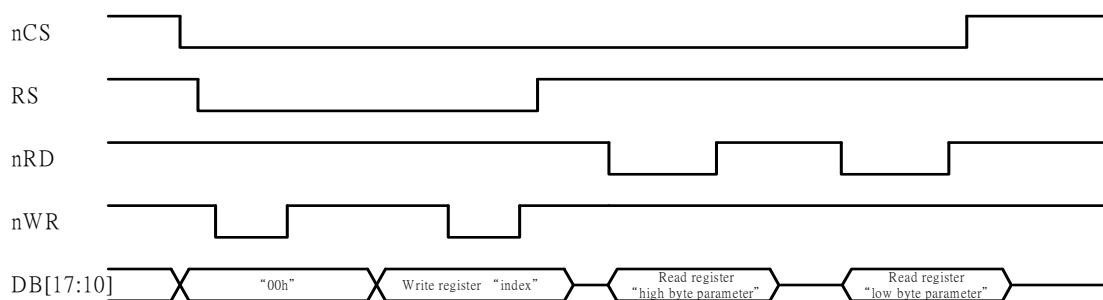


Figure 23 Register Read/Write Timing of i80 System Interface

8.2. Instruction Descriptions

No.	Registers Name	R/W	RS		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0		-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
00h	Driver Code Read	RO	1		1	0	0	1	0	0	1	1	0	0	1	0	0	1	0	1
01h	Driver Output Control 1	W	1		0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
02h	LCD Driving Control	W	1		0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
03h	Entry Mode	W	1		TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D1	I/D0	AM	0	0	0
05h	16 bits data format control	W	1		0	0	0	0	0	0	0	0	0	0	0	0	0	0	EPF1	EPF0
07h	Display Control 1	W	1		0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
08h	Display Control 2	W	1		0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
09h	Display Control 3	W	1		0	0	0	0	0	0	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
0Ah	Display Control 4	W	1		0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
0Ch	RGB Display Interface Control 1	W	1		0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
0Dh	Frame Maker Position	W	1		0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
0Fh	RGB Display Interface Control 2	W	1		0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
10h	Power Control 1	W	1		0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB
11h	Power Control 2	W	1		0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
12h	Power Control 3	W	1		0	0	0	0	0	0	0	0	VCIRE	0	0	0	VRH3	VRH2	VRH1	VRH0
13h	Power Control 4	W	1		0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
20h	Horizontal GRAM Address Set	W	1		0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
21h	Vertical GRAM Address Set	W	1		0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
22h	Write Data to GRAM	W	1		RAM write data (WD17-0) / read data (RD17-0) bits are transferred via different data bus lines according to the selected interfaces.															
29h	Power Control 7	W	1		0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
2Bh	Frame Rate and Color Control	W	1		0	0	0	0	0	0	0	0	0	0	0	0	FRS[3]	FRS[2]	FRS[1]	FRS[0]
30h	Gamma Control 1	W	1		0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
31h	Gamma Control 2	W	1		0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
32h	Gamma Control 3	W	1		0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
35h	Gamma Control 4	W	1		0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
36h	Gamma Control 5	W	1		0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
37h	Gamma Control 6	W	1		0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
38h	Gamma Control 7	W	1		0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
39h	Gamma Control 8	W	1		0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
3Ch	Gamma Control 9	W	1		0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]

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No.	Registers Name	R/W	RS		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
3Dh	Gamma Control 10	W	1		0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]
50h	Horizontal Address Start Position	W	1		0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
51h	Horizontal Address End Position	W	1		0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
52h	Vertical Address Start Position	W	1		0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
53h	Vertical Address End Position	W	1		0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
60h	Driver Output Control 2	W	1		GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
61h	Base Image Display Control	W	1		0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
66h	SPI Read/Write Control	W	1		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/WX (0)
6Ah	Vertical Scroll Control	W	1		0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
80h	Partial Image 1 Display Position	W	1		0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00
81h	Partial Image 1 Area (Start Line)	W	1		0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00
82h	Partial Image 1 Area (End Line)	W	1		0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00
83h	Partial Image 2 Display Position	W	1		0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10
84h	Partial Image 2 Area (Start Line)	W	1		0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10
85h	Partial Image 2 Area (End Line)	W	1		0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10
90h	Panel Interface Control 1	W	1		0	0	0	0	0	0	DIV11	DIV10	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
92h	Panel Interface Control 2	W	1		0	0	0	0	0	NOW12	NOW11	NOW10	0	0	0	0	0	0	0	0
95h	Panel Interface Control 4	W	1		0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0
97h	Panel Interface Control 5	W	1		0	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0
A0h	OTP ID Code Programming Control	W	1		0	0	0	0	0	0	0	0	OTP_ID_EN	0	0	0	OTP_ID[3:0]			
A1h	OTP VCM Programming Control	W	1		0	0	0	0	OTP_PGM_EN	0	0	0	0	0	VCM_OTP5	VCM_OTP4	VCM_OTP3	VCM_OTP2	VCM_OTP1	VCM_OTP0
A2h	OTP VCM Status and Enable	W	1		PGM_CNT1	PGM_CNT0	VCM_D5	VCM_D4	VCM_D3	VCM_D2	VCM_D1	VCM_D0	0	0	0	0	0	0	0	VCM_EN
A5h	OTP Programming ID Key	W	1		KEY_15	KEY_14	KEY_13	KEY_12	KEY_11	KEY_10	KEY_9	KEY_8	KEY_7	KEY_6	KEY_5	KEY_4	KEY_3	KEY_2	KEY_1	KEY_0
B1h	Write Display Brightness	W	1		0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
B2h	Read Display Brightness	R	1		0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
B3h	Write CTRL Display value	W	1		0	0	0	0	0	0	0	0	0	0	BCTRL	0	DD	BL	0	0
B4h	Read CTRL Display value	R	1		0	0	0	0	0	0	0	0	0	0	BCTRL	0	DD	BL	0	0

No.	Registers Name	R/W	RS		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
B5h	Write Content Adaptive Brightness Control value	W	1		0	0	0	0	0	0	0	0	0	0	0	0	0	0	C[1:0]	
B6h	Read Content Adaptive Brightness Control value	R	1		0	0	0	0	0	0	0	0	0	0	0	0	0	0	C[1:0]	
BEh	Write CABC Minimum Brightness	W	1		0	0	0	0	0	0	0	0	CMB[7:0]							
BFh	Read CABC Minimum Brightness	R	1		0	0	0	0	0	0	0	0	CMB[7:0]							
C8h	CABC Control 1	W	1		0	0	0	0	0	0	0	0	PWM_DIV[7:0]							
C9h	CABC Control 2	W	1		0	0	0	0	0	0	0	0	THRES_MOV[3:0]				THRES_STILL[3:0]			
CAh	CABC Control 3	W	1		0	0	0	0	0	0	0	0	0	0	0	0	THRES_UI[3:0]			
CBh	CABC Control 4	W	1		0	0	0	0	0	0	0	0	DTH_MOV[3:0]				DTH_STILL[3:0]			
CCh	CABC Control 5	W	1		0	0	0	0	0	0	0	0	0	0	0	0	DTH_UI[3:0]			
CDh	CABC Control 6	W	1		0	0	0	0	0	0	0	0	DIM_OPT2[3:0]				0	DIM_OPT1[2:0]		
DDh	Digital Gamma Control 1	W	1		0	0	0	0	0	0	0	0	RCS1	RCA0[2:0]			BCS1	BCA0[2:0]		
		W	1		0	0	0	0	0	0	0	0	RCSx	RCAx[2:0]			BCSx	BCAx[2:0]		
		W	1		0	0	0	0	0	0	0	0	RCS15	RCA15[2:0]			BCS15	BCA15[2:0]		
DEh	Digital Gamma Control 2	W	1		0	0	0	0	0	0	0	0	RFA0[3:0]				BFA0[3:0]			
		W	1		0	0	0	0	0	0	0	0	RFAx[3:0]				BFAx[3:0]			
		W	1		0	0	0	0	0	0	0	0	RFA63[3:0]				BFA63[3:0]			

8.2.1. Index (IR)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the address of register (R00h ~ RFFh) or RAM which will be accessed.

8.2.2. ID code (R00h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RO	1	1	0	0	1	0	0	1	1	0	0	1	0	0	1	0	1

The device code "9325" is read out when read this register.

8.2.3. Driver Output Control (R01h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SS: Select the shift direction of outputs from the source driver.

- When SS = 0, the shift direction of outputs is from S1 to S720
- When SS = 1, the shift direction of outputs is from S720 to S1.

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins.

- To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0.
- To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1.

When changing SS or BGR bits, RAM data must be rewritten.

SM: Sets the gate driver pin arrangement in combination with the GS bit (R60h) to select the optimal scan mode for the module.

SM	GS	Scan Direction	Gate Output Sequence
0	0		<p>G1, G2, G3, G4, ..., G316</p> <p>G317, G318, G319, G320</p>
0	1		<p>G320, G319, G318, ...,</p> <p>G6, G5, G4, G3, G2, G1</p>
1	0		<p>G1, G3, G5, G7, ..., G311</p> <p>G313, G315, G317, G319</p> <p>G2, G4, G6, G8, ..., G312</p> <p>G314, G316, G318, G320</p>
1	1		<p>G320, G318, G316, ...,</p> <p>G10, G8, G6, G4, G2</p> <p>G319, G317, G315, ...,</p> <p>G9, G7, G5, G3, G1</p>

8.2.4. LCD Driving Wave Control (R02h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

B/C 0 : Frame/Field inversion

1 : Line inversion

8.2.5. Entry Mode (R03h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D1	I/D0	AM	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

AM Control the GRAM update direction.

- When AM = "0", the address is updated in horizontal writing direction.

- When AM = "1", the address is updated in vertical writing direction.

When a window area is set by registers R50h ~R53h, only the addressed GRAM area is updated based on I/D[1:0] and AM bits setting.

I/D[1:0] Control the address counter (AC) to automatically increase or decrease by 1 when update one pixel display data. Refer to the following figure for the details.

	I/D[1:0] = 00 Horizontal : decrement Vertical : decrement	I/D[1:0] = 01 Horizontal : increment Vertical : decrement	I/D[1:0] = 10 Horizontal : decrement Vertical : increment	I/D[1:0] = 11 Horizontal : increment Vertical : increment
AM = 0 Horizontal				
AM = 1 Vertical				

Figure 24 GRAM Access Direction Setting

ORG Moves the origin address according to the ID setting when a window address area is made. This function is enabled when writing data with the window address area using high-speed RAM write.

ORG = "0": The origin address is not moved. In this case, specify the address to start write operation according to the GRAM address map within the window address area.

ORG = "1": The original address "00000h" moves according to the I/D[1:0] setting.

Notes 1: When *ORG*=1, only the origin address address"00000h" can be set in the *GRAM* address set registers *R20h*, and *R21h*.

2: In *GRAM* read operation, make sure to set *ORG*=0.

BGR Swap the R and B order of written data.

BGR="0": Follow the RGB order to write the pixel data.

BGR="1": Swap the RGB data to BGR in writing into *GRAM*.

TRI When *TRI* = "1", data are transferred to the internal RAM in 8-bit x 3 transfers mode via the 8-bit interface.

It is also possible to send data via the 16-bit interface or SPI (3W, 4W) in the transfer mode that realizes display in 262k colors in combination with DFM bits. When not using these interface modes, be sure to set *TRI* = "0".

DFM Set the mode of transferring data to the internal RAM when *TRI* = "1". See the following figures for details.

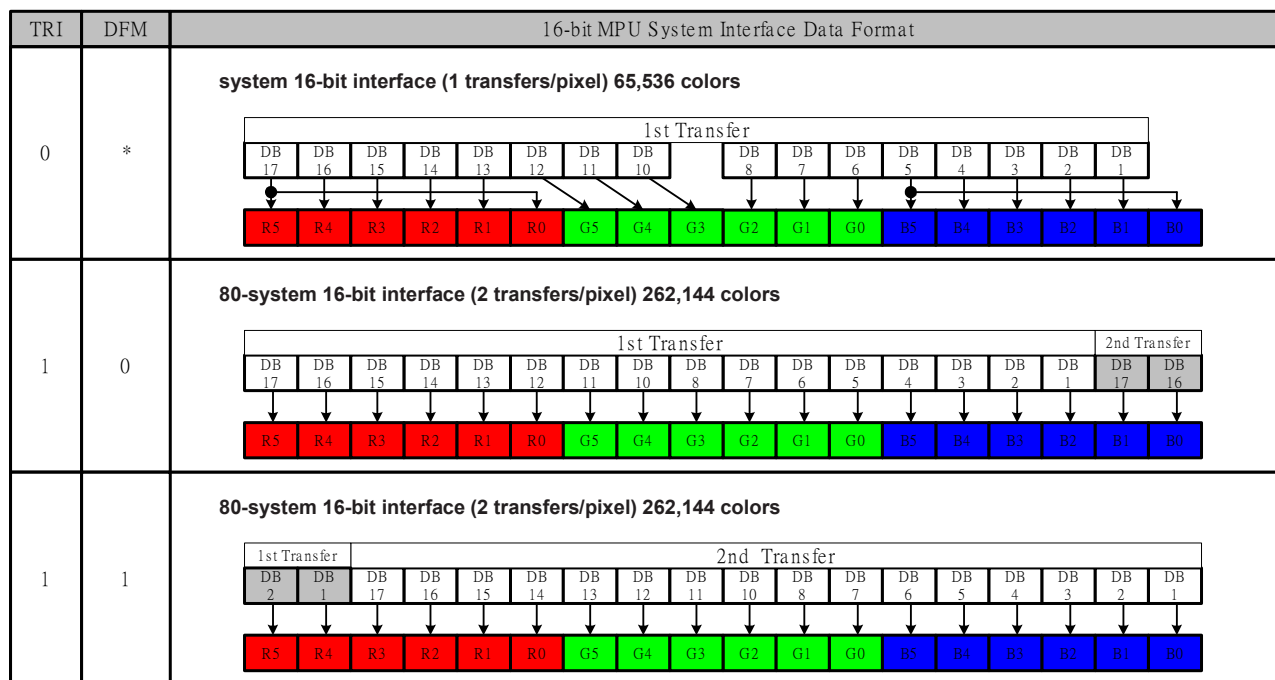


Figure 25 16-bit MPU System Interface Data Format

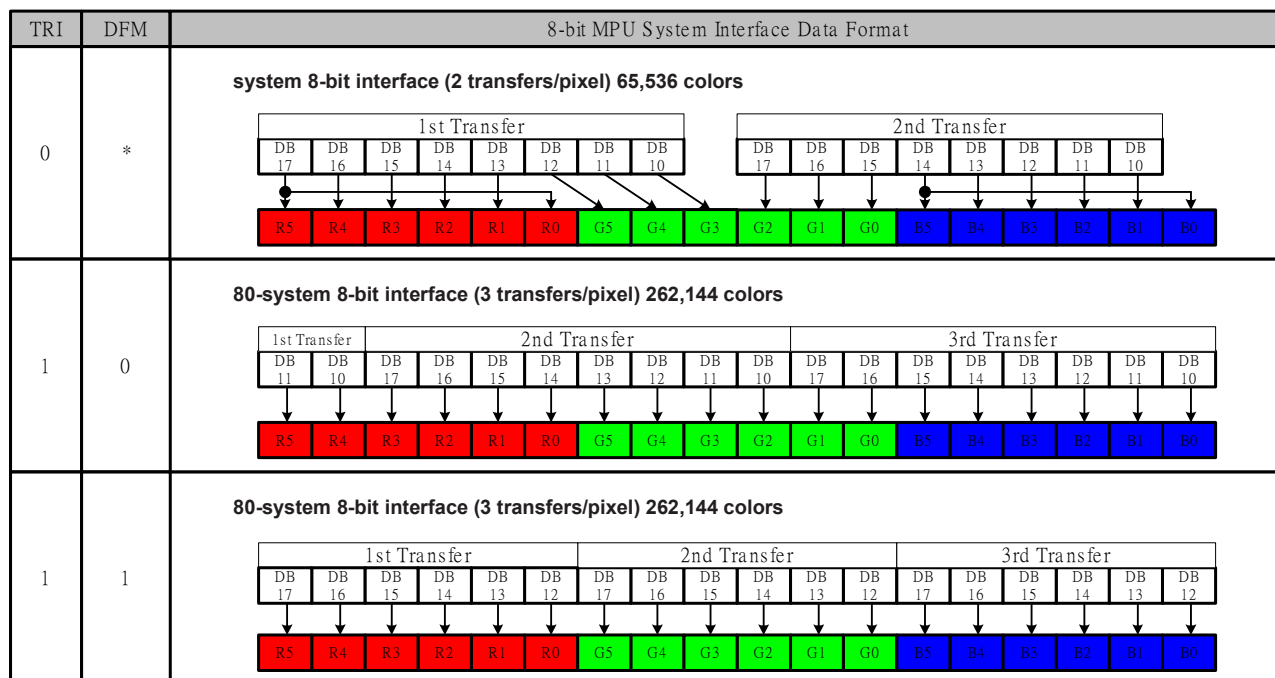
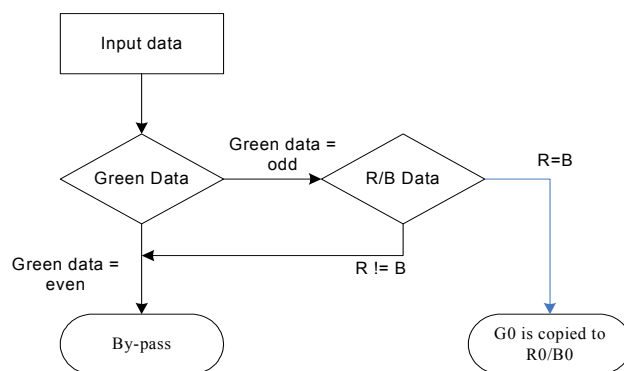
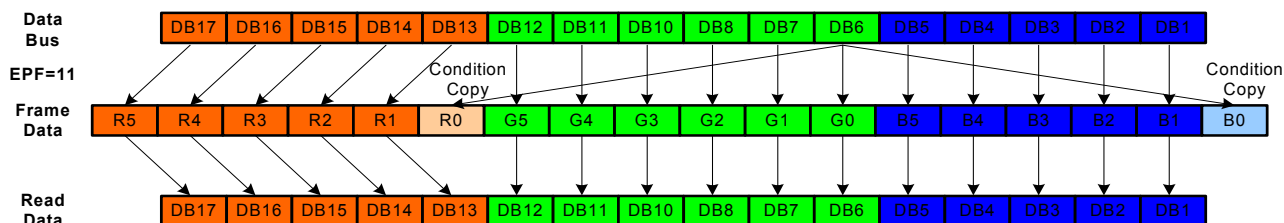
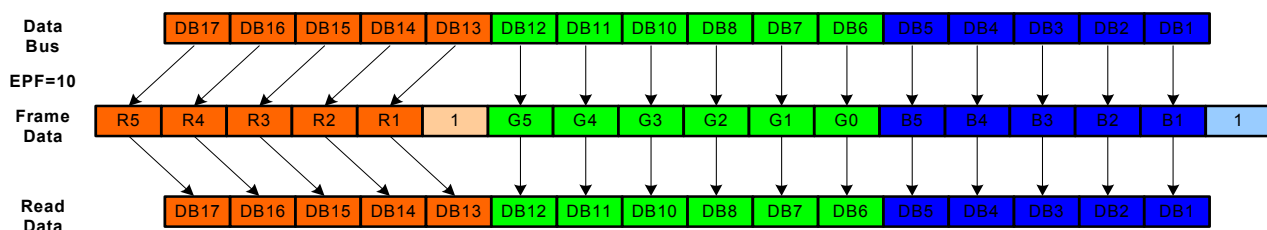
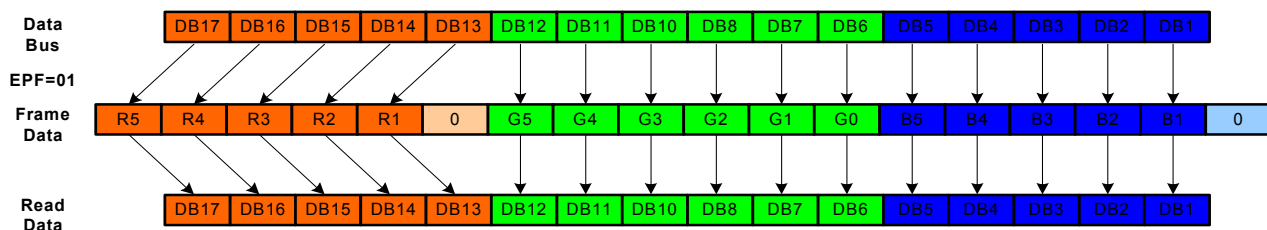
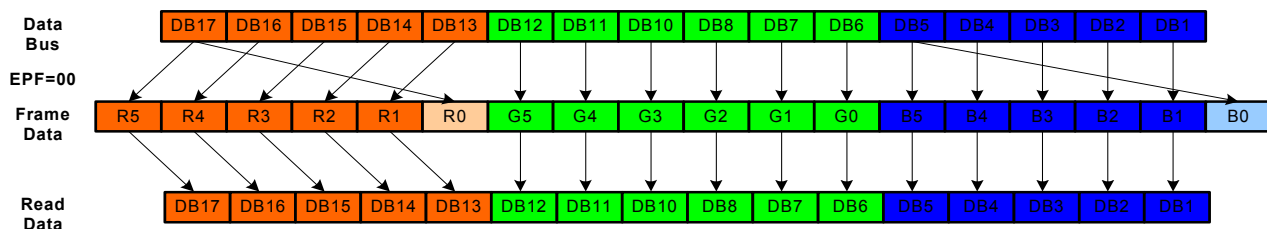


Figure 26 8-bit MPU System Interface Data Format

8.2.6. 16bits Data Format Selection (R05h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EPF1	EPF0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



8.2.7. Display Control 1 (R07h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D[1:0] Set D[1:0]="11" to turn on the display panel, and D[1:0]="00" to turn off the display panel.

A graphics display is turned on the panel when writing D1 = "1", and is turned off when writing D1 = "0". When writing D1 = "0", the graphics display data is retained in the internal GRAM and the ILI9325D displays the data when writing D1 = "1". When D1 = "0", i.e. while no display is shown on the panel, all source outputs becomes the GND level to reduce charging/discharging current, which is generated within the LCD while driving liquid crystal with AC voltage.

When the display is turned off by setting D[1:0] = "01", the ILI9325D continues internal display operation.

When the display is turned off by setting D[1:0] = "00", the ILI9325D internal display operation is halted completely. In combination with the GON, DTE setting, the D[1:0] setting controls display ON/OFF.

D1	D0	BASEE	Source, VCOM Output	ILI9325D internal operation
0	0	0	GND	Halt
0	1	1	GND	Operate
1	0	0	Non-lit display	Operate
1	1	0	Non-lit display	Operate
1	1	1	Base image display	Operate

Note: 1. data write operation from the microcontroller is performed irrespective of the setting of D[1:0] bits.

2. The D[1:0] setting is valid on both 1st and 2nd displays.

3. The non-lit display level from the source output pins is determined by instruction (PTS).

CL When CL = "1", the 8-color display mode is selected.

CL	Colors
0	262,144
1	8

GON and DTE Set the output level of gate driver G1 ~ G320 as follows

GON	DTE	G1 ~G320 Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	1	Normal Display

BASEE Base image display enable bit. When BASEE = "0", no base image is displayed. The ILI9325D drives liquid crystal at non-lit display level or displays only partial images. When BASEE = "1", the base image is displayed. The D[1:0] setting has higher priority over the BASEE setting.

PTDE[1:0] Partial image 2 and Partial image 1 enable bits

- PTDE1/0 = 0: turns off partial image. Only base image is displayed.
- PTDE1/0 = 1: turns on partial image. Set the base image display enable bit to 0 (BASEE = 0).

8.2.8. Display Control 2 (R08h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
Default		0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

FP[3:0]/BP[3:0] The FP[3:0] and BP[3:0] bits specify the line number of front and back porch periods respectively. When setting the FP[3:0] and BP[3:0] value, the following conditions shall be met:

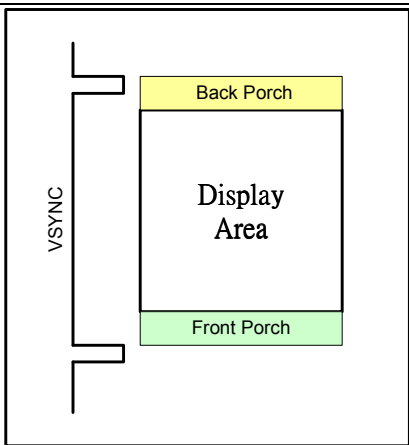
$BP + FP \leq 16$ lines

$FP \geq 2$ lines

$BP \geq 2$ lines

Set the BP[3:0] and FP[3:0] bits as below for each operation modes

Operation Mode	BP	FP	BP+FP
I80 System Interface Operation Mode	$BP \geq 2$ lines	$FP \geq 2$ lines	$FP + BP \leq 16$ lines
RGB interface Operation	$BP \geq 2$ lines	$FP \geq 2$ lines	$FP + BP \leq 16$ lines
VSYNC interface Operation	$BP \geq 2$ lines	$FP \geq 2$ lines	$FP + BP = 16$ lines

FP[3:0]	Number of lines for Front Porch	 <p>The diagram illustrates the vertical timing of the LCD display. A vertical line on the left represents the VSYNC signal. To its right is the Back Porch (yellow), followed by the Display Area (white), and then the Front Porch (green). The VSYNC signal is shown as a pulse that occurs before the Back Porch.</p>
BP[3:0]	Number of lines for Back Porch	
0000	Setting Prohibited	
0001	Setting Prohibited	
0010	2 lines	
0011	3 lines	
0100	4 lines	
0101	5 lines	
0110	6 lines	
0111	7 lines	
1000	8 lines	
1001	9 lines	
1010	10 lines	
1011	11 lines	
1100	12 lines	
1101	13 lines	
1110	14 lines	
1111	Setting Prohibited	

Note: The output timing to the LCD is delayed by 2 lines period from the input of synchronizing signal.

8.2.9. Display Control 3 (R09h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ISC[3:0]: Specify the scan cycle interval of gate driver in non-display area when PTG[1:0]="10" to select interval scan. Then scan cycle is set as odd number from 0~29 frame periods. The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	$f_{FLM}=60\text{ Hz}$
0	0	0	0	0 frame	-
0	0	0	1	0 frame	-
0	0	1	0	3 frame	50ms
0	0	1	1	5 frame	84ms
0	1	0	0	7 frame	117ms
0	1	0	1	9 frame	150ms
0	1	1	0	11 frame	184ms
0	1	1	1	13 frame	217ms
1	0	0	0	15 frame	251ms
1	0	0	1	17 frame	284ms
1	0	1	0	19 frame	317ms
1	0	1	1	21 frame	351ms
1	1	0	0	23 frame	384ms
1	1	0	1	25 frame	418ms
1	1	1	0	27 frame	451ms
1	1	1	1	29 frame	484ms

PTG[1:0] Set the scan mode in non-display area.

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	VCOM output
0	0	Normal scan	Set with the PTS[1:0] bits	VCOMH/VCOML
0	1	Setting Prohibited	-	-
1	0	Interval scan	Set with the PTS[1:0] bits	VCOMH/VCOML
1	1	Setting Prohibited	-	-

PTS[1:0] :Set the source output level in non-display area drive period (front/back porch period and blank area between partial displays).

PTS[1:0]		SOURCE / VCOM output level in non-display area driver period
00	frame with gate scan	white
	frame without gate scan	V63 / VCOML
01	frame with gate scan	black
	frame without gate scan	V0 / VCOML
10	frame with gate scan	white
	frame without gate scan	GND / GND
11	frame with gate scan	white
	frame without gate scan	Hi-Z / Hi-Z

8.2.10. Display Control 4 (R0Ah)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMI[2:0] Set the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMARKOE When FMARKOE=1, ILI9325D starts to output FMARK signal in the output interval set by FMI[2:0] bits.

FMI[2:0]	Output Interval
000	1 frame
001	2 frame
011	4 frame
101	6 frame
Others	Setting disabled

8.2.11. RGB Display Interface Control 1 (R0Ch)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIM[1:0] Select the RGB interface data width.

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (1 transfer/pixel), DB[17:0]
0	1	16-bit RGB interface (1 transfer/pixel), DB[17:13] and DB[11:1]
1	0	6-bit RGB interface (3 transfers/pixel), DB[17:12]
1	1	Setting disabled

Note1: Registers are set only by the system interface.

Note2: Be sure that one pixel (3 dots) data transfer finished when interface switch.

DM[1:0] Select the display operation mode.

DM1	DM0	Display Interface
0	0	Internal system clock
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

RM Select the interface to access the GRAM.

Set RM to "1" when writing display data by the RGB interface.

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM[1:0])
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM[1:0] = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
Rewrite still picture area while RGB interface Displaying moving pictures.		System interface (RM = 0)	RGB interface (DM[1:0] = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM[1:0] = 10)

Note 1: Registers are set only via the system interface or SPI interface.

Note 2: Refer to the flowcharts of "RGB Input Interface" section for the mode switch.

ENC[2:0] Set the GRAM write cycle through the RGB interface

ENC[2:0]	GRAM Write Cycle (Frame periods)
000	1 Frame
001	2 Frames
010	3 Frames
011	4 Frames
100	5 Frames
101	6 Frames
110	7 Frames
111	8 Frames

8.2.12. Frame Marker Position (R0Dh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMP[8:0] Sets the output position of frame cycle (frame marker).

When FMP[8:0]=0, a high-active pulse FMARK is output at the start of back porch period for one display line period (1H).

Make sure the $9'h000 \leq FMP \leq BP+NL+FP$

FMP[8:0]	FMARK Output Position
9'h000	0 th line
9'h001	1 st line
9'h002	2 nd line
9'h003	3 rd line
.	.
.	.
.	.
9'h175	373 rd line
9'h176	374 th line
9'h177	375 th line

8.2.13. RGB Display Interface Control 2 (R0Fh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DPL: Sets the signal polarity of the DOTCLK pin.

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DPL = "0" The data is input on the rising edge of DOTCLK

DPL = "1" The data is input on the falling edge of DOTCLK

EPL: Sets the signal polarity of the ENABLE pin.

EPL = "0" The data DB17-0 is written when ENABLE = "0". Disable data write operation when ENABLE = "1".

EPL = "1" The data DB17-0 is written when ENABLE = "1". Disable data write operation when ENABLE = "0".

HSPL: Sets the signal polarity of the HSYNC pin.

HSPL = "0" Low active

HSPL = "1" High active

VSPL: Sets the signal polarity of the VSYNC pin.

VSPL = "0" Low active

VSPL = "1" High active

8.2.14. Power Control 1 (R10h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SLP: When SLP = 1, ILI9325D enters the sleep mode and the display operation stops except the RC oscillator to reduce the power consumption. In the sleep mode, the GRAM data and instructions cannot be updated unless the driver exits sleep mode.(SLP = "0")

STB: When STB = 1, ILI9325D enters the standby mode and the display operation stops except the GRAM power supply to reduce the power consumption. In the STB mode, the GRAM data and instructions cannot be updated unless the driver exits standby mode.(STB = "0")

AP[2:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0] = "000" to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

AP[2:0]	Gamma driver amplifiers	Source driver amplifiers
000	Halt	Halt
001	1.00	1.00
010	1.00	0.75
011	1.00	0.50
100	0.75	1.00
101	0.75	0.75
110	0.75	0.50
111	0.50	0.50

SAP: Source Driver output control

SAP=0, Source driver is disabled.

SAP=1, Source driver is enabled.

When starting the charge-pump of LCD in the Power ON stage, make sure that SAP=0, and set the SAP=1, after starting up the LCD power supply circuit.

APE: Power supply enable bit.

Set APE = "1" to start the generation of power supply according to the power supply startup sequence.

BT[2:0]: Sets the factor used in the step-up circuits.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

BT[2:0]	DDVDH	VCL	VGH	VGL
3'h0	VCI1 x 2	- VCI1	VCI1 x 6	- VCI1 x 5
3'h1	VCI1 x 2	- VCI1		- VCI1 x 4
3'h2				- VCI1 x 3
3'h3	VCI1 x 2	- VCI1	VCI1 x 5	- VCI1 x 5
3'h4				- VCI1 x 4
3'h5				- VCI1 x 3
3'h6	VCI1 x 2	- VCI1	VCI1 x 4	- VCI1 x 4
3'h7				- VCI1 x 3

Notes: 1. Connect capacitors to the capacitor connection pins when generating DDVDH, VGH, VGL and VCL levels.

2. Make sure DDVDH = 6.0V (max.).

8.2.15. Power Control 2 (R11h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
Default		0	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0

VC[2:0] Sets the ratio factor of VCI to generate the reference voltages VCI1.

VC2	VC1	VC0	VCI1 voltage
0	0	0	0.95 x VCI
0	0	1	0.90 x VCI
0	1	0	0.85 x VCI
0	1	1	0.80 x VCI
1	0	0	0.75 x VCI
1	0	1	0.70 x VCI
1	1	0	Disabled
1	1	1	1.0 x VCI

DC0[2:0]: Selects the operating frequency of the step-up circuit 1. The higher step-up operating frequency

enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC1[2:0]: Selects the operating frequency of the step-up circuit 2. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC02	DC01	DC00	Step-up circuit1 step-up frequency (f_{DCDC1})
0	0	0	Fosc
0	0	1	Fosc / 2
0	1	0	Fosc / 4
0	1	1	Fosc / 8
1	0	0	Fosc / 16
1	0	1	Fosc / 32
1	1	0	Fosc / 64
1	1	1	Halt step-up circuit 1

DC12	DC11	DC10	Step-up circuit2 step-up frequency (f_{DCDC2})
0	0	0	Fosc / 4
0	0	1	Fosc / 8
0	1	0	Fosc / 16
0	1	1	Fosc / 32
1	0	0	Fosc / 64
1	0	1	Fosc / 128
1	1	0	Fosc / 256
1	1	1	Halt step-up circuit 2

Note: Be sure $f_{DCDC1} \geq f_{DCDC2}$ when setting DC0[2:0] and DC1[2:0].

8.2.16. Power Control 3 (R12h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	VCIRE	0	0	0	VRH3	VRH2	VRH1	VRH0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VRH[3:0] Set the amplifying rate (1.6 ~ 1.9) of VCI applied to output the VREG1OUT level, which is a reference level for the VCOM level and the grayscale voltage level.

VCIRE: Select the external reference voltage VCI or internal reference voltage VCIR.

VCIRE=0	External reference voltage VCI (default)
VCIRE =1	Internal reference voltage 2.5V

VCIRE =0				
VRH3	VRH2	VRH1	VRH0	VREG1OUT
0	0	0	0	Halt
0	0	0	1	VCI x 2.00
0	0	1	0	VCI x 2.05
0	0	1	1	VCI x 2.10
0	1	0	0	VCI x 2.20
0	1	0	1	VCI x 2.30
0	1	1	0	VCI x 2.40
0	1	1	1	VCI x 2.40
1	0	0	0	VCI x 1.60
1	0	0	1	VCI x 1.65
1	0	1	0	VCI x 1.70
1	0	1	1	VCI x 1.75
1	1	0	0	VCI x 1.80
1	1	0	1	VCI x 1.85
1	1	1	0	VCI x 1.90
1	1	1	1	VCI x 1.95

VCIRE =1				
VRH3	VRH2	VRH1	VRH0	VREG1OUT
0	0	0	0	Halt
0	0	0	1	2.5V x 2.00 = 5.000V
0	0	1	0	2.5V x 2.05 = 5.125V
0	0	1	1	2.5V x 2.10 = 5.250V
0	1	0	0	2.5V x 2.20 = 5.500V
0	1	0	1	2.5V x 2.30 = 5.750V
0	1	1	0	2.5V x 2.40 = 6.000V
0	1	1	1	2.5V x 2.40 = 6.000V
1	0	0	0	2.5V x 1.60 = 4.000V
1	0	0	1	2.5V x 1.65 = 4.125V
1	0	1	0	2.5V x 1.70 = 4.250V
1	0	1	1	2.5V x 1.75 = 4.375V
1	1	0	0	2.5V x 1.80 = 4.500V
1	1	0	1	2.5V x 1.85 = 4.625V
1	1	1	0	2.5V x 1.90 = 4.750V
1	1	1	1	2.5V x 1.95 = 4.875V

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When $V_{CI} < 2.5V$, Internal reference voltage will be same as V_{CI} .

Make sure that V_C and V_{RH} setting restriction: $V_{REG1OUT} \leq (DDVDH - 0.2)V$.

8.2.17. Power Control 4 (R13h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VDV[4:0] Select the factor of $V_{REG1OUT}$ to set the amplitude of VCOM alternating voltage from 0.70 to 1.24 x $V_{REG1OUT}$.

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude
0	0	0	0	0	$V_{REG1OUT} \times 0.70$
0	0	0	0	1	$V_{REG1OUT} \times 0.72$
0	0	0	1	0	$V_{REG1OUT} \times 0.74$
0	0	0	1	1	$V_{REG1OUT} \times 0.76$
0	0	1	0	0	$V_{REG1OUT} \times 0.78$
0	0	1	0	1	$V_{REG1OUT} \times 0.80$
0	0	1	1	0	$V_{REG1OUT} \times 0.82$
0	0	1	1	1	$V_{REG1OUT} \times 0.84$
0	1	0	0	0	$V_{REG1OUT} \times 0.86$
0	1	0	0	1	$V_{REG1OUT} \times 0.88$
0	1	0	1	0	$V_{REG1OUT} \times 0.90$
0	1	0	1	1	$V_{REG1OUT} \times 0.92$
0	1	1	0	0	$V_{REG1OUT} \times 0.94$
0	1	1	0	1	$V_{REG1OUT} \times 0.96$
0	1	1	1	0	$V_{REG1OUT} \times 0.98$
0	1	1	1	1	$V_{REG1OUT} \times 1.00$

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude
1	0	0	0	0	$V_{REG1OUT} \times 0.94$
1	0	0	0	1	$V_{REG1OUT} \times 0.96$
1	0	0	1	0	$V_{REG1OUT} \times 0.98$
1	0	0	1	1	$V_{REG1OUT} \times 1.00$
1	0	1	0	0	$V_{REG1OUT} \times 1.02$
1	0	1	0	1	$V_{REG1OUT} \times 1.04$
1	0	1	1	0	$V_{REG1OUT} \times 1.06$
1	0	1	1	1	$V_{REG1OUT} \times 1.08$
1	1	0	0	0	$V_{REG1OUT} \times 1.10$
1	1	0	0	1	$V_{REG1OUT} \times 1.12$
1	1	0	1	0	$V_{REG1OUT} \times 1.14$
1	1	0	1	1	$V_{REG1OUT} \times 1.16$
1	1	1	0	0	$V_{REG1OUT} \times 1.18$
1	1	1	0	1	$V_{REG1OUT} \times 1.20$
1	1	1	1	0	$V_{REG1OUT} \times 1.22$
1	1	1	1	1	$V_{REG1OUT} \times 1.24$

Set VDV[4:0] to let VCOM amplitude less than 6V.

8.2.18. GRAM Horizontal/Vertical Address Set (R20h, R21h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AD[16:0] Set the initial value of address counter (AC).

The address counter (AC) is automatically updated in accordance to the setting of the AM, I/D bits as data is written to the internal GRAM. The address counter is not automatically updated when read data from the internal GRAM.

AD[16:0]	GRAM Data Map
17'h00000 ~ 17'h000EF	1 st line GRAM Data
17'h00100 ~ 17'h001EF	2 nd line GRAM Data
17'h00200 ~ 17'h002EF	3 rd line GRAM Data
17'h00300 ~ 17'h003EF	4 th line GRAM Data
17'h13D00 ~ 17'h13DEF	318 th line GRAM Data
17'h13E00 ~ 17'h13EEF	319 th line GRAM Data
17'h13F00 ~ 17'h13FEF	320 th line GRAM Data

Note1: When the RGB interface is selected (RM = "1"), the address AD[16:0] is set to the address counter every frame on the falling edge of VSYNC.

8.2.19. Write Data to GRAM (R22h)

R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	RAM write data (WD[17:0], the DB[17:0] pin assignment differs for each interface.																	

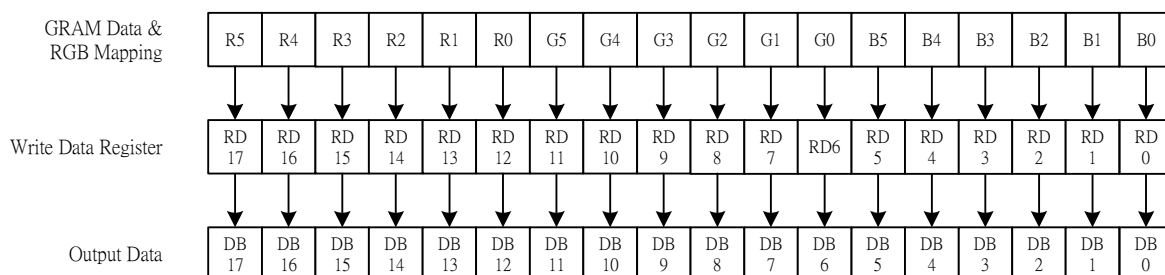
This register is the GRAM access port. When update the display data through this register, the address counter (AC) is increased/decreased automatically.

8.2.20. Read Data from GRAM (R22h)

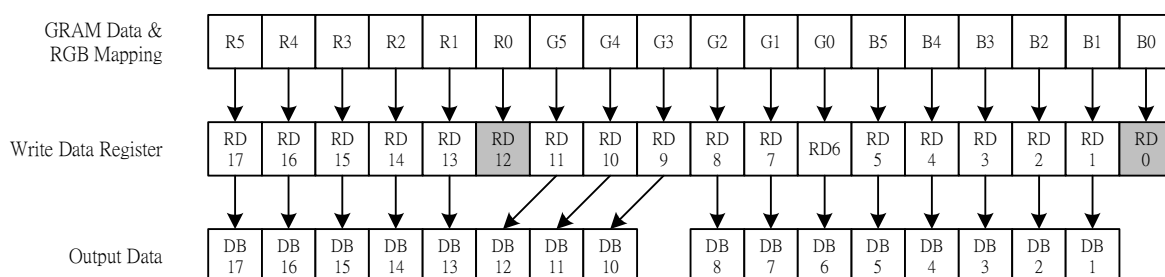
R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	RAM Read Data (RD[17:0], the DB[17:0] pin assignment differs for each interface.																	

RD[17:0] Read 18-bit data from GRAM through the read data register (RDR).

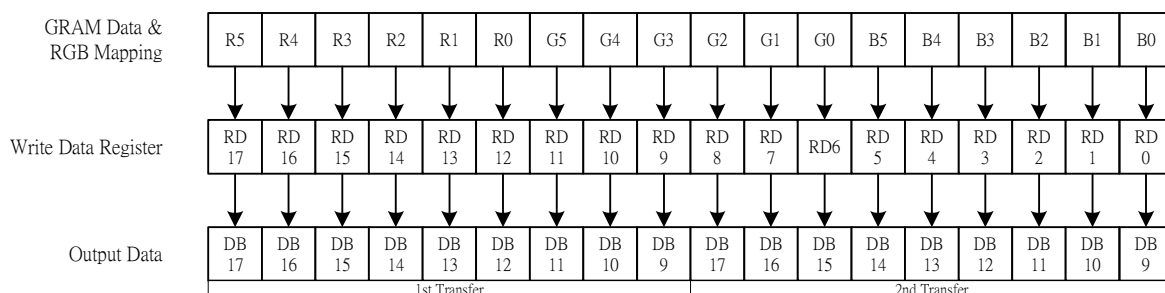
18-bit System Interface



16-bit System Interface



9-bit System Interface



8-bit System Interface

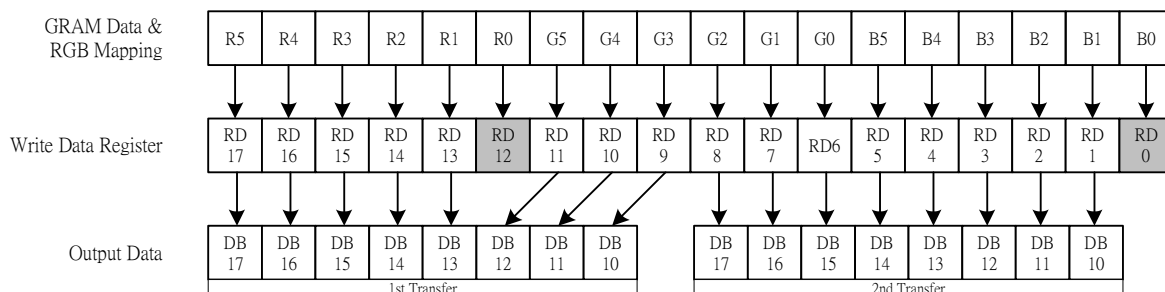


Figure 27 Data Read from GRAM through Read Data Register in 18-/16-/9-/8-bit Interface Mode

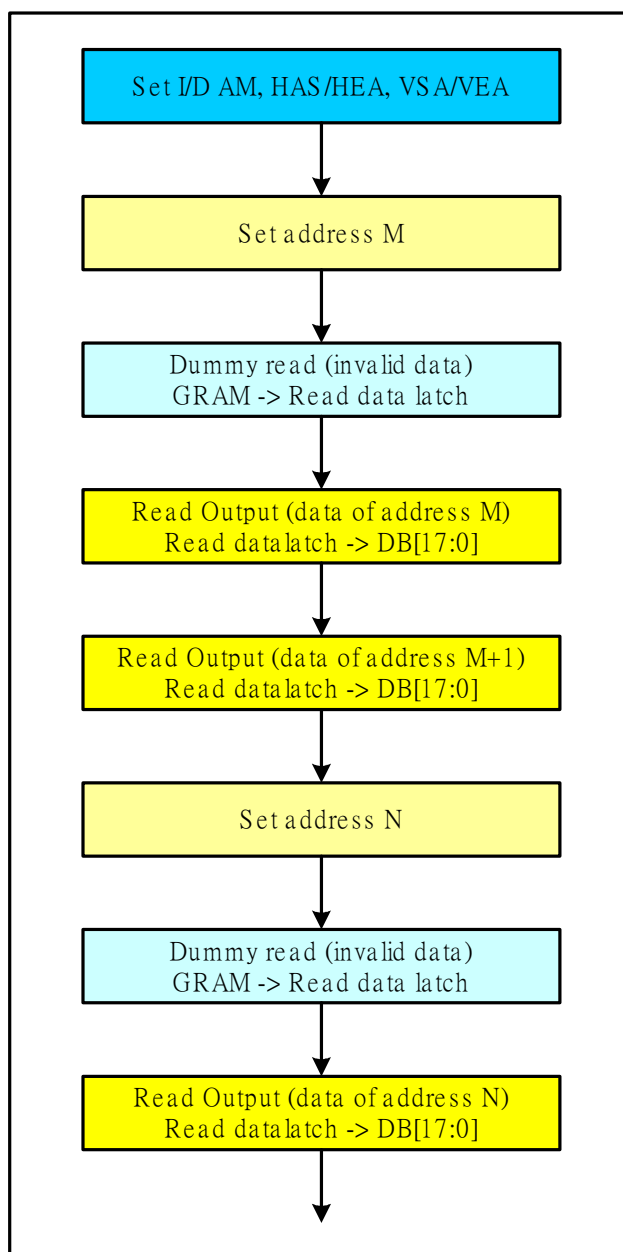


Figure 28 GRAM Data Read Back Flow Chart

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8.2.21. Power Control 7 (R29h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCM[5:0] Set the internal VCOMH voltage.

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	0	VREG1OUT x 0.685
0	0	0	0	0	1	VREG1OUT x 0.690
0	0	0	0	1	0	VREG1OUT x 0.695
0	0	0	0	1	1	VREG1OUT x 0.700
0	0	0	1	0	0	VREG1OUT x 0.705
0	0	0	1	0	1	VREG1OUT x 0.710
0	0	0	1	1	0	VREG1OUT x 0.715
0	0	0	1	1	1	VREG1OUT x 0.720
0	0	1	0	0	0	VREG1OUT x 0.725
0	0	1	0	0	1	VREG1OUT x 0.730
0	0	1	0	1	0	VREG1OUT x 0.735
0	0	1	0	1	1	VREG1OUT x 0.740
0	0	1	1	0	0	VREG1OUT x 0.745
0	0	1	1	0	1	VREG1OUT x 0.750
0	0	1	1	1	0	VREG1OUT x 0.755
0	0	1	1	1	1	VREG1OUT x 0.760
0	1	0	0	0	0	VREG1OUT x 0.765
0	1	0	0	0	1	VREG1OUT x 0.770
0	1	0	0	1	0	VREG1OUT x 0.775
0	1	0	0	1	1	VREG1OUT x 0.780
0	1	0	1	0	0	VREG1OUT x 0.785
0	1	0	1	0	1	VREG1OUT x 0.790
0	1	0	1	1	0	VREG1OUT x 0.795
0	1	0	1	1	1	VREG1OUT x 0.800
0	1	1	0	0	0	VREG1OUT x 0.805
0	1	1	0	0	1	VREG1OUT x 0.810
0	1	1	0	1	0	VREG1OUT x 0.815
0	1	1	0	1	1	VREG1OUT x 0.820
0	1	1	1	0	0	VREG1OUT x 0.825
0	1	1	1	0	1	VREG1OUT x 0.830
0	1	1	1	1	0	VREG1OUT x 0.835
0	1	1	1	1	1	VREG1OUT x 0.840

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
1	0	0	0	0	0	VREG1OUT x 0.845
1	0	0	0	0	1	VREG1OUT x 0.850
1	0	0	0	1	0	VREG1OUT x 0.855
1	0	0	0	1	1	VREG1OUT x 0.860
1	0	0	1	0	0	VREG1OUT x 0.865
1	0	0	1	0	1	VREG1OUT x 0.870
1	0	0	1	1	0	VREG1OUT x 0.875
1	0	0	1	1	1	VREG1OUT x 0.880
1	0	1	0	0	0	VREG1OUT x 0.885
1	0	1	0	0	1	VREG1OUT x 0.890
1	0	1	0	1	0	VREG1OUT x 0.895
1	0	1	0	1	1	VREG1OUT x 0.900
1	0	1	1	0	0	VREG1OUT x 0.905
1	0	1	1	0	1	VREG1OUT x 0.910
1	0	1	1	1	0	VREG1OUT x 0.915
1	0	1	1	1	1	VREG1OUT x 0.920
1	1	0	0	0	0	VREG1OUT x 0.925
1	1	0	0	0	1	VREG1OUT x 0.930
1	1	0	0	1	0	VREG1OUT x 0.935
1	1	0	0	1	1	VREG1OUT x 0.940
1	1	0	1	0	0	VREG1OUT x 0.945
1	1	0	1	0	1	VREG1OUT x 0.950
1	1	0	1	1	0	VREG1OUT x 0.955
1	1	0	1	1	1	VREG1OUT x 0.960
1	1	1	0	0	0	VREG1OUT x 0.965
1	1	1	0	0	1	VREG1OUT x 0.970
1	1	1	0	1	0	VREG1OUT x 0.975
1	1	1	0	1	1	VREG1OUT x 0.980
1	1	1	1	0	0	VREG1OUT x 0.985
1	1	1	1	0	1	VREG1OUT x 0.990
1	1	1	1	1	0	VREG1OUT x 0.995
1	1	1	1	1	1	VREG1OUT x 1.000

8.2.22. Frame Rate and Color Control (R2Bh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS3	FRS2	FRS1	FRS0
Default		0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

FRS[4:0] Set the frame rate when the internal resistor is used for oscillator circuit.

FRS[3:0]	FRS[3:0]	Frame Rate
0000	4'h0	30
0001	4'h1	32
0010	4'h2	34
0011	4'h3	36
0100	4'h4	38
0101	4'h5	41
0110	4'h6	44
0111	4'h7	48
1000	4'h8	52
1001	4'h9	58
1010	4'hA	64
1011	4'hB	72
1100	4'hC	83
1101	4'hD	97
1110	4'hE	Setting Prohibited
1111	4'hF	Setting Prohibited

8.2.23. Gamma Control (R30h ~ R3Dh)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R30h	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
R31h	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
R32h	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
R35h	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
R36h	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
R37h	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
R38h	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
R39h	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
R3Ch	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
R3Dh	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]

KP5-0[2:0] : γ fine adjustment register for positive polarity

RP1-0[2:0] : γ gradient adjustment register for positive polarity

VRP1-0[4:0] : γ amplitude adjustment register for positive polarity

KN5-0[2:0] : γ fine adjustment register for negative polarity

RN1-0[2:0] : γ gradient adjustment register for negative polarity

VRN1-0[4:0] : γ amplitude adjustment register for negative polarity

For details “ γ -Correction Function” section.

8.2.24. Horizontal and Vertical RAM Address Position (R50h, R51h, R52h, R53h)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R50h	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
R51h	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
R52h	W	1	0	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1
R53h	W	1	0	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1
R50h	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R51h			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R52h			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R53h			0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

HSA[7:0]/HEA[7:0] HSA[7:0] and HEA[7:0] represent the respective addresses at the start and end of the window address area in horizontal direction. By setting HSA and HEA bits, it is possible to limit the area on the GRAM horizontally for writing data. The HSA and HEA bits must be set before starting RAM write operation. In setting these bits, be sure “00”h \leq HSA[7:0] < HEA[7:0] \leq “EF”h. and “01”h \leq (HEA – HSA).

VSA[8:0]/VEA[8:0] VSA[8:0] and VEA[8:0] represent the respective addresses at the start and end of the window address area in vertical direction. By setting VSA and VEA bits, it is possible to limit the area on the GRAM vertically for writing data. The VSA and VEA bits must be set before starting RAM write operation. In setting, be sure “000”h \leq VSA[8:0] < VEA[8:0] \leq “13F”h.

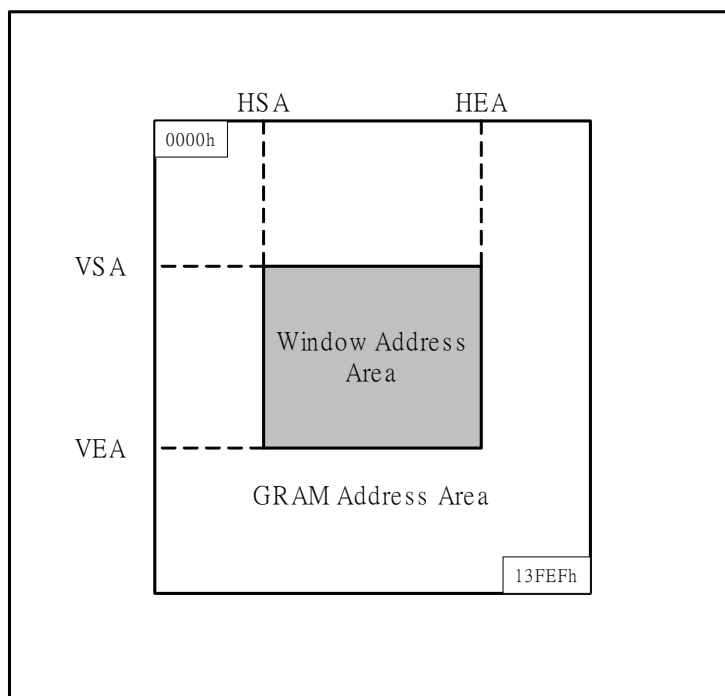


Figure 29 GRAM Access Range Configuration

$00h \leq HSA[7:0] \leq HEA[7:0] \leq EFh$

$00h \leq VSA[8:0] \leq VEA[8:0] \leq 13Fh$

Note1: The window address range must be within the GRAM address space.

Note2: Data are written to GRAM in four-words when operating in high speed mode, the dummy write operations should be inserted depending on the window address area. For details, see the High-Speed RAM Write Function section.

8.2.25. Gate Scan Control (R60h, R61h, R6Ah)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R60h	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
R61h	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
R6Ah	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
R60h	Default		0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0
R61h			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R6Ah			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCN[5:0] The ILI9325D allows to specify the gate line from which the gate driver starts to scan by setting the SCN[5:0] bits.

SCN[5:0]	Scanning Start Position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
00h	G1	G320	G1	G320
01h	G9	G312	G17	G304
02h	G17	G304	G33	G288
03h	G25	G296	G49	G272
04h	G33	G288	G65	G256
05h	G41	G280	G81	G240
06h	G49	G272	G97	G224
07h	G57	G264	G113	G208
08h	G65	G256	G129	G192
09h	G73	G248	G145	G176
0Ah	G81	G240	G161	G160
0Bh	G89	G232	G177	G144
0Ch	G97	G224	G193	G128
0Dh	G105	G216	G209	G112
0Eh	G113	G208	G225	G96
0Fh	G121	G200	G241	G80
10h	G129	G192	G257	G64
11h	G137	G184	G273	G48
12h	G145	G176	G289	G32
13h	G153	G168	G305	G16
14h	G161	G160	G2	G319
15h	G169	G152	G18	G303
16h	G177	G144	G34	G287
17h	G185	G136	G50	G271
18h	G193	G128	G66	G255
19h	G201	G120	G82	G239
1Ah	G209	G112	G98	G223
1Bh	G217	G104	G114	G207
1Ch	G225	G96	G130	G191
1Dh	G233	G88	G146	G175
1Eh	G241	G80	G162	G159
1Fh	G249	G72	G178	G143
20h	G257	G64	G194	G127
21h	G265	G56	G210	G111
22h	G273	G48	G226	G95
23h	G281	G40	G242	G79
24h	G289	G32	G258	G63
25h	G297	G24	G274	G47
26h	G305	G16	G290	G31
27h	G313	G8	G306	G15
28h ~ 3Fh	Setting disabled	Setting disabled	Setting disabled	Setting disabled

Note: When SM=1, it is a interlacing scanning. Please refer to register R01h.

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	LCD Drive Line
6'h00	8 lines
6'h01	16 lines
6'h02	24lines
...	...
6'h1D	240 lines
6'h1E	248 lines
6'h1F	256 lines
6'h20	264 lines
6'h21	272 lines
6'h22	280 lines
6'h23	288 lines
6'h24	296 lines
6'h25	304 lines
6'h26	312 line
6'h27	320 line
Others	Setting inhibited

NDL: Sets the source driver output level in the non-display area.

NDL	Non-Display Area	
	Positive Polarity	Negative Polarity
0	V63	V0
1	V0	V63

GS: Sets the direction of scan by the gate driver in the range determined by SCN[5:0] and NL[5:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

When GS = 0, the scan direction is from G1 to G320.

When GS = 1, the scan direction is from G320 to G1

REV: Enables the grayscale inversion of the image by setting REV=1.

REV	GRAM Data	Source Output in Display Area	
		Positive polarity	negative polarity
0	18'h00000	V63	V0
	.	.	.
	.	.	.
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	.	.	.
	.	.	.
	18'h3FFFF	V63	V0

VLE: Vertical scroll display enable bit. When VLE = 1, the ILI9325D starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the

number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

VLE	Base Image Display
0	Fixed
1	Enable Scrolling

VL[8:0]: Sets the scrolling amount of base image. The base image is scrolled in vertical direction and displayed from the line determined by VL[8:0]. Make sure that $VL[8:0] \leq 320$.

8.2.26. SPI Read/Write Control (R66h, Write Only)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/WX

This register is used to control the read/write function of registers when the 8/9-bit serial interface is used.

If users need to read back the register parameter by the 8/9-bit serial interface, the R/WX bit must be set as '1'.

R/WX	Description
0	Register write mode (default)
1	Register read mode

8.2.27. Partial Image 1 Display Position (R80h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTD P0[8]	PTD P0[7]	PTD P0[6]	PTD P0[5]	PTD P0[4]	PTD P0[3]	PTD P0[2]	PTD P0[1]	PTD P0[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTDP0[8:0]: Sets the display start position of partial image 1. The display areas of the partial images 1 and 2 must not overlap each another.

8.2.28. Partial Image 1 RAM Start/End Address (R81h, R82h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTS A0[8]	PTS A0[7]	PTS A0[6]	PTS A0[5]	PTS A0[4]	PTS A0[3]	PTS A0[2]	PTS A0[1]	PTS A0[0]
W	1	0	0	0	0	0	0	0	PTE A0[8]	PTE A0[7]	PTE A0[6]	PTE A0[5]	PTE A0[4]	PTE A0[3]	PTE A0[2]	PTE A0[1]	PTE A0[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTSA0[8:0] PTEA0[8:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 1. Make sure $PTSA0[8:0] \leq PTEA0[8:0]$.

8.2.29. Partial Image 2 Display Position (R83h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTD P1[8]	PTD P1[7]	PTD P1[6]	PTD P1[5]	PTD P1[4]	PTD P1[3]	PTD P1[2]	PTD P1[1]	PTD P1[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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PTDP1[8:0]: Sets the display start position of partial image 2. The display areas of the partial images 1 and 2 must not overlap each other.

8.2.30. Partial Image 2 RAM Start/End Address (R84h, R85h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTS A1[8]	PTS A1[7]	PTS A1[6]	PTS A1[5]	PTS A1[4]	PTS A1[3]	PTS A1[2]	PTS A1[1]	PTS A1[0]
W	1	0	0	0	0	0	0	0	PTE A1[8]	PTE A1[7]	PTE A1[6]	PTE A1[5]	PTE A1[4]	PTE A1[3]	PTE A1[2]	PTE A1[1]	PTE A1[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTSA1[8:0] PTEA1[8:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 2. Make sure $PTSA1[8:0] \leq PTEA1[8:0]$.

8.2.31. Panel Interface Control 1 (R90h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	DIV11	DIV10	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
Default		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

RTNI[4:0]: Sets 1H (line) clock number of internal clock operating mode. In this mode, ILI9325D display operation is synchronized with internal clock signal.

RTNI[4:0]	Clocks/Line
00000~01111	Setting Disabled
10000	16 clocks
10001	17 clocks
10010	18 clocks
10011	19 clocks
10100	20 clocks
10101	21 clocks
10110	22 clocks
10111	23 clocks

RTNI[4:0]	Clocks/Line
11000	24 clocks
11001	25 clocks
11010	26 clocks
11011	27 clocks
11100	28 clocks
11101	29 clocks
11110	30 clocks
11111	31 clocks

DIV1[1:0]: Sets the division ratio of internal clock frequency.

DIV11	DIV10	Division Ratio	Internal Operation Clock Frequency
0	0	1	$f_{osc} / 1$
0	1	2	$f_{osc} / 2$
1	0	4	$f_{osc} / 4$
1	1	8	$f_{osc} / 8$

8.2.32. Panel Interface Control 2 (R92h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	NOWI[2]	NOWI[1]	NOWI[0]	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

NOWI[2:0]: Sets the gate output non-overlap period when ILI9325D display operation is synchronized with internal clock signal.

NOWI[2:0]	Gate Non-overlap Period
000	Setting inhibited
001	1 clocks
010	2 clocks
011	3 clocks
100	4 clocks
101	5 clocks
110	6 clocks
111	Setting inhibited

Note: The gate output non-overlap period is defined by the number of frequency-divided internal clocks, the frequency of which is determined by instruction (DIVI), from the reference point.

8.2.33. Panel Interface Control 4 (R95h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

DIVE[1:0]: Sets the division ratio of DOTCLK when ILI9325D display operation is synchronized with RGB interface signals.

DIVE[1:0]	Division Ratio	18/16-bit RGB Interface	DOTCLK=5MHz	6-bit x 3 Transfers RGB Interface	DOTCLK=5MHz
00	Setting Prohibited	Setting Prohibited	-	Setting Prohibited	-
01	1/4	4 DOTCLKS	0.8 μ s	12 DOTCLKS	0.8 μ s
10	1/8	8 DOTCLKS	1.6 μ s	24 DOTCLKS	1.6 μ s
11	1/16	16 DOTCLKS	3.2 μ s	48 DOTCLKS	3.2 μ s

8.2.34. Panel Interface Control 5 (R97h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0
Default		0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

NOWE[3:0]: Sets the gate output non-overlap period when the ILI9325D display operation is synchronized with RGB interface signals.

NOWE[3:0]	Gate Non-overlap Period	NOWE[3:0]	Gate Non-overlap Period
0000	Setting inhibited	1000	8 clocks
0001	1 clocks	1001	9 clocks
0010	2 clocks	1010	10 clocks
0011	3 clocks	1011	11 clocks
0100	4 clocks	1100	12 clocks
0101	5 clocks	1101	Setting inhibited
0110	6 clocks	1110	Setting inhibited
0111	7 clocks	1111	Setting inhibited

Note: 1 clock = (number of data transfer/pixel) x DIVE (division ratio) [DOTCLK]

8.2.35. OTP ID Code Programming Control (RA0h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	OTP_ID_EN	0	0	0	OTP_ID3	OTP_ID2	OTP_ID1	OTP_ID0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OTP_ID_EN: OTP_ID code programming enable. When program OTP_ID, must set this bit. OTP_ID code can only be programmed 1 time.

OTP_ID[3:0]: The 4 bits code can be read out when read this register.

8.2.36. OTP VCM Programming Control (RA1h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	OTP_PGM_EN	0	0	0	0	0	VCM_OTP5	VCM_OTP4	VCM_OTP3	VCM_OTP2	VCM_OTP1	VCM_OTP0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OTP_PGM_EN: OTP programming enable. When program OTP, must set this bit. OTP data can be programmed 2 times.

VCM_OTP[5:0]: OTP programming data for VCOMH voltage, the voltage refer to VCM[5:0] value.

8.2.37. OTP VCM Status and Enable (RA2h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	PGM_CNT1	PGM_CNT0	VCM_D5	VCM_D4	VCM_D3	VCM_D2	VCM_D1	VCM_D0	0	0	0	0	0	0	0	VCM_EN
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PGM_CNT[1:0]: OTP programmed record. These bits are read only.

OTP_PGM_CNT[1:0]	Description
00	OTP clean
01	OTP programmed 1 time
10	OTP programmed 2 times

VCM_D[5:0]: OTP VCM data read value. These bits are read only.

VCM_EN: OTP VCM data enable.

'1': Set this bit to enable OTP VCM data to replace R29h VCM value.

'0': Default value, use R29h VCM value.

8.2.38. OTP Programming ID Key (RA5h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

KEY[15:0]: OTP Programming ID key protection. Before writing OTP programming data RA1h, it must write RA5h with 0xAA55 value first to make OTP programming successfully. If RA5h is not written with 0xAA55, OTP programming will be fail. See OTP Programming flow.

8.2.39. Write Display Brightness Value (RB1h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

This command is used to adjust the brightness value of the display.

DBV[7:0]: 8 bit, for display brightness of manual brightness setting and CABC in ILI9325D. There is a PWM output signal, LEDPWM pin, to control the LED driver IC in order to control display brightness.

8.2.40. Read Display Brightness Value (RB2h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

This command is used to return the brightness value of the display.

DBV[7:0] is reset when display is in sleep-in mode.

DBV[7:0] is '0' when bit BCTRL of "Write CTRL Display (B3h)" command is '0'.

DBV[7:0] is manual set brightness specified with "Write CTRL Display (B3h)" command when BCTRL bit is '1'.

When bit BCTRL of "Write CTRL Display (B3h)" command is '1' and C1/C0 bit of "Write Content Adaptive Brightness Control (B5h)" command are '0', DBV[7:0] output is the brightness value specified with "Write Display Brightness (B1h)" command.

8.2.41. Write CTRL Display Value (RB3h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
w	1	0	0	0	0	0	0	0	0	0	0	BCTRL	0	DD	BL	0	0

This command is used to control display brightness.

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block OFF (DBV[7:0]=00h)
1	Brightness Control Block ON (DBV[7:0] is active)

DD: Display Dimming Control. This function is only for manual brightness setting.

DD	Description
0	Display Dimming OFF
1	Display Dimming ON

BL: Backlight Control On/Off

BL	Description
0	Backlight Control OFF
1	Backlight Control ON

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1 -> 0.

When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected

8.2.42. Read CTRL Display Value (RB4h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	0	0	0	0	0	0	0	0	0	0	BCTRL	0	DD	BL	0	0

This command is used to control display brightness.

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block OFF (DBV[7:0]=00h)
1	Brightness Control Block ON (DBV[7:0] is active)

DD: Display Dimming Control. This function is only for manual brightness setting.

DD	Description
0	Display Dimming OFF
1	Display Dimming ON

BL: Backlight Control On/Off

BL	Description
0	Backlight Control OFF
1	Backlight Control ON

8.2.43. Write Content Adaptive Brightness Control Value (RB5h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C[1:0]

This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C[1:0]		Description
0	0	CABC OFF
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

8.2.44. Read Content Adaptive Brightness Control Value (RB6h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C[1:0]

This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C[1:0]		Description
0	0	CABC OFF
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

8.2.45. Write CABC Minimum Brightness (RBEh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	CMB[7:0]							

This command is used to set the minimum brightness value of the display for CABC function.

CMB[7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction. When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL=0 of "Write CTRL Display (B3h)"), CABC minimum brightness setting is ignored.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

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8.2.46. Read CABC Minimum Brightness (RBFh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	0	0	0	0	0	0	0	0								

Description

This command is used to set the minimum brightness value of the display for CABC function.

CMB[7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL=0 of "Write CTRL Display (B3h)"), CABC minimum brightness setting is ignored.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

8.2.47. CABC Control 1 (RC7h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	LEDONR	LEDONPOL	LEDPWMPOL

LEDPWMPOL: The bit is used to define polarity of LEDPWM signal.

BL	LEDPWMPOL	LEDPWM pin
0	0	0
0	1	1
1	0	Original polarity of PWM signal
1	1	Inversed polarity of PWM signal

LEDONPOL: This bit is used to control LEDON pin.

BL	LEDONPOL	LEDON pin
0	0	0
0	1	1
1	0	LEDONR
1	1	Inversed LEDONR

LEDONR: This bit is used to control LEDON pin.

LEDONR	Description
0	Low
1	High

8.2.48. CABC Control 1 (RC8h)

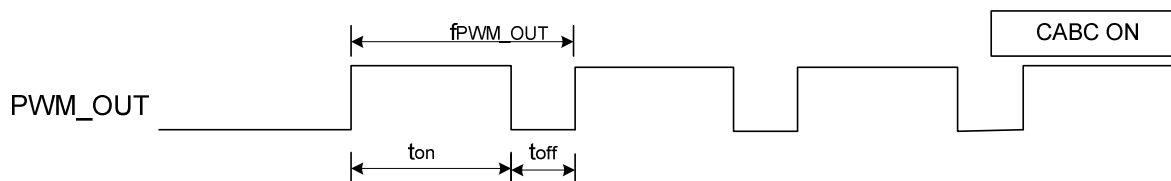
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	PWM_DIV[7:0]							

Description

PWM_DIV[7:0]: PWM_OUT output period control. This command is used to adjust the PWM waveform period of PWM_OUT. The PWM period can be calculated using the equation in the following.

$$f_{\text{PWM_OUT}} = \frac{5.8\text{MHz}}{(\text{PWM_DIV}[7:0] + 1) \times 255}$$

PWM_DIV[7:0]								f _{PWM_OUT}
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	22.74 KHz
0	0	0	0	0	0	0	1	11.37 KHz
0	0	0	0	0	0	1	0	7.58KHz
0	0	0	0	0	0	1	1	5.68 KHz
0	0	0	0	0	1	0	0	4.54 KHz
⋮								⋮
1	1	1	1	1	0	1	1	90.26 Hz
1	1	1	1	1	1	0	0	89.9Hz
1	1	1	1	1	1	0	1	89.53Hz
1	1	1	1	1	1	1	0	89.17 Hz
1	1	1	1	1	1	1	1	88.81 Hz



Note : The output frequency tolerance of internal frequency divider in CABC is $\pm 10\%$

8.2.49. CABC Control 2 (RC9h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	THRES_MOV[3:0]				THRES_STILL[3:0]			

THRES_MOV[3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63) to the total of pixels by image process in MOVING image mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

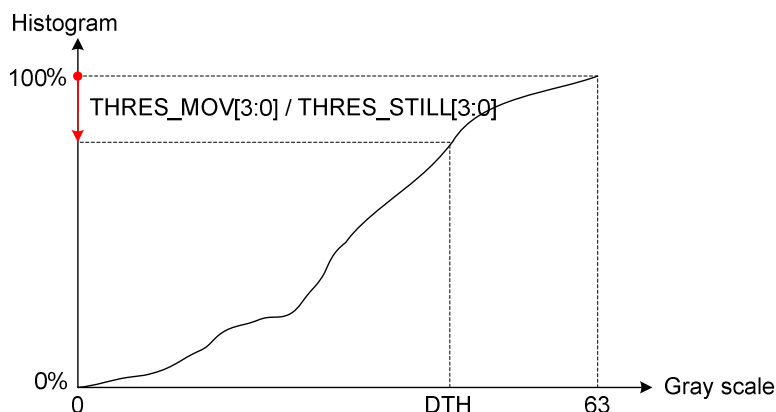
THRES_MOV[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

THRES_MOV[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %

THRES_STILL[3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63) to the total of pixels by image process in STILL mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

THRES_STILL[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

THRES_STILL[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %



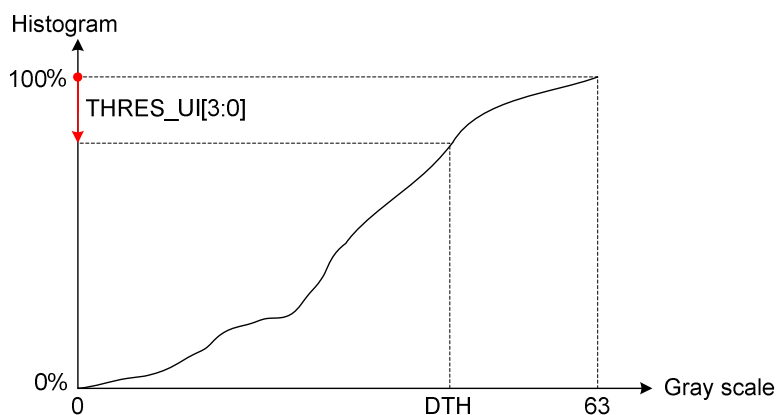
8.2.50. CABC Control 3 (RCAh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	THRES_UI[3:0]			

THRES_UI[3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63") to the total of pixels by image process in USER INTERFACE mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

THRES_UI[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

THRES_UI[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %



8.2.51. CABC Control 4 (RCBh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	DTH_MOV[3:0]				DTH_STILL[3:0]			

DTH_MOV[3:0]: This parameter is used set the minimum limitation of grayscale threshold value in MOVING image mode.

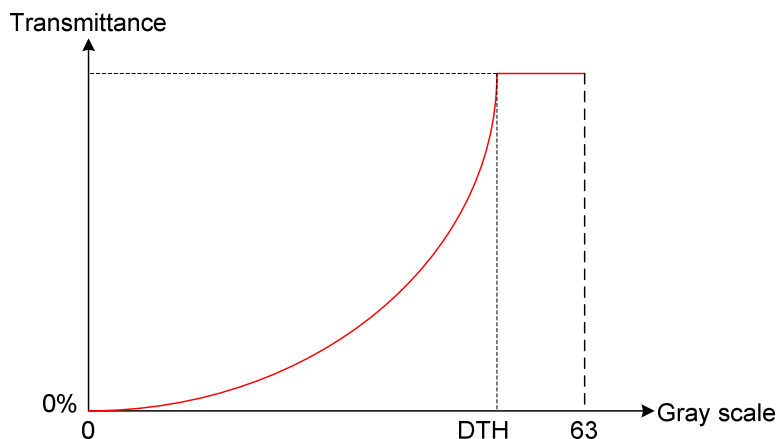
DTH_MOV[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	224
0	0	0	1	220
0	0	1	0	216
0	0	1	1	212
0	1	0	0	208
0	1	0	1	204
0	1	1	0	200
0	1	1	1	196

DTH_MOV[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	192
1	0	0	1	188
1	0	1	0	184
1	0	1	1	180
1	1	0	0	176
1	1	0	1	172
1	1	1	0	168
1	1	1	1	164

DTH_STILL[3:0]: This parameter is used to set the minimum limitation of grayscale threshold value in STILL image mode.

DTH_STILL[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	224
0	0	0	1	220
0	0	1	0	216
0	0	1	1	212
0	1	0	0	208
0	1	0	1	204
0	1	1	0	200
0	1	1	1	196

DTH_STILL[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	192
1	0	0	1	188
1	0	1	0	184
1	0	1	1	180
1	1	0	0	176
1	1	0	1	172
1	1	1	0	168
1	1	1	1	164



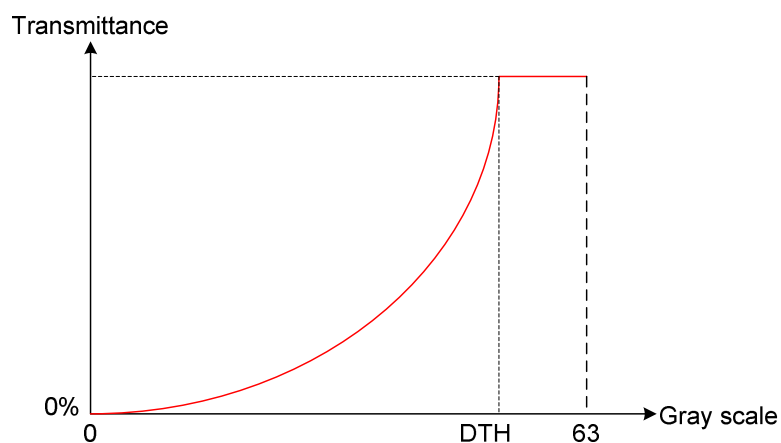
8.2.52. CABC Control 5 (RCCh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	DTH_UI[3:0]			

DTH_UI[3:0]: This parameter is used set the minimum limitation of grayscale threshold value in USER INTERFACE mode.

DTH_UI[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	252
0	0	0	1	248
0	0	1	0	244
0	0	1	1	240
0	1	0	0	236
0	1	0	1	232
0	1	1	0	228
0	1	1	1	224

DTH_UI[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	220
1	0	0	1	216
1	0	1	0	212
1	0	1	1	208
1	1	0	0	204
1	1	0	1	200
1	1	1	0	196
1	1	1	1	192



8.2.53. CABC Control 6 (RCDh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	DIM_OPT2[3:0]				0	DIM_OPT1[2:0]		

DIM_OPT1[2:0]: This parameter is used set the transition time of brightness level change to avoid the sharp brightness change on vision.

DIM_OPT1[2:0]			Description
D2	D1	D0	
0	0	0	1 frame
0	0	1	1 frame
0	1	0	2 frames
0	1	1	4 frames
1	0	0	8 frames
1	0	1	16 frames
1	1	0	32 frames
1	1	1	64 frames

DIM_OPT2[3:0]: This parameter is used to set the imitation of minimum brightness change. If this parameter is large than the difference between target brightness and current brightness, then the brightness will not change.

8.2.54. Digital Gamma Control 1 (RDDh, Write Only)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	RCS0	RCA0[2:0]		BCS0	BCA0[2:0]			
W	1	0	0	0	0	0	0	0	0	RCS1	RCA1[2:0]		BCS1	BCA1[2:0]			
...		...															
W	1	0	0	0	0	0	0	0	0	RCSx	RCAx[2:0]		BCSx	BCAx[2:0]			
...		...															
W	1	0	0	0	0	0	0	0	0	RCS14	RCA14[2:0]		BCS14	BCA14[2:0]			
W	1	0	0	0	0	0	0	0	0	RCS15	RCA15[2:0]		BCS15	BCA15[2:0]			

RCSx: The sign flag bit select RCA value as positive compensation or negative compensation for red display pixel. When RCSx = 0/1, positive compensation / negative compensation is selected.

RCAx[2:0]: Gamma Macro-adjustment registers for red gamma curve.

BCSx: The sign flag bit select BCA value as positive compensation or negative compensation for red display pixel. When RCSx = 0/1, positive compensation / negative compensation is selected.

BCAx[2:0]: Gamma Macro-adjustment registers for blue gamma curve.

Note 1: The RDDh and RDEh register tables must be completed entirely for implementing digital Gamma adjustment. Otherwise, the function does not work.

Note 2: It is invalid to control red (blue) gamma adjustment in 8-color display mode.

8.2.55. Digital Gamma Control 2 (RDEh, Write Only)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	RFA0[3:0]				BFA0[3:0]			
W	1	0	0	0	0	0	0	0	0	RFA1[3:0]				BFA1[3:0]			
...																	
W	1	0	0	0	0	0	0	0	0	RFAx[3:0]				BFAx[3:0]			
...																	
W	1	0	0	0	0	0	0	0	0	RFA62[3:0]				BFA62[3:0]			
W	1	0	0	0	0	0	0	0	0	RFA63[3:0]				BFA63[3:0]			

RFA[3:0]: Gamma Macro-adjustment registers for red gamma curve.

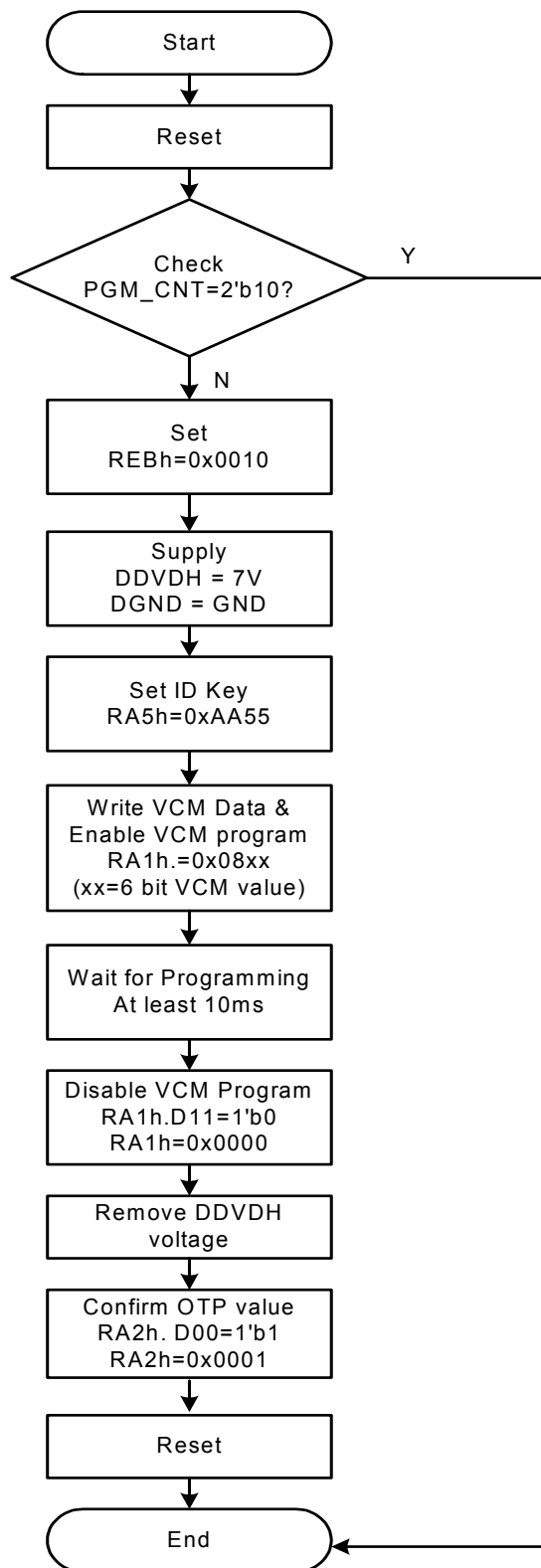
BFA[3:0]: Gamma Macro-adjustment registers for blue gamma curve.

Note 1: The RDDh and RDEh register tables must be completed entirely for implementing digital Gamma adjustment. Otherwise, the function does not work.

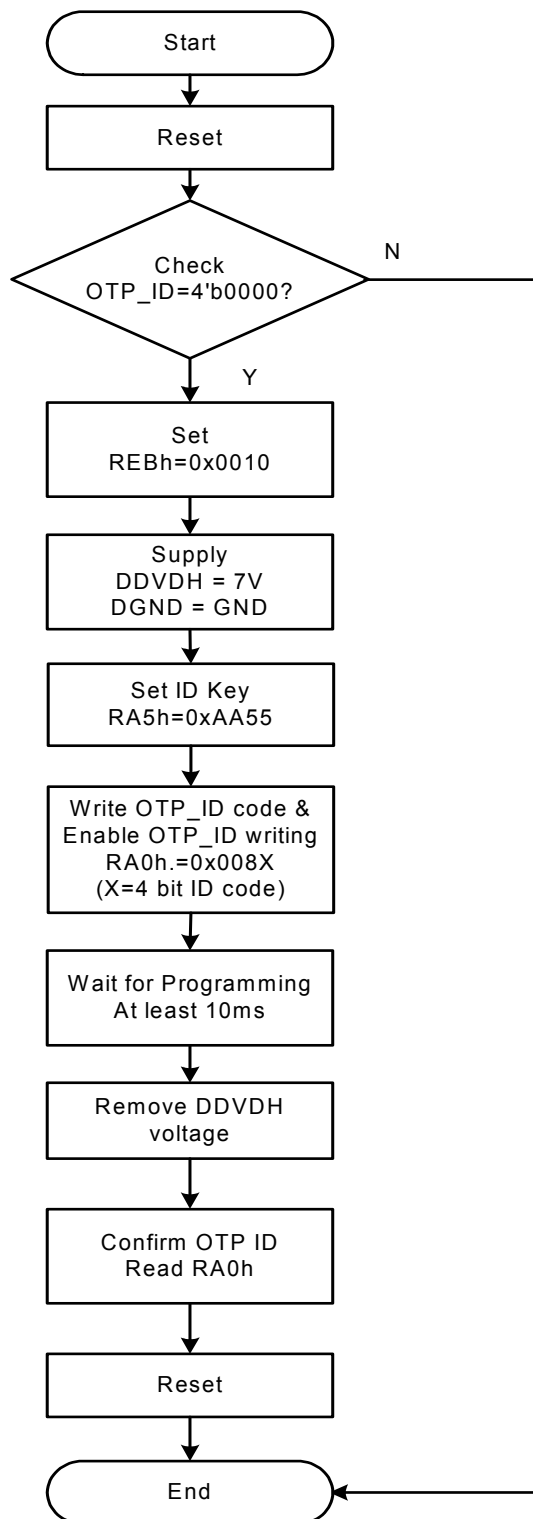
Note 2: It is invalid to control red (blue) gamma adjustment in 8-color display mode.

9. OTP Programming Flow

VCOMH OTP programming Flow



OTP ID Writing Flow



10. GRAM Address Map & Read/Write

ILI9325D has an internal graphics RAM (GRAM) of 172,800 bytes to store the display data and one pixel is constructed of 18 bits. The GRAM can be accessed through the i80 system, SPI and RGB interfaces.

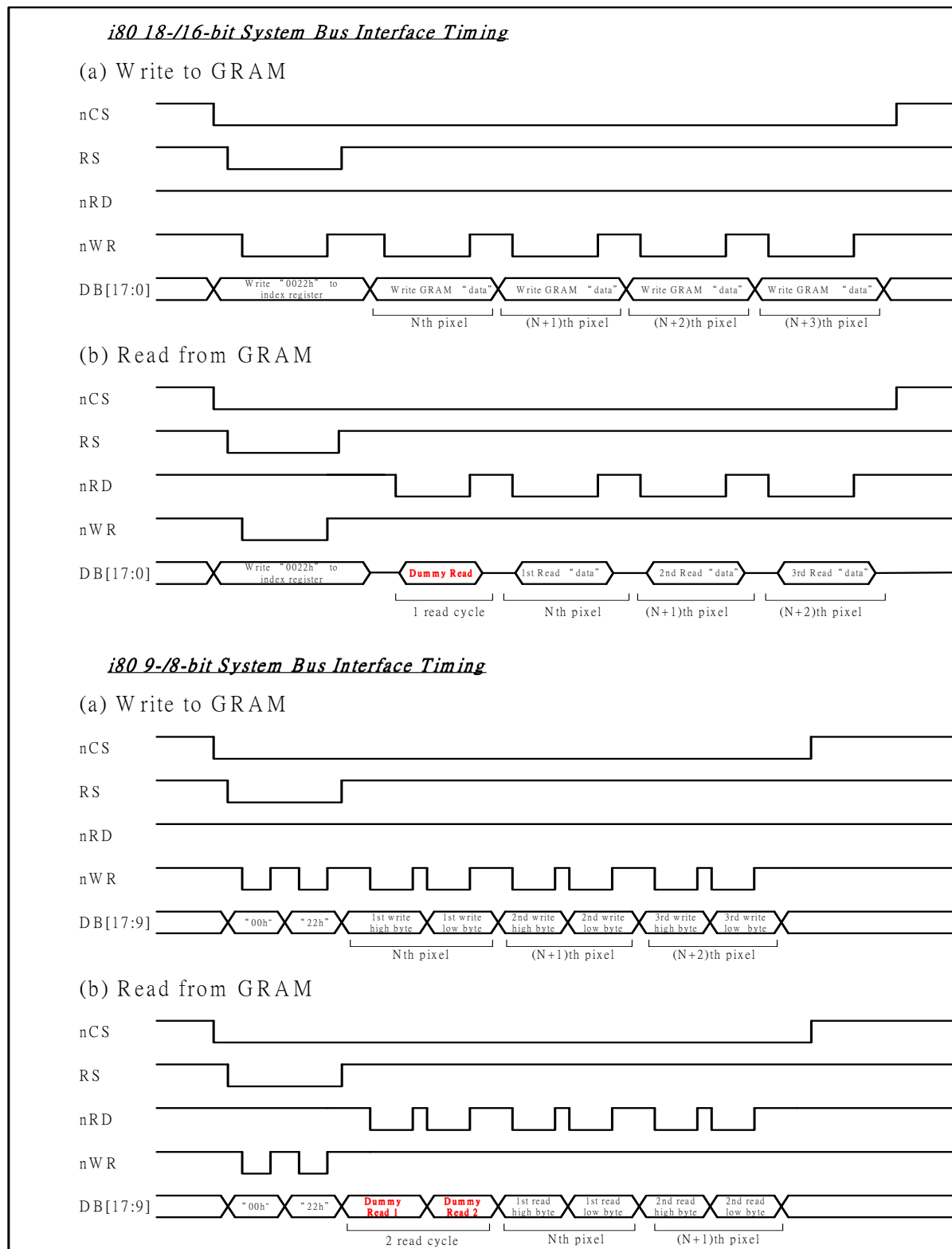
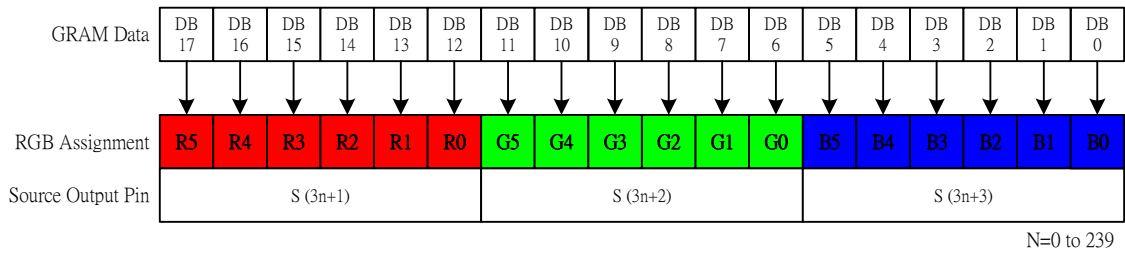


Figure 30 GRAM Read/Write Timing of i80-System Interface

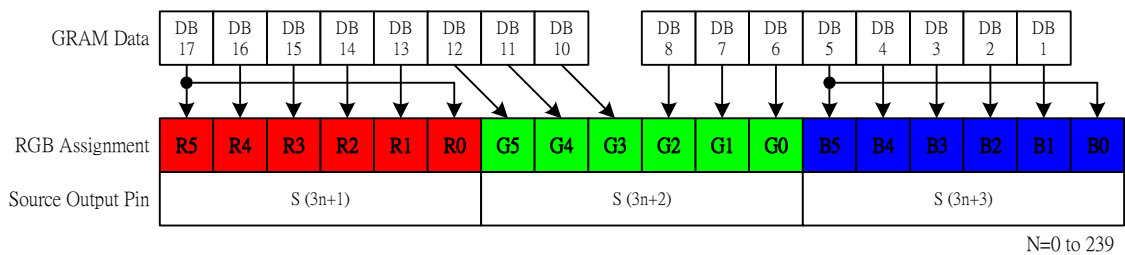
GRAM address map table of SS=0, BGR=0

SS=0, BGR=0	S1...S3	S4...S6	S7...S9	S10...S12	...	S517...S519	S520...S522	S523...S525	S526...S720
GS=0	GS=1	DB17...0	DB17...0	DB17...0	DB17...0	...	DB17...0	DB17...0	DB17...0
G1	G320	"00000h"	"00001h"	"00002h"	"00003h"	...	"000ECh"	"000EDh"	"000EEh"
G2	G319	"00100h"	"00101h"	"00102h"	"00103h"	...	"001ECh"	"001EDh"	"001EEh"
G3	G318	"00200h"	"00201h"	"00202h"	"00203h"	...	"002ECh"	"002EDh"	"002EEh"
G4	G317	"00300h"	"00301h"	"00302h"	"00303h"	...	"003ECh"	"003EDh"	"003EEh"
G5	G316	"00400h"	"00401h"	"00402h"	"00403h"	...	"004ECh"	"004EDh"	"004EEh"
G6	G315	"00500h"	"00501h"	"00502h"	"00503h"	...	"005ECh"	"005EDh"	"005EEh"
G7	G314	"00600h"	"00601h"	"00602h"	"00603h"	...	"006ECh"	"006EDh"	"006EEh"
G8	G313	"00700h"	"00701h"	"00702h"	"00703h"	...	"007ECh"	"007EDh"	"007EEh"
G9	G312	"00800h"	"00801h"	"00802h"	"00803h"	...	"008ECh"	"008EDh"	"008EEh"
G10	G311	"00900h"	"00901h"	"00902h"	"00903h"	...	"009ECh"	"009EDh"	"009EEh"
.
.
.
G311	G10	"13600h"	"13601h"	"13602h"	"13603h"	...	"136ECh"	"136EDh"	"136EEh"
G312	G9	"13700h"	"13701h"	"13702h"	"13703h"	...	"137ECh"	"137EDh"	"137EEh"
G313	G8	"13800h"	"13801h"	"13802h"	"13803h"	...	"138ECh"	"138EDh"	"138EEh"
G314	G7	"13900h"	"13901h"	"13902h"	"13903h"	...	"139ECh"	"139EDh"	"139EEh"
G315	G6	"13A00h"	"13A01h"	"13A02h"	"13A03h"	...	"13AECh"	"13AEDh"	"13AEEh"
G316	G5	"13B00h"	"13B01h"	"13B02h"	"13B03h"	...	"13BECh"	"13BEDh"	"13BEEh"
G317	G4	"13C00h"	"13C01h"	"13C02h"	"13C03h"	...	"13CECh"	"13CEDh"	"13CEEh"
G318	G3	"13D00h"	"13D01h"	"13D02h"	"13D03h"	...	"13DECh"	"13DEDh"	"13DEEh"
G319	G2	"13E00h"	"13E01h"	"13E02h"	"13E03h"	...	"13EECh"	"13EEDh"	"13EEEh"
G320	G1	"13F00h"	"13F01h"	"13F02h"	"13F03h"	...	"13FECh"	"13FEDh"	"13FEEh"

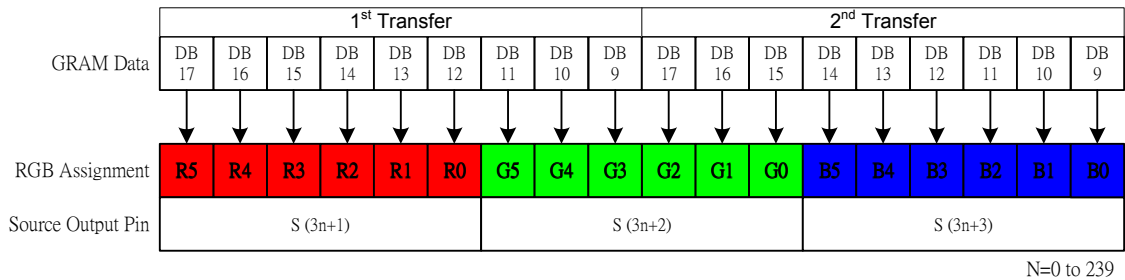
i80 system 18-bit data bus interface



i80 system 16-bit data bus interface



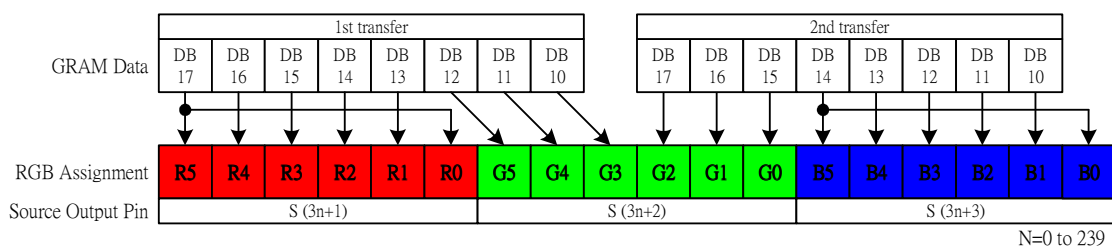
i80 system 9-bit data bus interface



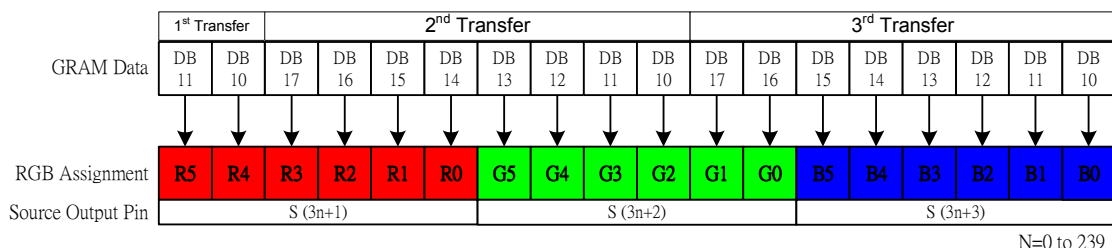
GRAM Data and display data of 18-/16-/9-bit system interface (SS=" 0", BGR=" 0")

Figure 31 i80-System Interface with 18-/16-/9-bit Data Bus (SS="0", BGR="0")

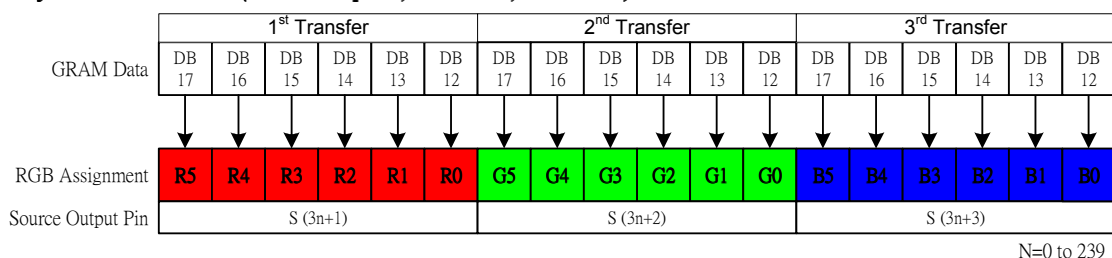
i80 system 8-bit interface (2 transfers/pixel)



i80 system 8-bit interface (3 transfers/pixel, TRI=" 1", DFM=" 0")



i80 system 8-bit interface (3 transfers/pixel, TRI=" 1", DFM=" 1")



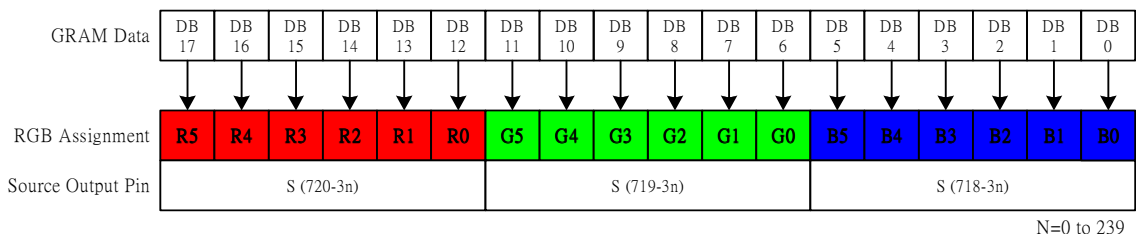
i80 system 8-bit interface (SS=" 0", BGR=" 0")

Figure 32 i80-System Interface with 8-bit Data Bus (SS="0", BGR="0")

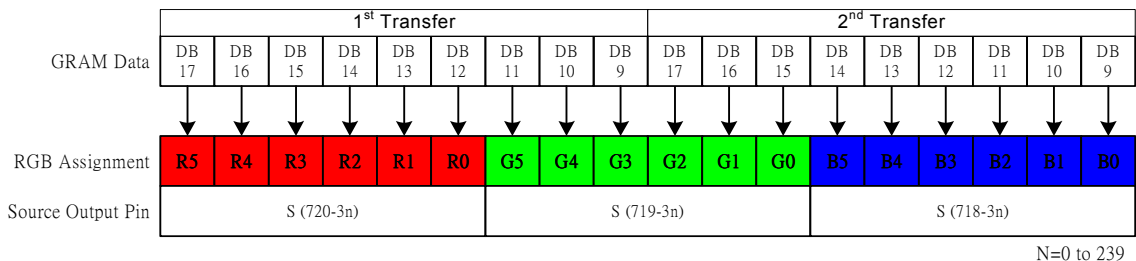
GRAM address map table of SS=1, BGR=1

SS=1, BGR=1	S720...S718	S717...S715	S714...S712	S711...S709	...	S12...S10	S9...S7	S6...S4	S3...S1
GS=0	GS=1	DB17...0	DB17...0	DB17...0	DB17...0	...	DB17...0	DB17...0	DB17...0
G1	G320	"00000h"	"00001h"	"00002h"	"00003h"	...	"000ECh"	"000EDh"	"000EEh"
G2	G319	"00100h"	"00101h"	"00102h"	"00103h"	...	"001ECh"	"001EDh"	"001EEh"
G3	G318	"00200h"	"00201h"	"00202h"	"00203h"	...	"002ECh"	"002EDh"	"002EEh"
G4	G317	"00300h"	"00301h"	"00302h"	"00303h"	...	"003ECh"	"003EDh"	"003EEh"
G5	G316	"00400h"	"00401h"	"00402h"	"00403h"	...	"004ECh"	"004EDh"	"004EEh"
G6	G315	"00500h"	"00501h"	"00502h"	"00503h"	...	"005ECh"	"005EDh"	"005EEh"
G7	G314	"00600h"	"00601h"	"00602h"	"00603h"	...	"006ECh"	"006EDh"	"006EEh"
G8	G313	"00700h"	"00701h"	"00702h"	"00703h"	...	"007ECh"	"007EDh"	"007EEh"
G9	G312	"00800h"	"00801h"	"00802h"	"00803h"	...	"008ECh"	"008EDh"	"008EEh"
G10	G311	"00900h"	"00901h"	"00902h"	"00903h"	...	"009ECh"	"009EDh"	"009EEh"
.
.
.
G311	G10	"13600h"	"13601h"	"13602h"	"13603h"	...	"136ECh"	"136EDh"	"136EEh"
G312	G9	"13700h"	"13701h"	"13702h"	"13703h"	...	"137ECh"	"137EDh"	"137EEh"
G313	G8	"13800h"	"13801h"	"13802h"	"13803h"	...	"138ECh"	"138EDh"	"138EEh"
G314	G7	"13900h"	"13901h"	"13902h"	"13903h"	...	"139ECh"	"139EDh"	"139EEh"
G315	G6	"13A00h"	"13A01h"	"13A02h"	"13A03h"	...	"13AECh"	"13AEDh"	"13AEEh"
G316	G5	"13B00h"	"13B01h"	"13B02h"	"13B03h"	...	"13BECh"	"13BEDh"	"13BEEh"
G317	G4	"13C00h"	"13C01h"	"13C02h"	"13C03h"	...	"13CECh"	"13CEDh"	"13CEEh"
G318	G3	"13D00h"	"13D01h"	"13D02h"	"13D03h"	...	"13DECh"	"13DEDh"	"13DEEh"
G319	G2	"13E00h"	"13E01h"	"13E02h"	"13E03h"	...	"13EECh"	"13EEDh"	"13EEEh"
G320	G1	"13F00h"	"13F01h"	"13F02h"	"13F03h"	...	"13FECh"	"13FEDh"	"13FEEh"

i80 system 18-bit data bus interface



i80 system 9-bit data bus interface



GRAM Data and display data of 18-/9-bit system interface (SS="1", BGR="1")

Figure 33 i80-System Interface with 18-/9-bit Data Bus (SS="1", BGR="1")

11. Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal RAM. The window address area is made by setting the horizontal address register (start: HSA[7:0], end: HEA[7:0] bits) and the vertical address register (start: VSA[8:0], end: VEA[8:0] bits). The AM bit sets the transition direction of RAM address (either increment or decrement). These bits enable the ILI9325D to write data including image data consecutively not taking data wrap positions into account.

The window address area must be made within the GRAM address map area. Also, the GRAM address bits (RAM address set register) must be an address within the window address area.

[Window address setting area]

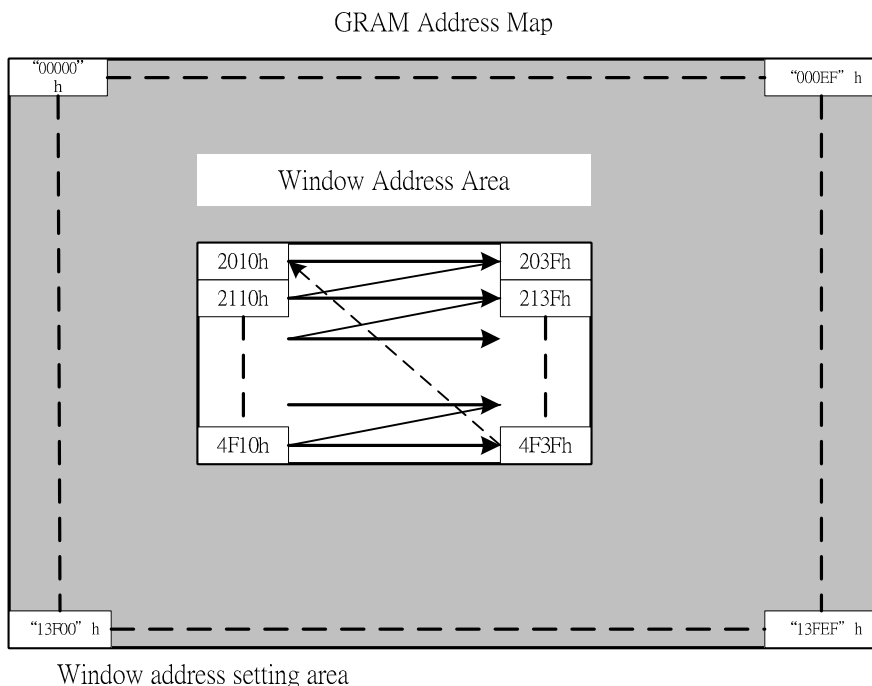
(Horizontal direction) $00H \leq HSA[7:0] \leq HEA[7:0] \leq "EF"H$

(Vertical direction) $00H \leq VSA[8:0] \leq VEA[8:0] \leq "13F"H$

[RAM address, AD (an address within a window address area)]

(RAM address) $HSA[7:0] \leq AD[7:0] \leq HEA[7:0]$

$VSA[8:0] \leq AD[15:8] \leq VEA[8:0]$



HSA[7:0] = 10h, HEA[7:0] = 3Fh, I/D = 1 (increment)
VSA[8:0] = 20h, VEA[8:0] = 4Fh, AM = 0 (horizontal writing)

Figure 34 GRAM Access Window Map

12. Gamma Correction

ILI9325D incorporates the γ -correction function to display 262,144 colors for the LCD panel. The γ -correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make ILI9325D available with liquid crystal panels of various characteristics.

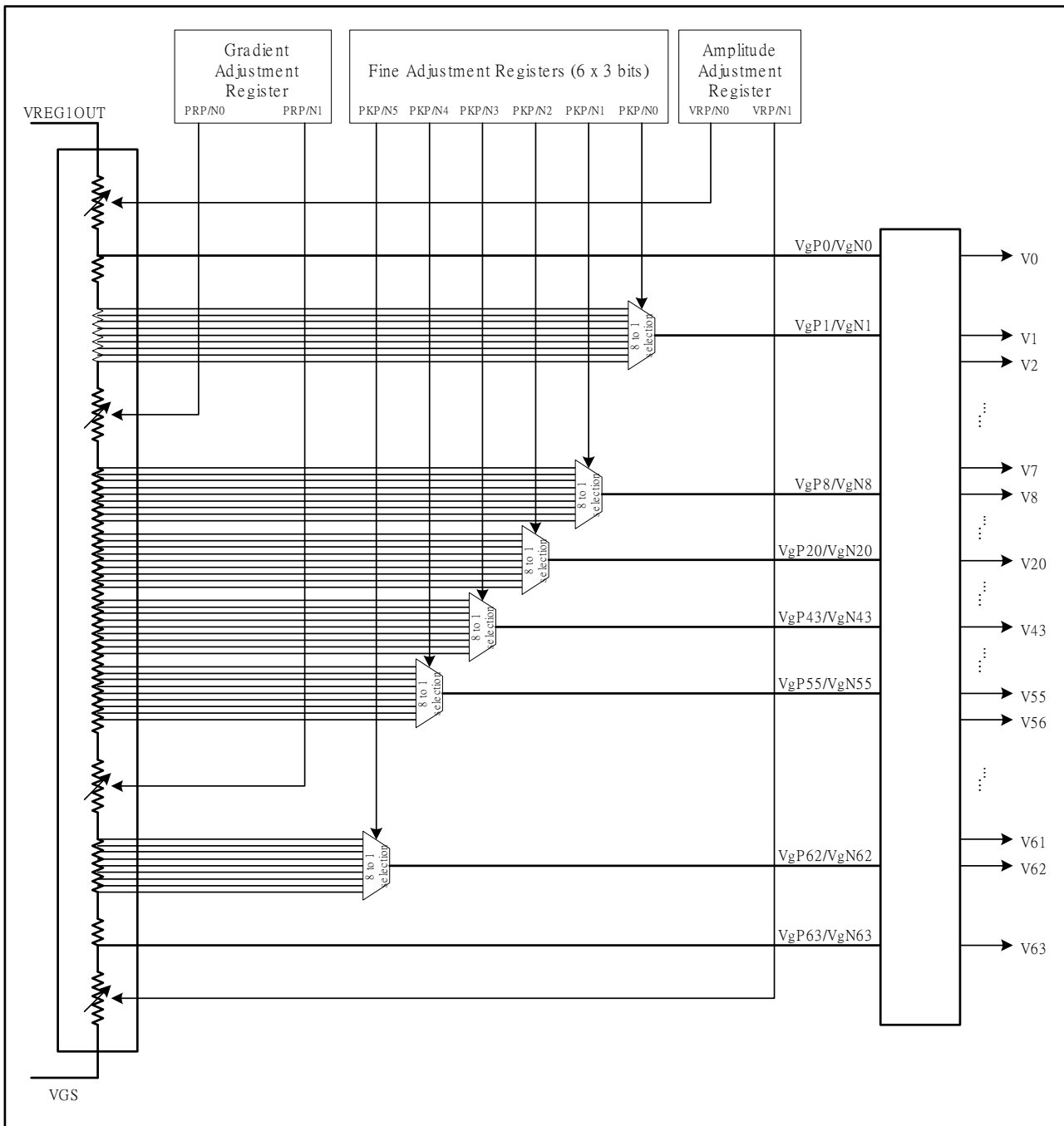


Figure 35 Grayscale Voltage Generation

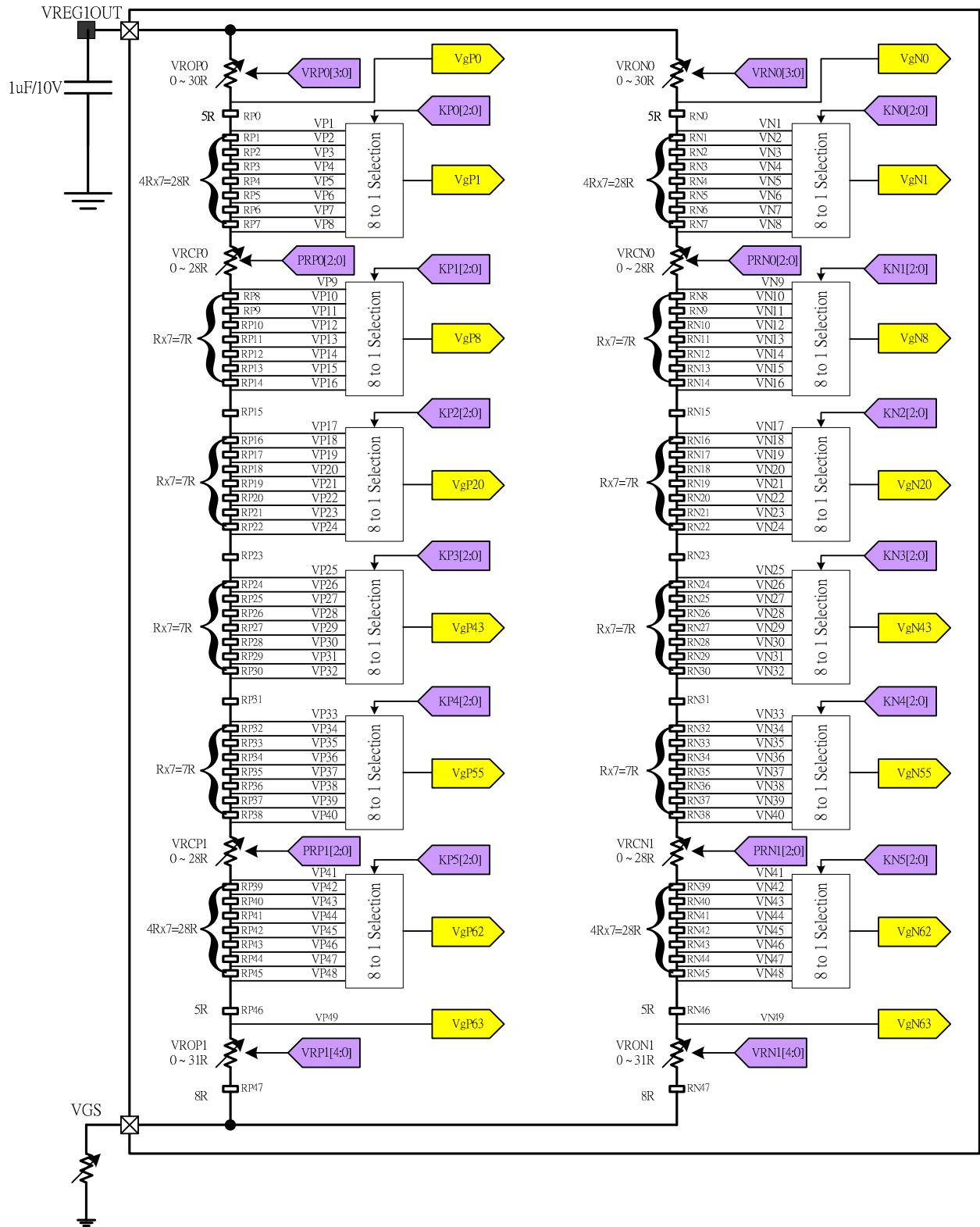


Figure 36 Grayscale Voltage Adjustment

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale reference voltage level. To adjust the gradient, the resistance values of variable resistors in the middle of the ladder resistor are adjusted by registers PRP0[2:0]/PRN0[2:0], PRP1[2:0]/PRN1[2:0]. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers, VRP0[3:0]/VRN0[3:0], VRP1[4:0]/VRN1[4:0], are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of variable resistors at the top and bottom of the ladder resistor are adjusted. Same as the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

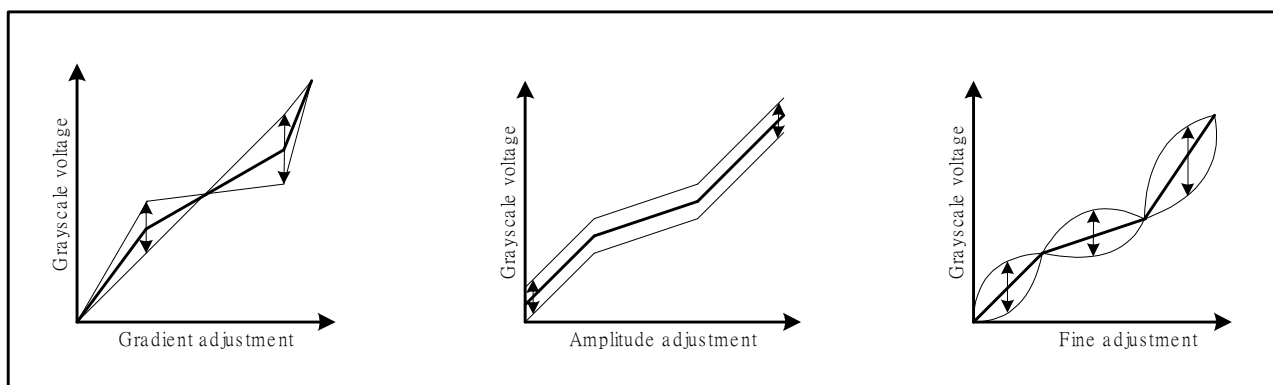


Figure 37 Gamma Curve Adjustment

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0 [2:0]	PRN0 [2:0]	Variable resistor VRCP0, VRCN0
	PRP1 [2:0]	PRN1 [2:0]	Variable resistor VRCP1, VRCN1
Amplitude adjustment	VRP0 [3:0]	VRN0 [3:0]	Variable resistor VROP0, VRON0
	VRP1 [4:0]	VRN1 [4:0]	Variable resistor VROP1, VRON1
Fine adjustment	KP0 [2:0]	KN0 [2:0]	8-to-1 selector (voltage level of grayscale 1)
	KP1 [2:0]	KN1 [2:0]	8-to-1 selector (voltage level of grayscale 8)
	KP2 [2:0]	KN2 [2:0]	8-to-1 selector (voltage level of grayscale 20)
	KP3 [2:0]	KN3 [2:0]	8-to-1 selector (voltage level of grayscale 43)
	KP4 [2:0]	KN4 [2:0]	8-to-1 selector (voltage level of grayscale 55)
	KP5 [2:0]	KN5 [2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder resistors and 8-to-1 selector Block configuration

The reference voltage generating block consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ -correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

Variable resistors

ILI9325D uses variable resistors of the following three purposes: gradient adjustment (VRCP(N)0/VRCP(N)1); amplitude adjustment (1) (VROP(N)0); and the amplitude adjustment (2) (VROP(N)1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Gradient adjustment	
PRP(N)0/1[2:0] Register	VRCP(N)0/1 Resistance
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Amplitude adjustment (1)	
VRP(N)0[3:0] Register	VROP(N)0 Resistance
0000	0R
0001	2R
0010	4R
:	:
:	:
1101	26R
1111	28R
1111	30R

Amplitude adjustment (2)	
VRP(N)1[4:0] Register	VROP(N)1 Resistance
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

8-to-1 selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register and output the selected voltage level as a reference grayscale voltage (VgP(N)1~6).

The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

Fine adjustment registers and selected voltage						
Register	Selected Voltage					
KP(N)[2:0]	VgP(N)1	VgP(N)8	VgP(N)20	VgP(N)43	VgP(N)55	VgP(N)62
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Fine adjustment registers and selected resistor						
Register	Selected Resistor					
KP(N)[2:0]	RMP(N)0	RMP(N)1	RMP(N)2	RMP(N)3	RMP(N)4	RMP(N)5
000	0R	0R	0R	0R	0R	0R
001	4R	1R	1R	1R	1R	4R
010	8R	2R	2R	2R	2R	8R
011	12R	3R	3R	3R	3R	12R
100	16R	4R	4R	4R	4R	16R
101	20R	5R	5R	5R	5R	20R
110	24R	6R	6R	6R	6R	24R
111	28R	7R	7R	7R	7R	28R

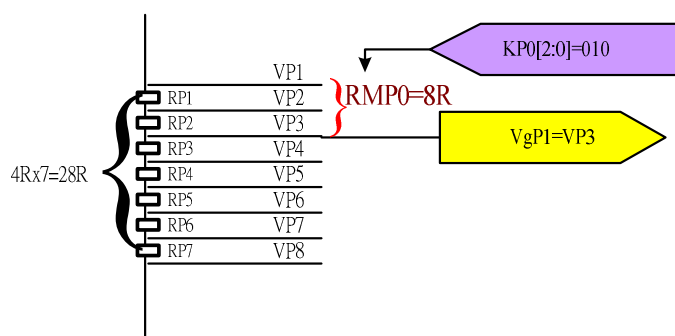


Figure 38 Example of RMP(N)0~5 definition

Gamma correction resistor ratio

Data	Positive polarity output voltage		Negative polarity output voltage	
00h	VP0	(VgP0)	VN0	(VgN0)
01h	VP1	(VgP1)	VN1	(VgN1)
02h	VP2	$(VP8+(VP1-VP8)*(30/48))$	VN2	$(VN8+(VN1-VN8)*(30/48))$
03h	VP3	$(VP8+(VP1-VP8)*(23/48))$	VN3	$(VN8+(VN1-VN8)*(23/48))$
04h	VP4	$(VP8+(VP1-VP8)*(16/48))$	VN4	$(VN8+(VN1-VN8)*(16/48))$
05h	VP5	$(VP8+(VP1-VP8)*(12/48))$	VN5	$(VN8+(VN1-VN8)*(12/48))$
06h	VP6	$(VP8+(VP1-VP8)*(8/48))$	VN6	$(VN8+(VN1-VN8)*(8/48))$
07h	VP7	$(VP8+(VP1-VP8)*(4/48))$	VN7	$(VN8+(VN1-VN8)*(4/48))$
08h	VP8	(VgP8)	VN8	(VgN8)
09h	VP9	$VP20+(VP8-VP20)*(22/24)$	VN9	$VN20+(VN8-VN20)*(22/24)$
0Ah	VP10	$VP20+(VP8-VP20)*(20/24)$	VN10	$VN20+(VN8-VN20)*(20/24)$
0Bh	VP11	$VP20+(VP8-VP20)*(18/24)$	VN11	$VN20+(VN8-VN20)*(18/24)$
0Ch	VP12	$VP20+(VP8-VP20)*(16/24)$	VN12	$VN20+(VN8-VN20)*(16/24)$
0Dh	VP13	$VP20+(VP8-VP20)*(14/24)$	VN13	$VN20+(VN8-VN20)*(14/24)$
0Eh	VP14	$VP20+(VP8-VP20)*(12/24)$	VN14	$VN20+(VN8-VN20)*(12/24)$
0Fh	VP15	$VP20+(VP8-VP20)*(10/24)$	VN15	$VN20+(VN8-VN20)*(10/24)$
10h	VP16	$VP20+(VP8-VP20)*(8/24)$	VN16	$VN20+(VN8-VN20)*(8/24)$
11h	VP17	$VP20+(VP8-VP20)*(6/24)$	VN17	$VN20+(VN8-VN20)*(6/24)$
12h	VP18	$VP20+(VP8-VP20)*(4/24)$	VN18	$VN20+(VN8-VN20)*(4/24)$
13h	VP19	$VP20+(VP8-VP20)*(2/24)$	VN19	$VN20+(VN8-VN20)*(2/24)$
14h	VP20	(VgP20)	VN20	(VgN20)
15h	VP21	$(VP43+(VP20-VP43)*(22/23))$	VN21	$(VN43+(VN20-VN43)*(22/23))$
16h	VP22	$(VP43+(VP20-VP43)*(21/23))$	VN22	$(VN43+(VN20-VN43)*(21/23))$
17h	VP23	$(VP43+(VP20-VP43)*(20/23))$	VN23	$(VN43+(VN20-VN43)*(20/23))$
18h	VP24	$(VP43+(VP20-VP43)*(19/23))$	VN24	$(VN43+(VN20-VN43)*(19/23))$
19h	VP25	$(VP43+(VP20-VP43)*(18/23))$	VN25	$(VN43+(VN20-VN43)*(18/23))$
1Ah	VP26	$(VP43+(VP20-VP43)*(17/23))$	VN26	$(VN43+(VN20-VN43)*(17/23))$
1Bh	VP27	$(VP43+(VP20-VP43)*(16/23))$	VN27	$(VN43+(VN20-VN43)*(16/23))$
1Ch	VP28	$(VP43+(VP20-VP43)*(15/23))$	VN28	$(VN43+(VN20-VN43)*(15/23))$
1Dh	VP29	$(VP43+(VP20-VP43)*(14/23))$	VN29	$(VN43+(VN20-VN43)*(14/23))$
1Eh	VP30	$(VP43+(VP20-VP43)*(13/23))$	VN30	$(VN43+(VN20-VN43)*(13/23))$
1Fh	VP31	$(VP43+(VP20-VP43)*(12/23))$	VN31	$(VN43+(VN20-VN43)*(12/23))$

Data	Positive polarity output voltage		Negative polarity output voltage	
20h	VP32	$(VP43+(VP20-VP43)*(11/23))$	VN32	$(VN43+(VN20-VN43)*(11/23))$
21h	VP33	$(VP43+(VP20-VP43)*(10/23))$	VN33	$(VN43+(VN20-VN43)*(10/23))$
22h	VP34	$(VP43+(VP20-VP43)*(9/23))$	VN34	$(VN43+(VN20-VN43)*(9/23))$
23h	VP35	$(VP43+(VP20-VP43)*(8/23))$	VN35	$(VN43+(VN20-VN43)*(8/23))$
24h	VP36	$(VP43+(VP20-VP43)*(7/23))$	VN36	$(VN43+(VN20-VN43)*(7/23))$
25h	VP37	$(VP43+(VP20-VP43)*(6/23))$	VN37	$(VN43+(VN20-VN43)*(6/23))$
26h	VP38	$(VP43+(VP20-VP43)*(5/23))$	VN38	$(VN43+(VN20-VN43)*(5/23))$
27h	VP39	$(VP43+(VP20-VP43)*(4/23))$	VN39	$(VN43+(VN20-VN43)*(4/23))$
28h	VP40	$(VP43+(VP20-VP43)*(3/23))$	VN40	$(VN43+(VN20-VN43)*(3/23))$
29h	VP41	$(VP43+(VP20-VP43)*(2/23))$	VN41	$(VN43+(VN20-VN43)*(2/23))$
2Ah	VP42	$(VP43+(VP20-VP43)*(1/23))$	VN42	$(VN43+(VN20-VN43)*(1/23))$
2Bh	VP43	(VgP43)	VN43	(VgN43)
2Ch	VP44	$(VP55+(VP43-VP55)*(22/24))$	VN44	$(VN55+(VN43-VN55)*(22/24))$
2Dh	VP45	$(VP55+(VP43-VP55)*(20/24))$	VN45	$(VN55+(VN43-VN55)*(20/24))$
2Eh	VP46	$(VP55+(VP43-VP55)*(18/24))$	VN46	$(VN55+(VN43-VN55)*(18/24))$
2Fh	VP47	$(VP55+(VP43-VP55)*(16/24))$	VN47	$(VN55+(VN43-VN55)*(16/24))$
30h	VP48	$(VP55+(VP43-VP55)*(14/24))$	VN48	$(VN55+(VN43-VN55)*(14/24))$
31h	VP49	$(VP55+(VP43-VP55)*(12/24))$	VN49	$(VN55+(VN43-VN55)*(12/24))$
32h	VP50	$(VP55+(VP43-VP55)*(10/24))$	VN50	$(VN55+(VN43-VN55)*(10/24))$
33h	VP51	$(VP55+(VP43-VP55)*(8/24))$	VN51	$(VN55+(VN43-VN55)*(8/24))$
34h	VP52	$(VP55+(VP43-VP55)*(6/24))$	VN52	$(VN55+(VN43-VN55)*(6/24))$
35h	VP53	$(VP55+(VP43-VP55)*(4/24))$	VN53	$(VN55+(VN43-VN55)*(4/24))$
36h	VP54	$(VP55+(VP43-VP55)*(2/24))$	VN54	$(VN55+(VN43-VN55)*(2/24))$
37h	VP55	(VgP55)	VN55	(VgN55)
38h	VP56	$(VP62+(VP55-VP62)*(44/48))$	VN56	$(VN62+(VN55-VN62)*(44/48))$
39h	VP57	$(VP62+(VP55-VP62)*(40/48))$	VN57	$(VN62+(VN55-VN62)*(40/48))$
3Ah	VP58	$(VP62+(VP55-VP62)*(36/48))$	VN58	$(VN62+(VN55-VN62)*(36/48))$
3Bh	VP59	$(VP62+(VP55-VP62)*(32/48))$	VN59	$(VN62+(VN55-VN62)*(32/48))$
3Ch	VP60	$(VP62+(VP55-VP62)*(25/48))$	VN60	$(VN62+(VN55-VN62)*(25/48))$
3Dh	VP61	$(VP62+(VP55-VP62)*(18/48))$	VN61	$(VN62+(VN55-VN62)*(18/48))$
3Eh	VP62	(VgP62)	VN62	(VgN62)
3Fh	VP63	(VgP63)	VN63	(VgN63)

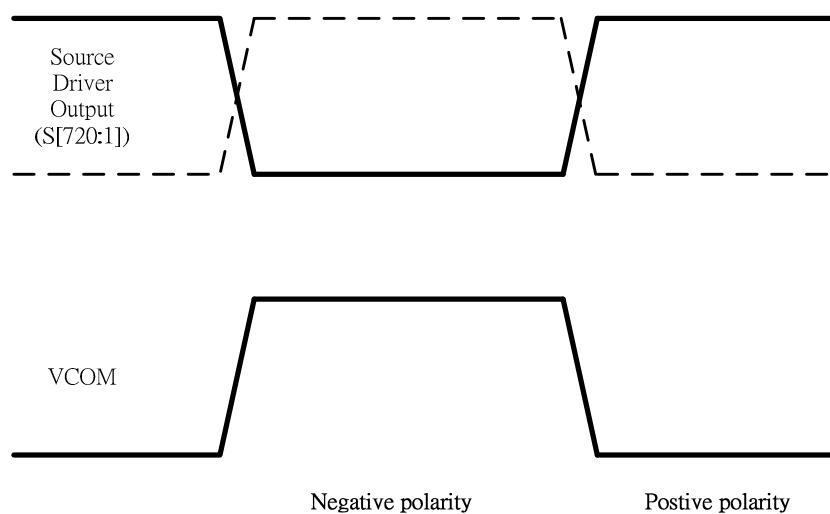


Figure 39 Relationship between Source Output and VCOM

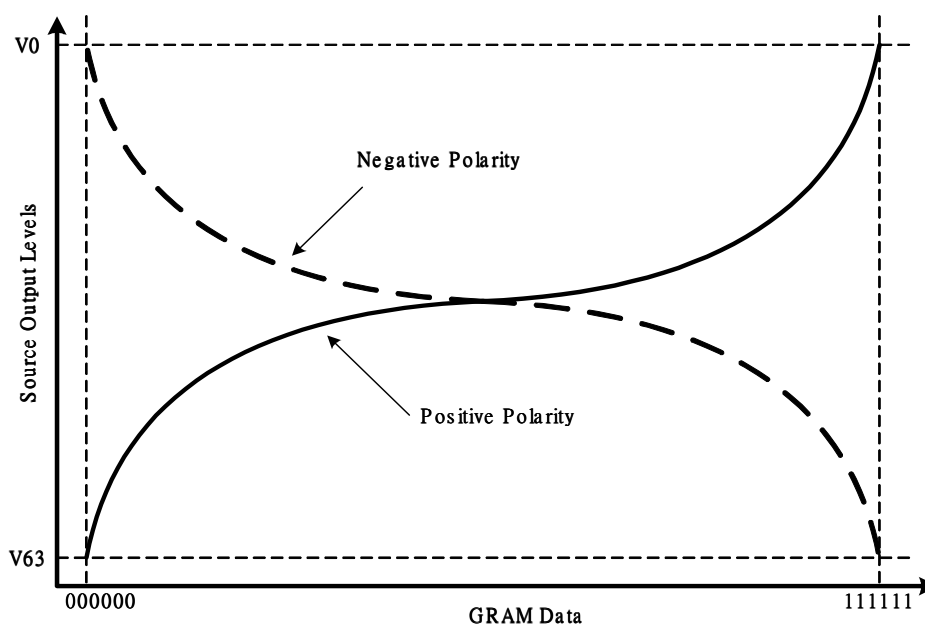


Figure 40 Relationship between GRAM Data and Output Level

13. Application

13.1. Configuration of Power Supply Circuit

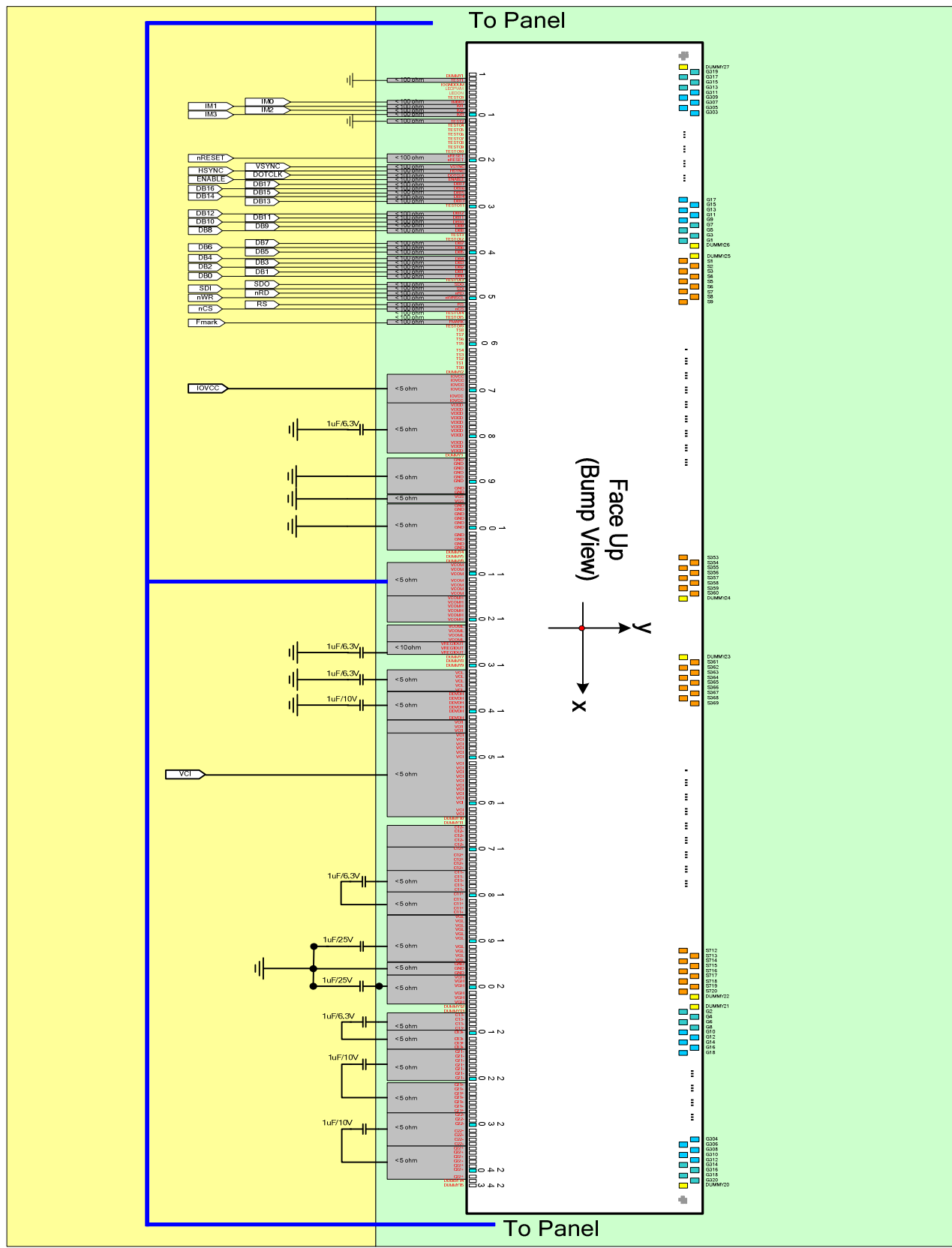


Figure 41 Power Supply Circuit Block

The following table shows specifications of external elements connected to the ILI9325D's power supply circuit.

Items	Recommended Specification	Pin connection
Capacity 1 μ F (B characteristics)	6.3V	VDDD, VCL, C11A/B, C13 A/B, VREG1OUT
	10V	DDVDH, C21 A/B, C22 A/B
	25V	VGH, VGL
Schottky diode	$V_F < 0.4\text{V}/20\text{mA}$ at 25°C , $V_R \geq 30\text{V}$ (Recommended diode: HSC226)	

13.2. Display ON/OFF Sequence

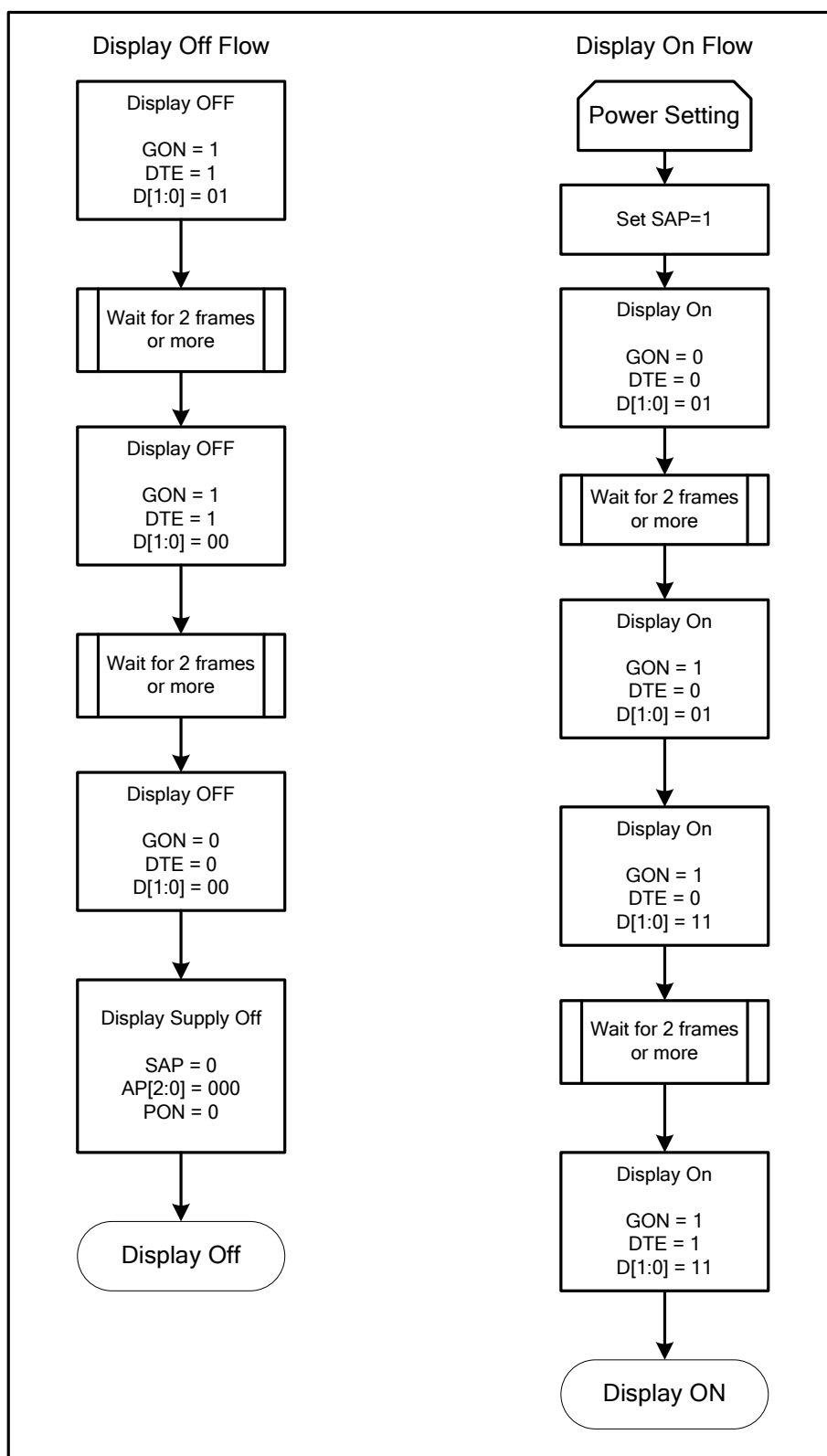


Figure 42 Display On/Off Register Setting Sequence

13.3. Standby and Sleep Mode

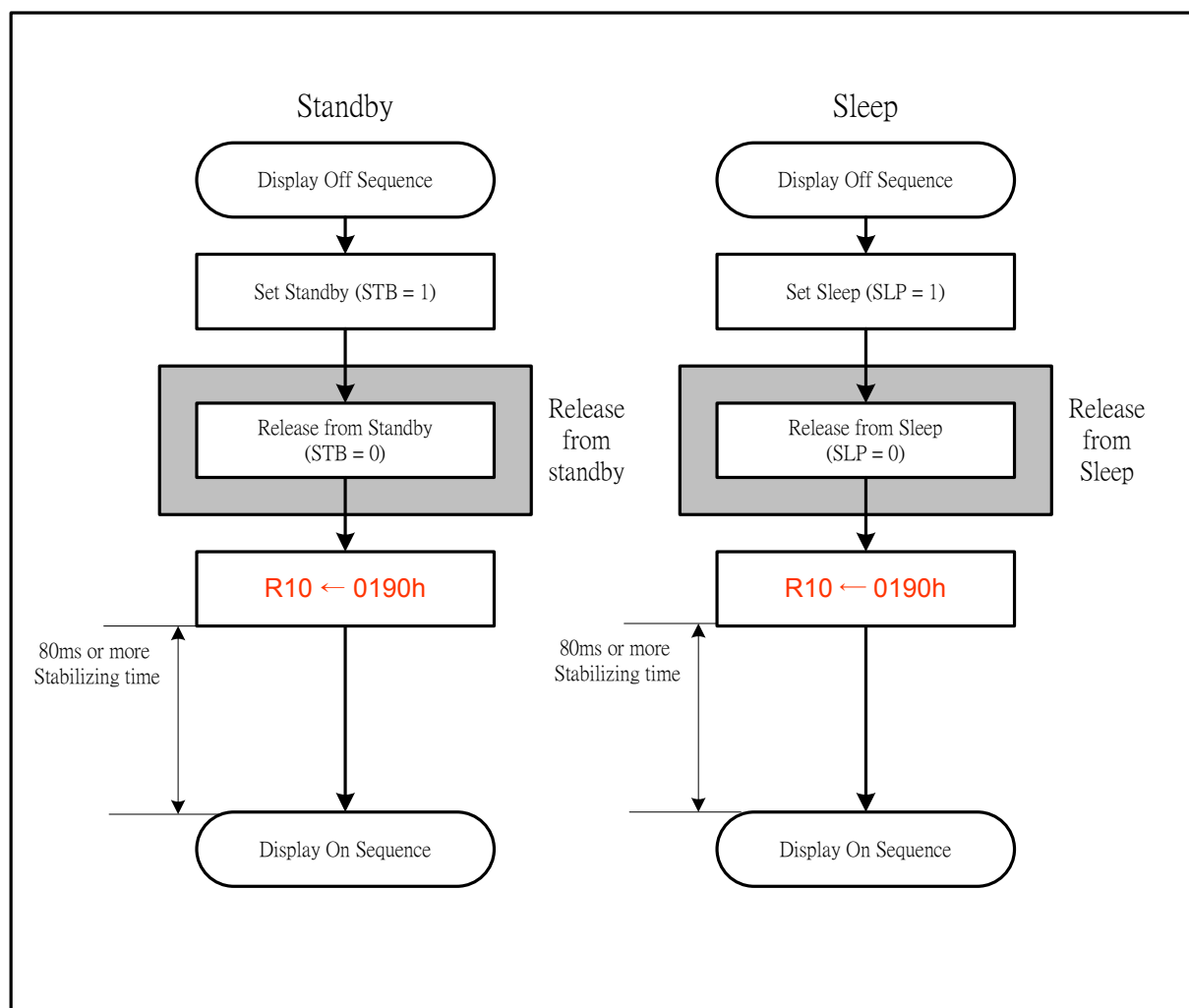


Figure 43 Standby/Sleep Mode Register Setting Sequence

13.4. Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for step-up circuits and operational amplifiers depends on external resistance and capacitance.

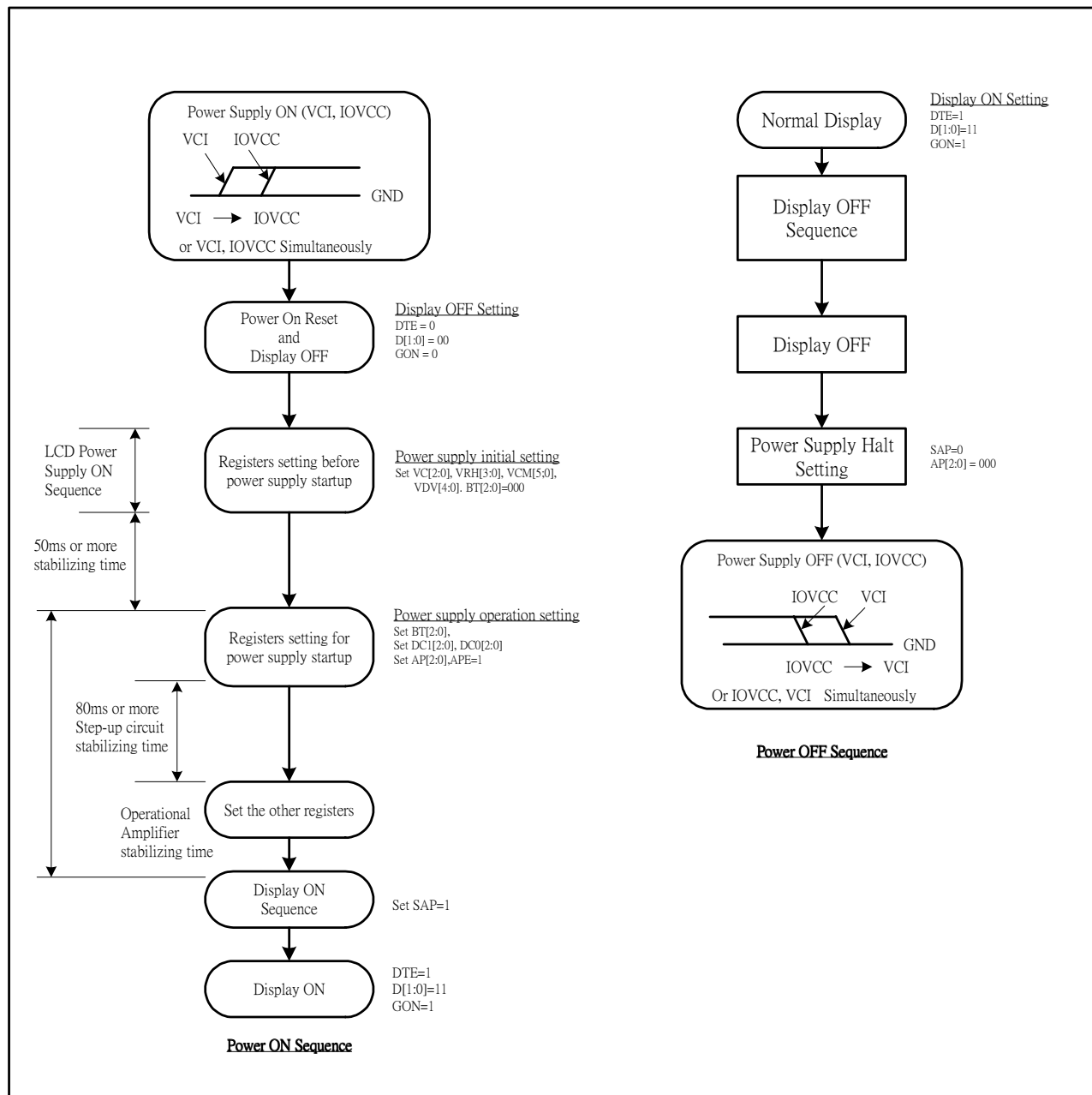


Figure 44 Power Supply ON/OFF Sequence

13.6. Applied Voltage to the TFT panel

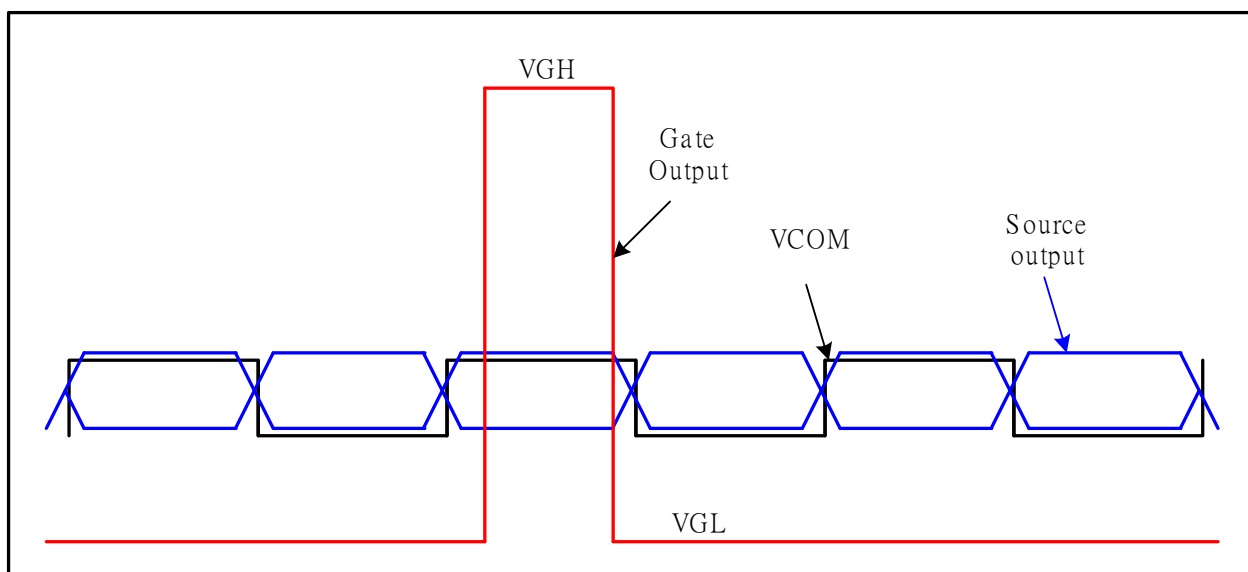


Figure 46 Voltage Output to TFT LCD Panel

13.7. Partial Display Function

The ILI9325D allows selectively driving two partial images on the screen at arbitrary positions set in the screen drive position registers.

The following example shows the setting for partial display function:

Base Image Display Setting	
BASEE	0
NL[5:0]	6'h27
Partial Image 1 Display Setting	
PTDE0	1
PTSA0[8:0]	9'h000
PTEA0[8:0]	9'h00F
PTDP0[8:0]	9'h080
Partial Image 2 Display Setting	
PTDE1	1
PTSA1[8:0]	9'h020
PTEA1[8:0]	9'h02F
PTDP1[8:0]	9'h0C0

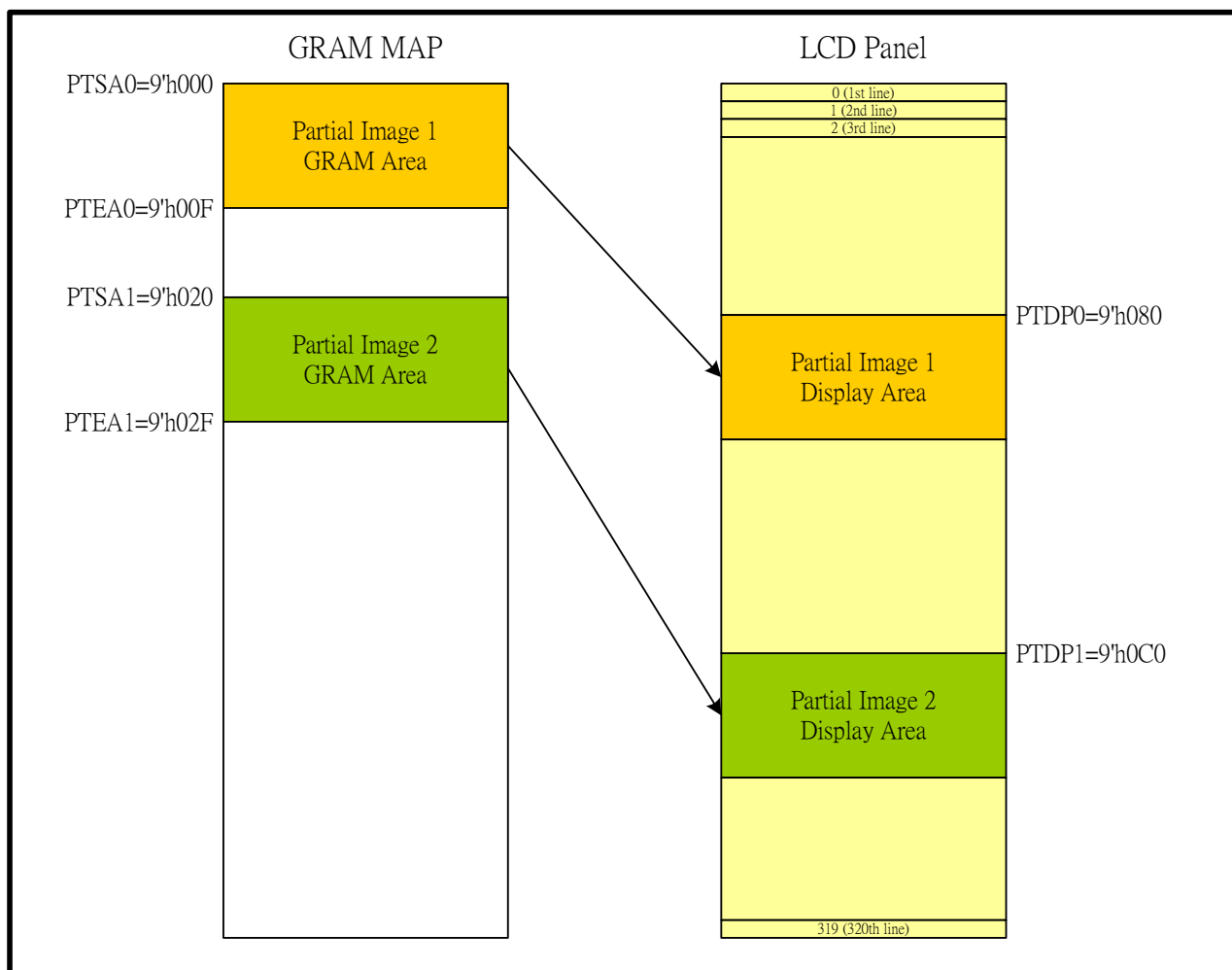


Figure 47 Partial Display Example

14. Electrical Characteristics

14.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9325D is used out of the absolute maximum ratings, the ILI9325D may be permanently damaged. To use the ILI9325D within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during operation, the ILI9325D will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power supply voltage (Digital)	IOVCC-GND	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (Analog)	VCI – GND	V	-0.3 ~ + 4.6	1, 2
Driver supply voltage range	DDVDH – GND	V	-0.3 ~ + 6.0	1, 4
	VCOMH-VCOML	V	-0.3 ~ + 6.0	1, 4
	GND –VCL	V	-0.3 ~ + 4.6	1
	DDVDH – VCL	V	-0.3 ~ + 9.0	1, 5
	VGH – VGL	V	-0.3 ~ + 30	6, 7
Input voltage	Vt	V	-0.3 ~ IOVCC+ 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	8
Storage temperature	Tstg	°C	-55 ~ + 110	8

Notes:

1. GND must be maintained
2. (High) VCI ≥ GND (Low), (High) IOVCC ≥ GND (Low).
3. Make sure (High) VCI ≥ GND (Low).
4. Make sure (High) DDVDH ≥ GND (Low).
5. Make sure (High) DDVDH ≥ VCL (Low).
6. Make sure (High) VGH ≥ GND (Low).
7. Make sure (High) GND ≥ VGL (Low).
8. For die and wafer products, specified up to 85°C.

14.2. DC Characteristics

(VCI=2.50 ~ 3.3V, IOVCC = 1.65 ~ 3.30V, Ta= -40 ~ 85 °C)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V _{IH}	V	IOVCC= 1.65 ~ 3.3V	0.7*IOVCC	-	IOVCC	-
Input low voltage	V _{IL}	V	IOVCC= 1.65 ~ 3.3V	0	-	0.3*IOVCC	-
Output high voltage (DB0 - DB17 Pins)	V _{OH1}	V	IOH = -0.1 mA	0.8*IOVCC	-	-	-
Output low voltage (DB0 - DB17 Pins)	V _{OL1}	V	IOVCC=1.65~3.3V	-	-	0.2*IOVCC	-
I/O leakage current	I _{LI}	μA	Vin = 0 ~ VCI	-1	-	1	-
Current consumption during normal operation (VCI - GND)+ (IOVCC - GND)	I _{OP}	mA	VCI=IOVCC=2.8V , Ta=25°C , Frame rate = 72 Hz, Line inversion VCIRE=1,VRH[3:0]=1100, VC[2:0]=001,BT[2:0]=100 VCM[5:0]=010111, VDV[4:0]=10011 AP[2:0]=001,PC0[2:0]=PC1[2:0]=010 REV=1, GRAM data=00000h No panel load	-	5.5	7.5	-
Sleep Current consumption (VCI - GND)+ (IOVCC - GND)	I _{SLP}	μA	VCI=IOVCC=2.8V , Ta=25°C No panel load	-	70	200	-
Current consumption during standby mode (VCI - GND)+ (IOVCC - GND)	I _{ST}	μA	VCI=IOVCC=2.8V , Ta=25°C No panel load	-	40	120	-
LCD Drive Power Supply Current (DDVDH-GND)	ILCD	mA	VCI=2.8V , VREG1OUT =4.8V DDVDH=5.2V , Frame Rate: 70Hz, line-inversion, Ta=25°C, GRAM data = 00000h,	-	5.5	-	-
LCD Driving Voltage (DDVDH-GND)	DDVDH	V	-	4.5	-	6	-
Output deviation voltage (Mean value)	V _{DEV}	mV	Gray scale voltage V0, V1, V62, V63			±60	1
	V _{DEV}	mV	Gray scale voltage V2 ~ V61	-	-	±40	1
Output offset voltage	V _{OFFSET}	mV	Gray scale voltage V0 ~ V63	-	-	±40	2

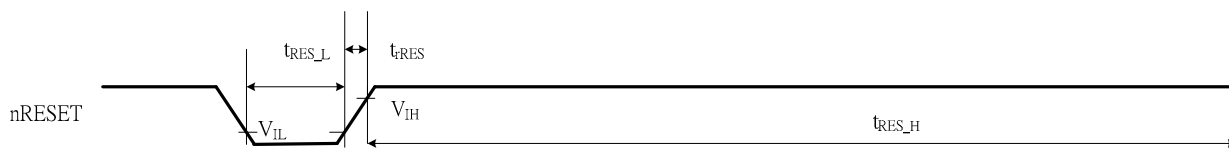
Note1: Deviation voltage = Max (Min) [S1,S2 ...,S720] – Mean [S1,S2,...S720].

Note2: The maximum value is between with measure point and Gamma setting value.

14.3. Reset Timing Characteristics

Reset Timing Characteristics (IOVCC = 1.65 ~ 3.3 V)

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	t _{RES_L}	ms	1	-	-
Reset rise time	t _{RES}	μs	-	-	10
Reset high-level width	t _{RES_H}	ms	50	-	-



14.4. AC Characteristics

14.4.1. i80-System Interface Timing Characteristics

Normal Write Mode (IOVCC = 1.65~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	80	-	-
	Read	t_{CYCR}	ns	300	-	-
Write low-level pulse width	PW_{LW}	ns	50	-	-	-
Write high-level pulse width	PW_{HW}	ns	15	-	-	-
Read low-level pulse width	PW_{LR}	ns	150	-	-	-
Read high-level pulse width	PW_{HR}	ns	150	-	-	-
Write / Read rise / fall time	t_{WRr}/t_{WRf}	ns	-	-	25	-
Setup time	Write (RS to nCS, E/nWR)	t_{AS}	ns	10	-	-
	Read (RS to nCS, RW/nRD)					
Address hold time	t_{AH}	ns	5	-	-	-
Write data set up time	t_{DSW}	ns	10	-	-	-
Write data hold time	t_H	ns	15	-	-	-
Read data delay time	t_{DDR}	ns	-	-	100	-
Read data hold time	t_{DHR}	ns	20	-	100	-

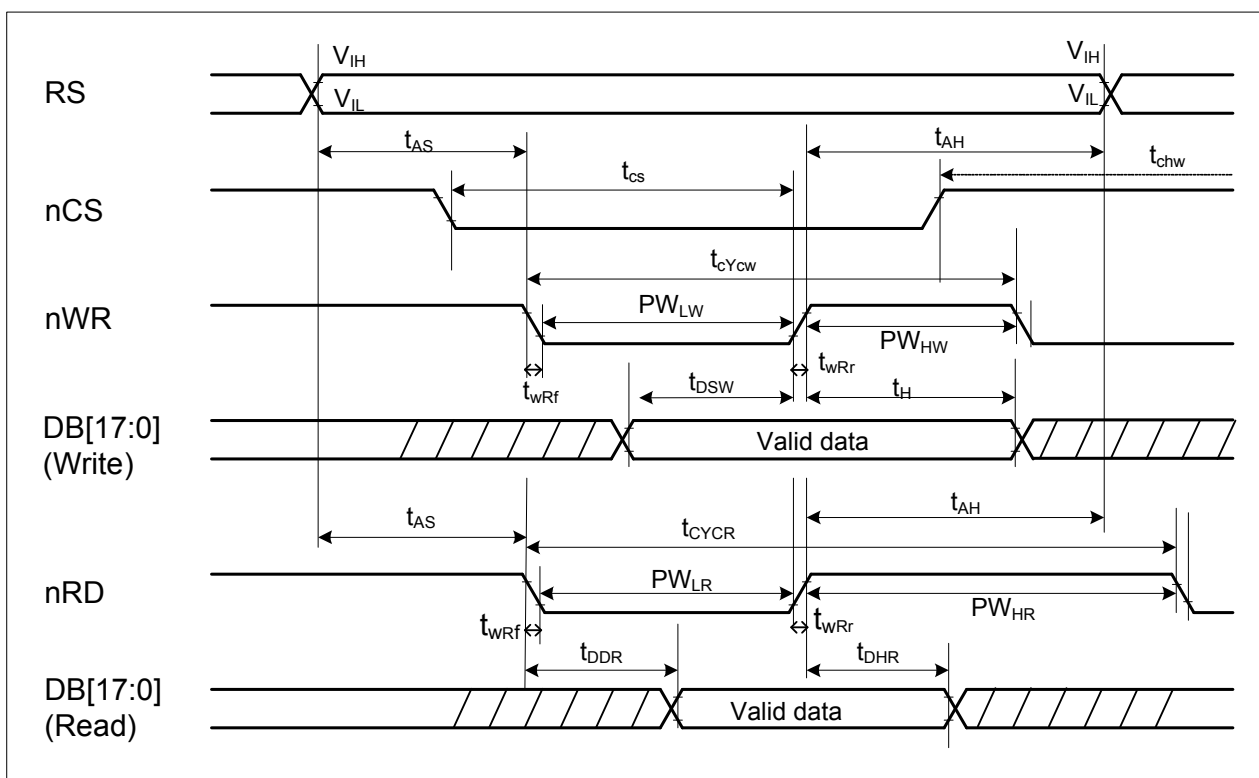


Figure 48 i80-System Bus Timing

14.4.2. Serial Data Transfer Interface Timing Characteristics

(IOVCC= 1.65 ~ 3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	μs	50	-	-
	Read (transmitted)	t_{SCYC}	μs	200	-	-
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	20	-	-
	Read (transmitted)	t_{SCH}	ns	100	-	-
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	20	-	-
	Read (transmitted)	t_{SCL}	ns	100	-	-
Serial clock rise / fall time	t_{SCr}, t_{SCf}	ns	-	-	5	
Chip select set up time	t_{CSU}	ns	10	-	-	
Chip select hold time	t_{CH}	ns	50	-	-	
Serial input data set up time	t_{SISU}	ns	15	-	-	
Serial input data hold time	t_{SIH}	ns	15	-	-	
Serial output data set up time	t_{SOD}	ns	-	-	100	
Serial output data hold time	t_{SOH}	ns	15	-	-	

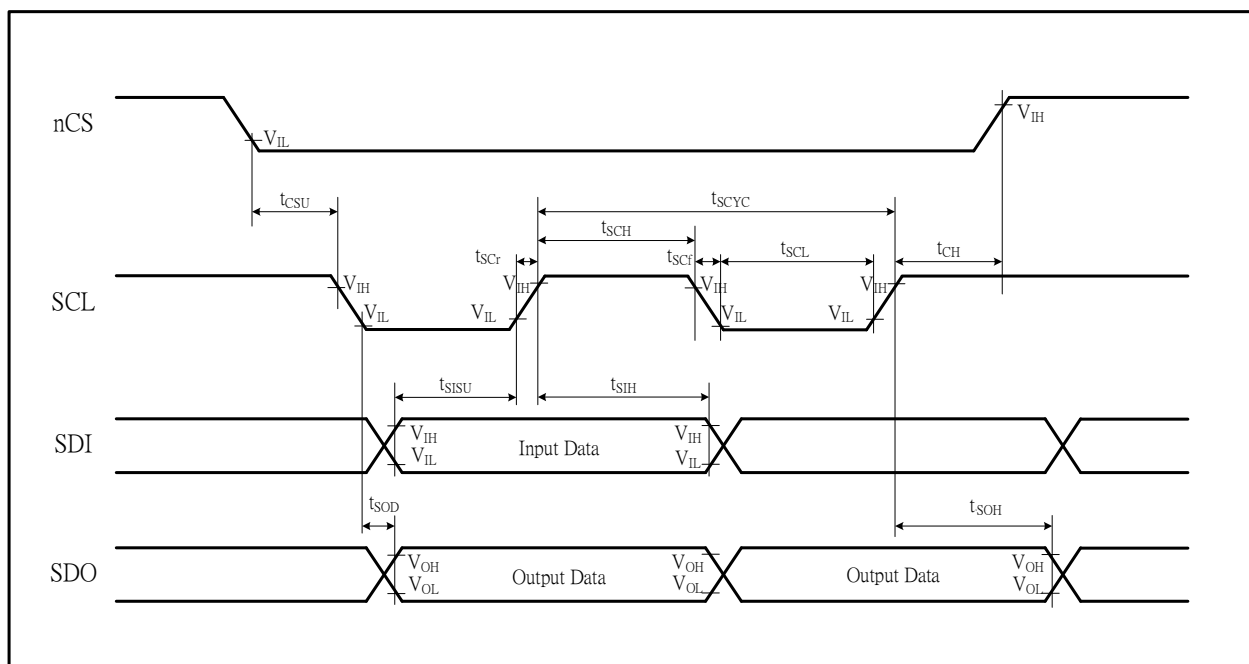


Figure 49 SPI system Bus Timing

14.4.3. RGB Interface Timing Characteristics

18/16-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	100	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-

6-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	30	-	-	-
DOTCLK high-level pulse width	PWDH	ns	30	-	-	-
DOTCLK low-level pulse width	PWDL	ns	30	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	80	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-

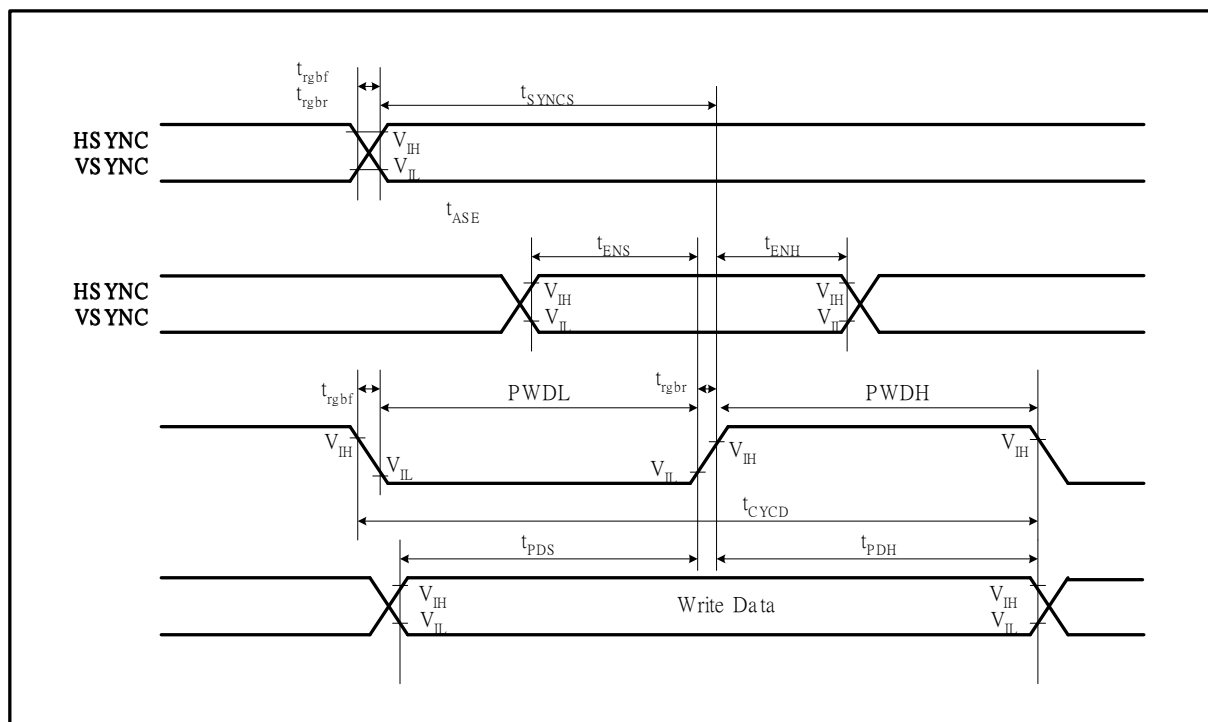


Figure 50 RGB Interface Timing

