HPSDR - USB Data Protocol

Revisions

Rev	Date	Changes	By
0.1	29 Jan 06	Original draft	VK6APH
0.2	30 Jan 06	Added I/Q designation to packet diagram. Added BPF and LPF to be on I2C	VK6APH
0.3	7 Feb 06	Modified number of bytes in sync/command bytes to be the same in both directions	VK6APH
0.4	9 Feb 06	Added explanation regarding choice of sync bytes	VK6APH
0.5	20 Feb 06	Changed protocol so that Microphone/Line data is sent at all times. Removed I2C data from control packets since now sent via FX2	VK6APH
1.0	25 Feb 06	Added note that V1.0 of Janus code runs at 48kHz	VK6APH
1.4	25 Feb 06	First version for public comment	VK6APH
1.5	1 May 06	Added MOX from PC, dot and dash inputs and A/D speed control	VK6APH
1.6	1 Aug 06	Updated Sync characters	VK6APH
1.7	28 May 07	Revised C&C data format	VK6APH
1.8	10 Sep 07	Revised C&C data format to include Penny and Mercury	VK6APH
1.9	17 Sept 07	Added number of bytes in FIFO to Tx protocol	VK6APH
1.10	24 Feb 08	Changed 125MHz clock reference to 122.88MHz. Changed Alex Attenuator options to 0/10/20/30dB. Added Class E or Normal mode. Added LT2208 Preamp gain Added LT2208 Overflow Added LT2208 Dither	VK6APH
1.11	25 May 08	Added LT2208 Random	VK6APH
1.12	2 June 08	Correct Left Right data	VK6APH
1.13	14 June 08	Added Alex antenna switching data	VK6APH
1.14	31 Jan 09	Changed LT2208 Preamp to Preamp Added Software serial numbers for Mercury and Penny Added ADC samples on EP4	VK6APH
1.15	3 Feb 09	Added Software serial number for Ozy	VK6APH
1.16	17 Feb 09	Added Penelope Forward Power	VK6APH
1.17	28 Mar 09	Added note regarding sampling rates to Ozy + EP4 notes	VK6APH
1.18	11Apr 09	Added note regarding initial clock selection	VK6APH
1.19	21Apr 09	Added support for Excalibur 10MHz clock	VK6APH
1.20	25 June 09	Explained Penny mic data	VK6APH
1.21	10 Aug 09	Split dot & PTT into separate signals (from Ozy V1.6)	VK6APH
1.22	14 Aug 09	Added fully Duplex capability (from Ozy V1.6) and multiple Mercury receivers (incomplete)	VK6APH
1.23	9 Sept 09	Completed multiple Mercury receiver support. Changed to fixed width font (Courier New – 8 pt)	VK6APH
1.24	13 Nov 09	Added support for Hermes and PennyLane	VK6APH
1.25	27 Feb 10	Clarified EP4 data size, pump prime corrected	VK6APH
1.26	2 July 10	Corrected two typos in Mercury data format	VK6APH
1.27	11 Nov 10	Added Metis to the mic gain settings. Added PennyLane to Power out settings	VK6APH
1.28	23 Jan 11	Added note re Drive setting when using Penelope and PennyLane	VK6APH
1.29	3 Feb 11	Added mic/Line-in selection for Metis with Penelope or PennyLane	VK6APH
1.30	4 Mar 11	Added C&C signals for four Mercury boards code version and ADC overload	VK6APH
1.31	26 Apr 11	Added C&C signals for selection and control of Apollo	VK6APH
1.32	7 Aug 11	Added C&C signals for FWD and REV power from Alex or Apollo	VK6APH
1.33	10 Sept 11	Added PC selection of Alex HPF & LPF filters	VK6APH
1.34	28 Sept 11	Added note re selection of Alex Rx out relay	VK6APH
1.35	29 Oct 11	Added time stamp option from Atlas A13 to LSB of mic data	VK6APH
1.36	6 Feb 12	Added common or separate frequencies to Mercury boards. Removed requirement for C4[2] to be set when using multiple Mercury boards. Added individual selection of pre-amp On/Off when using multiple Mercury boards. Suggest setting Drive level to zero when not transmitting.	K5SO
1.37	11 Apr 12	Added Hermes input IO4. Corrected location of Hermes software version in C&C data & added location of Metis software version.	VK6APH

1.38	7 May 12	Updated PTT, DOT & DASH pins on Hermes. Removed need to send initial frames to select Hermes clocks.	VK6APH
1.39	9 May 12	Added Cyclops PLL locked signal to C&C	VK6APH
1.40	3 Jun 12	Moved Cyclops PLL locked signal and added Mercury frequency changed to C&C	VK6APH
1.41	9 Sep 12	Added VNA mode to C&C	VK6APH
1.42	13 Sep 12	Added TLV320 line_boost control for Metis or Hermes	K5SO
1.43	4 Oct 12	Added control of pins 1-4 on Metis DB9 connector (JP7)	K5SO
1.44	15 Nov 12	Added support for 31dB stepped attenuator on Hermes	K5SO
1.45	30 Dec 12	Added disable Alex Tx relay for transverter use	K5SO
1.46	21 Jan 13	Added Hermes_atten_enable	K5SO
1.47	26 Jan 13	Added support for 384ksps sample rate	VK6APH
1.48	12 May 13	Added support for second 31dB attenuator for Angelia	K5SO
1.49	2 Jun 13	Removed selection for ADC1/ADC2 attenuator and provided independent control for each	K5SO
1.50	6 Mar 14	Added ability to assign receivers to a particular ADC. Added support for ADC3 attenuator.	K5SO
1.51	7 Mar 14	Added support for CW to be generated in the SDR hardware rather than the PC. Documented that I&Q are swapped on Tx.	VK6PH
1.52	14 Apr 14	Added support for Mic and PTT selection for Orion	VK5SO
1.53	1 May 14	Added C&C bit to disable Mic PTT on Orion	VK5SO
1.54	5 May 14	Added C&C bits for CW Keyer	VK6PH
1.55	17 May 14	Added Penelope selection for CW	VK6PH
1.56	5 Jun 14	Added independent Rx and Tx 0-31dB attenuator settings. Added PureSignal selection.	VK6PH
1.57	20 Jun 14	Changed Mercury(n) ADC overload to ADC(n) overload	K5SO
1.58	4 Aug 14	Added Max and Min values for PWM envelope generator	VK6PH
1.59	????	Added support for send LPF and HPF blocks	????
1.60	23 Jan 19	Added ET/EER Firmware Envelope Gain value	VK6PH

Protocol Overview:

- The USB data consists of 512 byte packets
- The sample rate from the receiver A/D converter to the PC is selectable between 48/96/192/384kHz at 24 bits
- The sample rate from the microphone to the PC is 48kHz at 16 bits
- The sample rate from the PC to the speakers/headphones is 48kHz at 16 bits
- The sample rate from the PC to the I/Q transmit audio is 48kHz at 16 bits
- Control signals that are high priority are sent each 512 block, lower priority data is sent less frequently

Functions required:

- PTT
- Dot/dash key active
- A/D sampling speed 384/192/96/48k
- NCO Frequencies
- Penelope Open Collector outputs
- Mercury Pre-amps and attenuator

Protocol

The protocol consists of a 512 byte frame consisting of a sync sequence, Command & Control data and ADC or DAC data.

A frame length of 512 bytes is used since this is the maximum number of bytes that the FIFO in the FX2 USB interface can hold.

High priority control data is sent as part of each frame e.g. PTT command/request. Lower priority data is sent as available on a predefined schedule e.g. NCO frequency.

Sync Sequence

This consists of a three byte sync sequence comprising <0x7F><0x7F><0x7F> . The sync sequence is sent at the start of every 512byte frame and appears at the start of the frame.

Protocol – From HPSDR to PC

HPSDR sends data to the PC over USB using End Points (EP) 4 and 6.

EP4.

HPSDR sends to EP4 a block of 4096 x 16 bit raw ADC samples. These are intended to be used to create a separate bandscope or ‘scope display of the RF input.
Data can be read from EP4 in 4k word (8k bytes) blocks. The start of each block will always be the start of the block of samples; hence no sync or start of block signal is required.

Data can be read at any time, it is not necessary to read at any particular data rate. At present the sample rate is 48kHz so a 4k word (8k bytes) buffer is available 10.7 time per second.

EP6.

The protocol consists of a frame of 512 bytes. Each frame starts with three sync bytes (0x7F, 0x7F, 0x7F) followed by five Command and Control (C&C) bytes (C0..C4). The first C&C byte(C0) bits [7:3] are used as an address that indicates what the next four bytes contain.

The balance of the frame consists of I, Q and microphone/line in samples (or left, right and microphone/line samples if a Janus card is being used).

For a **single** Mercury board/receiver, Hermes or Janus the protocol is as follows:

```
0                                                                   15
<Sync><Sync><Sync><C0><C1><C2><C3><C4><I2><I1><I0><Q2><Q1><Q0><M1><M0>

16                                                                  31
<I2><I1><I0><Q2><Q1><Q0><M1><M0><I2><I1><I0><Q2><Q1><Q0><M1><M0>

etc

504                         511
<I2><I1><I0><Q2><Q1><Q0><M1><M0>
```

Where:

```
Sync    – 0x7F
Cn      – Command/Control Byte
I2      – Bits 23-16 of I sample (Mercury/Hermes) or Left sample (Janus)
I1      – Bits  15-8 of I sample (Mercury/Hermes) or Left sample (Janus)
I0      – Bits   7-0 of I sample (Mercury/Hermes) or Left sample (Janus)
Q2      – Bits 23-16 of Q sample (Mercury/Hermes) or Right sample (Janus)
Q1      – Bits  15-8 of Q sample (Mercury/Hermes) or Right sample (Janus)
Q0      – Bits   7-0 of Q sample (Mercury/Hermes) or Right sample (Janus)
M1      – Bits  15-9 of Mic/Line sample
M0      – Bits   7-0 of Mic/Line sample
```

For **multiple** Mercury boards, or multiple receivers in the one Mercury/Hermes board, the protocol is extended as follows:

E.g. with 3 receivers

```
0                                   7
<Sync><Sync><Sync><C0><C1><C2><C3><C4>

8                                                                                                   27
<I1 2><I1 1><I1 0><Q1 2><Q1 1><Q1 0><I2 2><I2 1><I2 0><Q2 2><Q2 1><Q2 0><I3 2><I3 1><I3 0><Q3 2><Q3 1><Q3 0><M1><M0>

28                                                                                                  47
<I1 2><I1 1><I1 0><Q1 2><Q1 1><Q1 0><I2 2><I2 1><I2 0><Q2 2><Q2 1><Q2 0><I3 2><I3 1><I3 0><Q3 2><Q3 1><Q3 0><M1><M0>

Etc

492                                                             511
<Q2 2><Q2 1><Q2 0><I3 2><I3 1><I3 0><Q3 2><Q3 1><Q3 0><M1><M0><0><0><0><0>
```

Where:

I_n2 - Bits 23-16 of I sample for receiver n etc.

NOTE 1: where there are insufficient samples to exactly fill a 512 byte frame then the end of the frame is padded with 0s. The number of padded 0s is as follows:

Number of receivers	Padding
1	0
2	0
3	4
4	10
5	24
6	10
7	20
8	4

NOTE 2: The sample rate of the Microphone data is <u>always</u> 48kHz irrespective of the L/R (I&Q) sample rates. At 96/192/384kHz sample rates the microphone data is just duplicated and additional samples can be discarded as required.

Command & Control

NOTE: Bits **7-3** of C0 form an address that determines how C1-C4 should be decoded. C0 is varied round-robin fashion so that all addresses are sent in sequence.

C0

```
0 0 0 0 0 0 0 0
          | | |
          | | + --------- PTT  (1 = active, 0 = inactive), GPIO[23]= Ozy J8-8, Hermes J16-1
          | +------------ DASH (1 = active, 0 = inactive), GPIO[21]= Ozy J8-6, Hermes J6-2
          +-------------- DOT  (1 = active, 0 = inactive), GPIO[22]= Ozy J8-7, Hermes J6-3
```

C1

```
0 0 0 0 0 0 0 0
  | | | | | | |
  | | | | | | +---------- LT2208 Overflow (1 = active, 0 = inactive)
  | | | | | +------------ Hermes I01 (0 = active, 1 = inactive)
  | | | | +-------------- Hermes I02 (0 = active, 1 = inactive)
  | | | +---------------- Hermes I03 (0 = active, 1 = inactive)
  | | +------------------ Hermes I04 (0 = active, 1 = inactive)
  | +-------------------- Cyclops PLL locked (0 = unlocked, 1 = locked)
  +---------------------- Cyclops - Mercury frequency changed, bit toggles
```

C2 – Mercury software serial number (0 to 255) - set to 0 when Hermes
C3 - Penelope software serial number (0 to 255) – set to 0 when Hermes
C4 - Ozy/Magister or Metis or Hermes software serial number (0 to 255)

C0

0 0 0 0 **1** x x x

C1 – Bits 15-8 of Forward Power from Penelope or Hermes* (AIN5)
C2 - Bits 7-0 of Forward Power from Penelope or Hermes* (AIN5)
C3 – Bits 15-8 of Forward Power from Alex or Apollo*(AIN1)
C4 – Bits 7-0 of Forward Power from Alex or Apollo*(AIN1)

C0

0 0 0 **1** 0 x x x

C1 – Bits 15-8 of Reverse Power from Alex or Apollo*(AIN2)
C2 - Bits 7-0 of Reverse Power from Alex or Apollo*(AIN2)
C3 – Bits 15-8 of AIN3 from Penny or Hermes*
C4 – Bits 7-0 of AIN3 from Penny or Hermes*

C0

0 0 0 **1 1** x x x

C1 – Bits 15-8 of AIN4 from Penny or Hermes*
C2 - Bits 7-0 of AIN4 from Penny or Hermes*
C3 – Bits 15-8 of AIN6,13.8v supply on Hermes*
C4 – Bits 7-0 of AIN6,13.8v supply on Hermes*

*Note: All analog levels are 12 bits.

C0

0 0 **1 0 0** x x x

C1

```
0 0 0 0 0 0 0 0
|           | |
|           | +---------- ADC 1 Overflow (1 = active, 0 = inactive)
+-----------+------------ Mercury 1 software version (0 to 127)
                       (NOTE: This is a duplicate of C0 = 00000xxx to maintain software
                        compatibility)
```

C2

```
0 0 0 0 0 0 0 0
|           | |
|           | +---------- ADC 2 Overflow (1 = active, 0 = inactive)
+-----------+------------ Mercury 2 software version (0 to 127)
```

C3

```
0 0 0 0 0 0 0 0
|           | |
|           | +---------- ADC 3 Overflow (1 = active, 0 = inactive)
+-----------+------------ Mercury 3 software version (0 to 127)
```

C4

```
0 0 0 0 0 0 0 0
|           | |
|           | +---------- ADC 4 Overflow (1 = active, 0 = inactive)
+-----------+------------ Mercury 4 software version (0 to 127)
```

IMPORTANT: It is necessary to send a few C&C frames to select the desired clock source before data can be received from Ozy or Magister.

Protocol – From PC to HPSDR

The PC sends Command and Control plus two audio streams to the HPSDR on End Point 2 (EP2). The audio signals are:

1. 48kHz 16 bit Left/Right received audio
2. 48kHz 16 bit I/Q

Since the received audio is also used to monitor the transmitted audio then these two streams must be available simultaneously.

NOTE: The sampling rate, and hence data rate, is *ALWAYS* 48kHz and is independent of the sampling rate (e.g. 384/192/96/48kHz) set on the HPSDR to PC link.

IMPORTANT: It is necessary to send a few C&C frames to select the desired clock source before data can be received from Ozy.

Since the DACs use 16 bits per sample then, in order that an integer number of Left/Right and I/Q samples will be included in the 512 byte packed, the maximum number of samples is

(512 – 8) = 63 x 4 x 2 bytes i.e. 63 Receiver L/R samples and 63 I/Q L/R samples

This provides 8 bytes to transfer status data from the PC to the FPGA. The first characters in the 512 byte packet will be sync which is 0x7F7F7F. Since 3 bytes are required for the sync character 5 bytes are used to send Command & Control data.

```
0                                                                   15
<Sync><Sync><Sync><C0><C1><C2><C3><C4><L1><L0><R1><R0><I1><I0><Q1><Q0>

 16                                                                  31
<L1><L0><R1><R0><I1><I0><Q1><Q0><L1><L0><R1><R0><I1><I0><Q1><Q0>

Etc

496                                                                 511
<L1><L0><R1><R0><I1><I0><Q1><Q0><L1><L0><R1><R0><I1><I0><Q1><Q0>
```

Where:

```
Sync    – 0x7F
Cn      – Command/Control Byte
L1      – Bits  15-8 of Left audio sample
L0      – Bits   7-0 of Left audio sample
R1      – Bits  15-8 of Right audio sample
R0      – Bits   7-0 of Right audio sample
I1      – Bits  15-8 of I sample
I0      – Bits   7-0 of I sample
Q1      - Bits  15-8 of Q sample
Q0      - Bits   7-0 of Q sample
```

Note: When using Hermes or PennyLane the Transmitter output level is set by the drive level value (C0 = 0b0001001x, C1 = 0x00 to 0xFF) and not by the amplitude of the I&Q signals. These are held to a peak value of +/-1.0 by AGC action in the PC DSP code. When using Penelope the amplitude of the I&Q signals controls the output level. Set the drive level (C1) to 0x00 when Penelope is selected and whilst the transmitter is not active.

NOTE: The I&Q samples, relative to receive, are reversed. This is a historical bug that goes back to the very first version of PowerSDR. Simply swap I&Q in the PC code before sending to rectify this problem. It's too engrained, for too many years, to change now.

Command & Control

NOTE: Bits **7-1** of C0 form an address that determines how C1-C4 should be decoded. C0 is varied round-robin fashion so that all addresses are sent in sequence.

C0
0 0 0 0 0 0 0 0
|
+------------ MOX (1 = active, 0 = inactive)

C1
0 0 0 0 0 0 0 0
| | | | | | | |
| | | | | | + +------------ Speed (00 = 48kHz, 01 = 96kHz, 10 = 192kHz, 11 = 384kHz)
| | | | + +---------------- 10MHz Ref. (00 = Atlas/Excalibur, 01 = Penelope, 10 = Mercury)*
| | | +-------------------- 122.88MHz source (0 = Penelope, 1 = Mercury)*
| + +---------------------- Config (00 = nil, 01 = Penelope, 10 = Mercury, 11 = both)*
+------------------------- Mic source (0 = Janus, 1 = Penelope)*

* Ignored by Hermes

C2
0 0 0 0 0 0 0 0
| | |
| | | +------------ Mode (1 = Class E, 0 = All other modes)
+---------- +-------------- Open Collector Outputs on Penelope or Hermes (bit 6…..bit 0)

C3
0 0 0 0 0 0 0 0
| | | | | | | |
| | | | | | + +------------ Alex Attenuator (00 = 0dB, 01 = 10dB, 10 = 20dB, 11 = 30dB)
| | | | | +---------------- Preamp On/Off (0 = Off, 1 = On)
| | | | +------------------ LT2208 Dither (0 = Off, 1 = On)
| | | + ------------------- LT2208 Random (0= Off, 1 = On)
| + + ---------------------- Alex Rx Antenna (00 = none, 01 = Rx1, 10 = Rx2, 11 = XV)
+ ------------------------- Alex Rx out (0 = off, 1 = on). Set if Alex Rx Antenna > 0.

C4
0 0 0 0 0 0 0 0
| | | | | | | |
| | | | | | + + ------------ Alex Tx relay (00 = Tx1, 01= Tx2, 10 = Tx3)
| | | | | + ---------------- Duplex (0 = off, 1 = on)
| | + + +------------------- Number of Receivers (000 = 1, 111 = 8)
| +------------------------ Time stamp – 1PPS on LSB of Mic data (0 = off, 1 = on)
+-------------------------- Common Mercury Frequency (0 = independent frequencies to Mercury
Boards, 1 = same frequency to all Mercury boards)

C0
0 0 0 0 0 0 **1** x **C1, C2, C3, C4** NCO Frequency in Hz for Transmitter, Apollo ATU
(32 bit binary representation - MSB in C1)

C0
0 0 0 0 0 **1** 0 x **C1, C2, C3, C4** NCO Frequency in Hz for Receiver_1

C0
0 0 0 0 0 **1 1** x **C1, C2, C3, C4** NCO Frequency in Hz for Receiver _2

C0
0 0 0 0 **1** 0 0 x **C1, C2, C3, C4** NCO Frequency in Hz for Receiver _3

C0
0 0 0 0 **1** 0 **1** x **C1, C2, C3, C4** NCO Frequency in Hz for Receiver _4

C0
0 0 0 0 **1 1** 0 x **C1, C2, C3, C4** NCO Frequency in Hz for Receiver _5

C0
0 0 0 0 **1 1 1** x **C1, C2, C3, C4** NCO Frequency in Hz for Receiver _6

C0
0 0 0 **1** 0 0 0 x **C1, C2, C3, C4** NCO Frequency in Hz for Receiver _7

C0
0 0 0 **1** 0 0 **1** x

C1
```
0 0 0 0 0 0 0 0
|             |
+-------------+------------ Hermes/PennyLane Drive Level (0-255)[1]
```

[1] Ignored by Penelope

C2
```
0 0 0 0 0 0 0 0
| | | | | | | |
| | | | | | | +------------ Hermes/Metis Penelope Mic boost (0 = 0dB, 1 = 20dB)
| | | | | | +-------------- Metis/Penelope or PennyLane Mic/Line-in (0 = mic, 1 = Line-in)
| | | | | +---------------- Hermes – Enable/disable Apollo filter (0 = disable, 1 = enable)
| | | | +------------------ Hermes – Enable/disable Apollo tuner (0 = disable, 1 = enable)
| | | +-------------------- Hermes – Apollo auto tune (0 = end, 1 = start)
| | +---------------------- Hermes – select filter board (0 = Alex, 1 = Apollo)
| +------------------------ Alex   - manual HPF/LPF filter select (0 = disable, 1 = enable)[2]
+-------------------------- VNA Mode (0 = off, 1 = on)
```

C3
```
0 0 0 0 0 0 0 0
| | | | | | | |
| | | | | | | +------------ Alex   -  select 13MHz  HPF (0 = disable, 1 = enable)[2]
| | | | | | +-------------- Alex   -  select 20MHz  HPF (0 = disable, 1 = enable)[2]
| | | | | +---------------- Alex   -  select 9.5MHz HPF (0 = disable, 1 = enable)[2]
| | | | +------------------ Alex   -  select 6.5MHz HPF (0 = disable, 1 = enable)[2]
| | | +-------------------- Alex   -  select 1.5MHz HPF (0 = disable, 1 = enable)[2]
| | +---------------------- Alex   -  Bypass all HPFs   (0 = disable, 1 = enable)[2]
| +------------------------ Alex   -  6M low noise amplifier (0 = disable, 1 = enable)[2]
+-------------------------- Disable Alex T/R relay (0 = enable, 1 = disable)
```

C4
```
0 0 0 0 0 0 0 0
  | | | | | | |
  | | | | | | +------------ Alex   -  select 30/20m LPF (0 = disable, 1 = enable)[2]
  | | | | | +-------------- Alex   -  select 60/40m LPF (0 = disable, 1 = enable)[2]
  | | | | +---------------- Alex   -  select 80m    LPF (0 = disable, 1 = enable)[2]
  | | | +------------------ Alex   -  select 160m   LPF (0 = disable, 1 = enable)[2]
  | | +-------------------- Alex   -  select 6m     LPF (0 = disable, 1 = enable)[2]
  | +---------------------- Alex   -  select 12/10m LPF (0 = disable, 1 = enable)[2]
  +------------------------ Alex   -  select 17/15m LPF (0 = disable, 1 = enable)[2]
```

[2] Only valid when Alex - manual HPF/LPF filter select is enabled

C0
0 0 0 **1** 0 **1** **0** x

C1
```
0 0 0 0 0 0 0 0
  | | | | | | |
  | | | | | | +------------ Rx1 pre-amp (0=OFF, 1= ON)
  | | | | | +-------------- Rx2 pre-amp (0=OFF, 1= ON)
  | | | | +---------------- Rx3 pre-amp (0=OFF, 1= ON)
  | | | +------------------ Rx4 pre-amp (0=OFF, 1= ON)
  | | +-------------------- Orion tip/ring select (0 = micPTT to ring, mic/mic bias to tip,
  | |                                               1 = micPTT to tip, mic/mic bias to ring)
  | +---------------------- Orion mic bias (0 = disable, 1 = enable)
  +------------------------ Orion mic PTT  (0 = enable, 1 = disable)
```

C2
```
0 0 0 0 0 0 0 0
| | | |       |
| | | +------ +------------ TLV320 Line-in Gain [4:0]
| | +---------------------- If set enable 20dB Attenuator on Mercury when on Tx*
| +------------------------ PureSignal (0 = disable, 1 = enable)
+------------------------- Penelope selected (0 = false, 1 = true) used for CW
```

[3] Sets TLV320 line_boost value for Ethernet based boards
*if common setting used.

C3
```
0 0 0 0 0 0 0 0
      | | | | |
      | | | | +------------ Metis DB9 pin 1 Open Drain Output (0=OFF, 1= ON)
      | | | +-------------- Metis DB9 pin 2 Open Drain Output (0=OFF, 1= ON)
      | | +---------------- Metis DB9 pin 3 3.3v TTL Output (0=OFF, 1= ON)
      | +------------------ Metis DB9 pin 4 3.3v TTL Output (0=OFF, 1= ON)
      +-------------------- 20dB Attenuator on Mercury when Tx (0 = disable, 1 = enable)
```

C4
```
0 0 0 0 0 0 0 0
    | |       |
    | +-------+------------ ADC1 Input Attenuator Rx (0 – 31dB) [4:0]
    +---------------------- Hermes/Angelia Attenuator enable (0 = disable, 1 = enable)
                            If disabled then Preamp On/Off bit is used.
```

C0
0 0 0 **1** 0 **1** **1** x

C1
```
0 0 0 0 0 0 0 0
    | |       |
    | +-------+------------ ADC2 Input Attenuator Rx (0-31dB) [4:0]
    +---------------------- ADC2 Input Attenuator enable (0 = disable, 1 = enable)
                           If disabled then attenuation is 0dB.
```

C2
```
0 0 0 0 0 0 0 0
  | | |       |
  | | +-------+------------ ADC3 Input Attenuator Rx (0-31dB) [4:0]
  | +---------------------- ADC3 Input Attenuator enable (0 = disable, 1 = enable)
  |                        If disabled then attenuation is 0dB.
  +------------------------ CW keys reversed (0 = disable, 1 = enable)
```

C3
```
0 0 0 0 0 0 0 0
| | |         |
| | +---------+------------ Keyer speed [5:0] (1-60 WPM)
+-+------------------------ Keyer Mode [1:0] (00 = straight, 01 = Mode A, 10 = Mode B)
```

C4
```
0 0 0 0 0 0 0 0
| |           |
| +-----------+------------ Keyer Weight [6:0] (0 – 100)
+-------------+------------ Keyer Spacing (0 = off, 1 = on)
```

C0
```
0 0 0 1 1 0 0 x             Reserved for additional Mercury Boards
```

C0
```
0 0 0 1 1 0 1 x             Reserved for additional Mercury Boards
```

C0
```
0 0 0 1 1 1 0 x
```

C1
```
0 0 0 0 0 0 0 0
| | | | | | | |
| | | | | | +-+------------ ADC assignment for RX1 (00 = ADC1, 01 = ADC2, 10 = ADC3)
| | | | +-+---------------- ADC assignment for RX2 (00 = ADC1, 01 = ADC2, 10 = ADC3)
| | +-+-------------------- ADC assignment for RX3 (00 = ADC1, 01 = ADC2, 10 = ADC3)
+-+------------------------ ADC assignment for RX4 (00 = ADC1, 01 = ADC2, 10 = ADC3)
```

C2
```
0 0 0 0 0 0 0 0
    | | | | | |
    | | | | +-+------------ ADC assignment for RX5 (00 = ADC1, 01 = ADC2, 10 = ADC3)[4]
    | | +-+---------------- ADC assignment for RX6 (00 = ADC1, 01 = ADC2, 10 = ADC3)
    +-+-------------------- ADC assignment for RX7 (00 = ADC1, 01 = ADC2, 10 = ADC3)
```

[4] Except on Tx where RX5 input is assigned to the Tx DAC

C3
```
0 0 0 0 0 0 0 0
      |       |
      +-------+------------ ADC Input Attenuator Tx (0-31dB) [4:0]
```

C4 – not presently used

C0
```
0 0 0 1 1 1 1 x
```

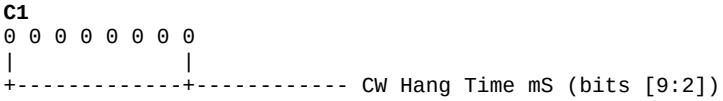
C1
```
0 0 0 0 0 0 0 0
              |
              +------------ CW (0 = External, 1 = Internal)
```

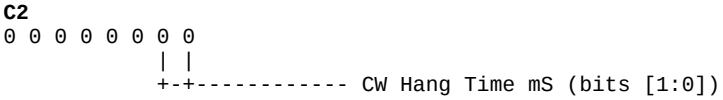
C2
```
0 0 0 0 0 0 0 0
|             |
+-------------+------------ CW Sidetone Volume (0 to 127 [7:0])
```

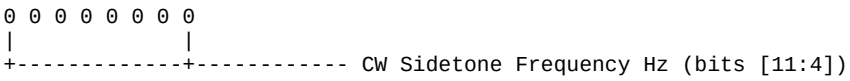
C3
```
0 0 0 0 0 0 0 0
|             |
+-------------+------------ CW PTT delay mS (0 to 255 [7:0])
```

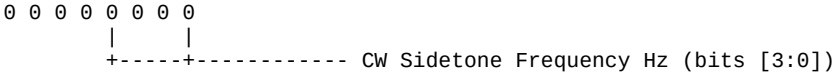
C4 currently not used – reserved for raised cosine profile time if required

C0
0 0 **1** 0 0 0 0 x

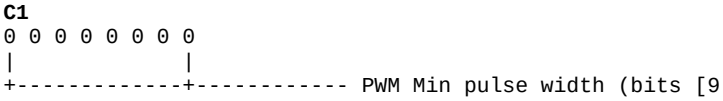
C1


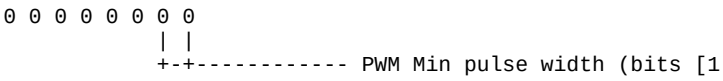
C2


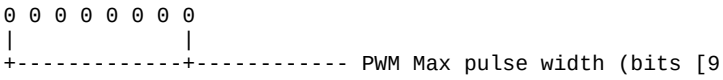
C3


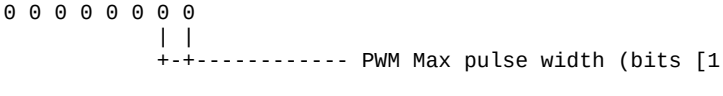
C4


C0
0 0 **1** 0 0 0 **1** x

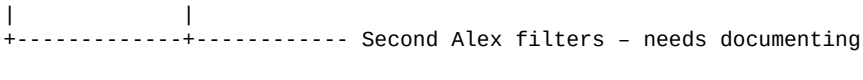
C1


C2


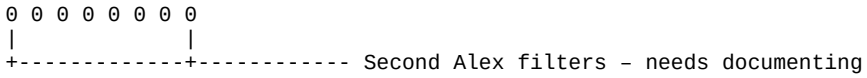
C3


C4


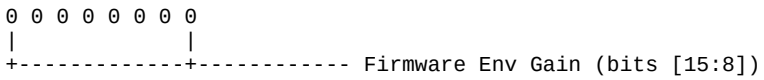
C0
0 0 **1** 0 0 **1 0** x

C1


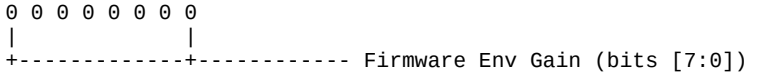
C2


0 0 0 0 0 0 0 0
Second Alex filters – needs documenting

C3


0 0 0 0 0 0 0 0
Firmware Env Gain (bits [15:8])

C4


0 0 0 0 0 0 0 0
Firmware Env Gain (bits [7:0])

ENDS