Documentation of Photocurrent Sampling Amplifier

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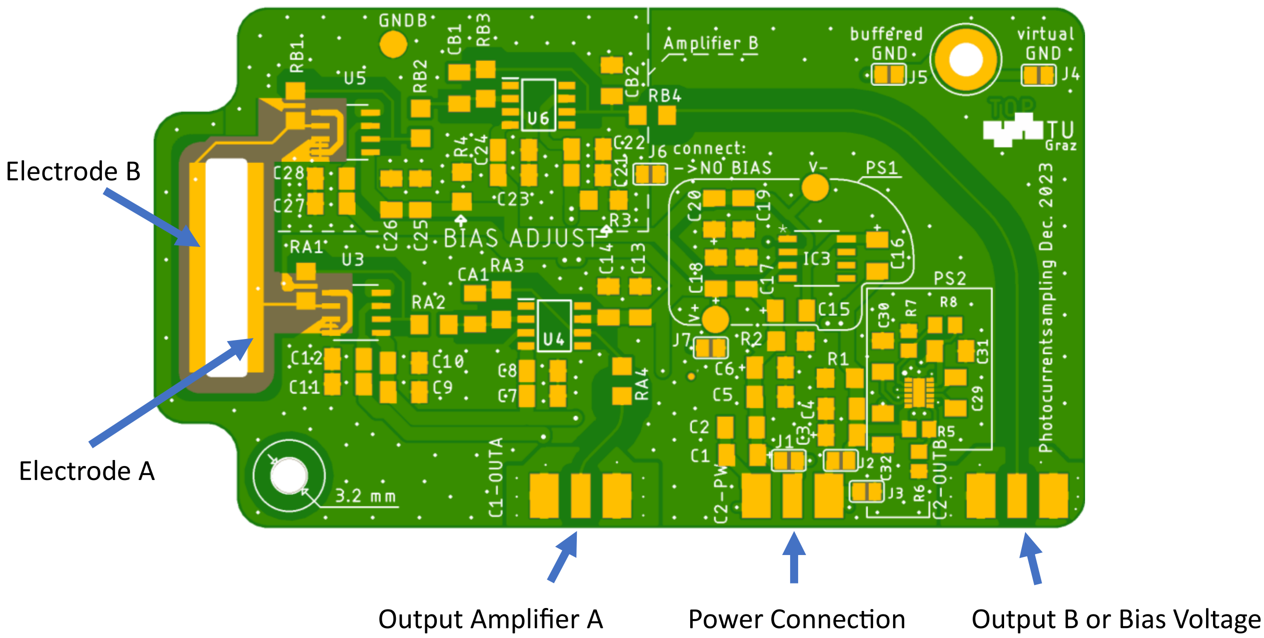
This document contains a detailed description of how to build and use a transimpedance amplifier that is specifically tuned to the task of photocurrent sampling. A more concise description containing the minimum information to build and operate the device is contained in 'Quick Guide PCS PCB_en.pdf'. More information on the design process is available in the bachelor thesis 'Photocurrent Sampling in free Air'. Files mentioned within the document are available in this repository.

Content

PCB Layout



The layout and circuit diagram are available as Autodesk Eagle files (PCSoposeLM.brd, PCSoposeLM.sch). In addition, Gerber files are also available in the repository.

Intended use

The PCB and circuit can be used to amplify currents produced by a strong laser field that interacts with some gas or material (Photo Current Sampling / PCS). The PCB can be operated in a fine to high vacuum to observe ions of pure gases at low pressures.

The currents are collected at the electrodes A and B and can range from pA to µA according to the amplification gain that is chosen. To collect these currents, electrodes made out of sheet metal can be soldered onto the gold-plated electrodes. To prevent the electrode elements from acting as antenna, the whole PCB should be placed inside a metal enclosure.

The outputs are voltages with a range from +/- 2.5 V, provided on the SMA connector that corresponds to the respective amplifier / electrode (A / B). The output voltage is proportional to the input current times the gain that is set by the components. Linearity is guaranteed up to +/- 2 V when connected to a load of 1k$\Ohm$ or bigger.

Gain Settings

Electrode A and electrode B are each connected to an independent amplification circuit. For both A and B, the same rules apply, therefore the following description uses only the component designations corresponding to A.

The overall gain is the product of the transimpedance of the first stage and the gain of the second stage.

First Stage

The first stage or input stage consist of a LTC6268-10 in a transimpedance amplifier configuration. The value of the feedback resistor RA1 sets the TIA gain. Bigger RA1 values increase the DC-transimpedance linear, however noise is only increased proportional to $\sqrt{R_{A1}}$. Therefore, SNR (Signal to Noise Ratio) of

DC (and slow) signals is improved with increasing RA1. The bandwidth decreases when increasing RA1, however the datasheet of LTC6268-10 is ambiguous about the proportionality:

Equation 1: $f_{-3dB} \approx \frac{1}{2*\pi*C_{par}*R_{A1}}$ (Results some percent better than experiment)

Equation 2: $f_{-3dB} \approx \sqrt{\frac{GBW}{2*\pi*C_{par}*R_{A1}}}$ (Results are orders of magnitude away from experiment)

Experiment data is best matched by Equation 1, which is also used for prediction of values. However, the circuit has only been tested up to 10 MHz and effects of *GBW* are expected to play a significant role at higher frequencies, closer to the *GBW*.

$C_{par} \approx 40 - 60$fF

$GBW \approx 4$ GHz (laut LTC6268-10 Datasheet)

SNR of short pulses has to be treated differently than for DC. In photocurrent sampling, packets of charge arrive at the electrodes. This event is typically shorter than what can be resolved by this amplifier and thus produces a smeared-out peak. The integral over one peak created by such an event is proportional to the amount of charge that arrived at the electrode. The signal is therefore typically recorded with a lock-in amplifier or boxcar amplifier. The amplitude of these short pulses is not only governed by the transimpedance, but also depends on the bandwidth of the amplifier, as does the noise. Higher bandwidth leads to shorter and taller peaks and in turn improves SNR.

This effect of increased bandwidth and sharper peaks (according to eq. 1) does almost cancel out the loss of DC gain when reducing RA1. This results in the value of RA1 having little influence on the amplitude of the signal pulses created by short charge packets, as long as the current to the input has a duration << $1/f_{-3dB}$. Smaller values of RA1 still affect DC transimpedance and decrease the visibility of DC input currents as well as increasing the bandwidth.

Second Stage

Operational amplifier OPA380 in inverting configuration.

The purpose of the second stage is to decouple the sensitive output of the LTC6268-10 from capacitive or ohmic loads presented by the oscilloscope or other instruments attached to the output. At the same time, additional gain and a lowpass filter can be incorporated into the second stage.

Second stage gain: $-\frac{R_{A3}}{R_{A2}}$

Lowpass: $f_{-3dB} \approx \frac{1}{2*\pi*R_{A3}*C_{A1}}$

A sensible approach is to set the corner frequency f_{-3dB} of the lowpass the same as the corner frequency of the first stage. This cuts away only the high frequency noise that does not contain signal. In order to achieve minimal noise while only barely compromising bandwidth, the lowpass corner frequency can be set a little bit below that of the first stage. On the other hand, a reasonable flat transfer curve and low distortion while maintaining good noise figures can be obtained when the lowpass corner frequency is set to about three times that of the first stage. The transfer function can be simulated and optimized using the LT-Spice file ‘2ndStageRCcalculator.asc’.

The values of resistor RA1 and RA2 should be at least 1 kΩ. Much bigger values will introduce additional Johnson-Nyquist noise. CA1 should be a ceramic capacitor with dielectric of type NP0 / C0G.

Overall transimpedance (DC):

$$Gain = R_{A1} * \frac{R_{A3}}{R_{A2}}$$

Currents flowing into the electrode lead to a positive voltage signal on the output. Note that electrons hitting the electrode cause a technical current flow out of the electrode.

In the following table, suggestions for component values are given. These values can be used as a starting point for experiments. Alternatively, values for various configurations are listed in file 'Quick Guide PCS PCB_en.pdf'.

Table 1: Suggestions for component values. This will result in approximately 250 kHz bandwidth, DC-transimpedance of 10 MΩ

RA1	10MΩ
RA2	10kΩ
RA3	10kΩ
CA1	22pF

Power Supply Settings

There are three possible ways to supply the circuit with power:

PS1

PS1 needs a symmetrical voltage supply. The outer conductor of the connector C2-PW carries the negative voltage (-2.5 V) and the inner conductor carries the positive voltage (+2.5 V). A potential free 5V power supply is appropriate for this task, the GND voltage for the circuit is then generated by a TLE2426 rail splitter on the PCB. A well-suited power supply is described in the file 'LowNoisePSU_doc_en.pdf'XX.

No charge pump (TLE2426) (PS1):

- J1: connect
- J2: connect
- J3: not connect
- J4 = connection of voltage divider GND to housing, OR J5 = buffered GND der of signal output to housing)
- J4 AND J5: connects internal (voltage divider) ground to output ground
- PS2 area (solid line with sharp corners) do not populate.
    - R5-R8 do not populate
    - C29-C32 do not populate
- Input voltage: J2-PW should be connected to 5V low noise voltage source, capable of providing at least 40 mA per populated amplifier (measured: A~33mA, A&B <80mA) The outer conductor of J2-PW (shielding) is at -2,5 V below ground potential, therefore only feedthroughs with floating shield can be used.
  Suitable power supply: see *LowNoisePSU-DokuXXXXXXX*

PS2

PS2 only requires a positive power supply (approx. 3.3 V) on the inner conductor, the positive and negative voltage of +/- 2.5 V is then generated by an LM27762 charge pump on the circuit board. With this variant, the outer conductor of the power supply has to be grounded.

This version has not been tested in a photo current sampling experiment. It seemingly worked fine in test runs in air with simulated signals. If problems occur, they most likely will stem from the switching frequency of the charge pump. With correct component values and current draw, the switching frequency should be around 2 MHz and should not adversely affect configurations with lower bandwidth.

Charge pump LM27762 (PS2):

- J1: NC
- J2: NC
- J3: connect
- J4: connect
- J5: connect
- J7: connect
- Cxx: Durch Kerko x.xuF ersetzen
- PS1 area (rounded solid line) do not populate
- PS2 area (solid line with sharp corners) populate
- do not populate R1 & R2
- do not populate TLE2624 (=IC3)
- do not populate C15-C20. However, no problem if already populated.
- Input voltage: J2-PW should be connected to a 3-5V voltage source that provides double the current as needed for a PS1 configuration. The outer conductor of J2-PW (shielding) is at ground potential, therefore grounded feedthroughs can be used.

Bias Settings

No bias = 0 V between both electrodes / both TIA inputs:

In reality there may be a bias voltage corresponding to the difference of the offset voltages of the LTC6268-10. (U_{Offset} << 10mV)

- J6: connect
- R1 & R2 populate both with 1 kΩ
- R3 & R4 (BIAS ADJUST): do not populate OR populate both with 1 kΩ

Fixed Bias:

- J6: NC
- Voltage divider B input bias: + R3—V_B—R4-
- Voltage divider A input bias: + R2—V_B—R1- (A-Bias only possible when using PS1)
- Deviations of the voltage dividers from 1:1 will be visible on the output as a DC component of the signal
- The sum of R of each voltage divider should be around 2 kΩ

$$U_{Bias_B} = U_{Betrieb} \cdot \left(\frac{R_4}{R_3 + R_4} - 0.5\right)$$

B electrode as variable bias:

- do not populate B-amplifier area (dashed line) except for:
- RB1 & RB2 & RB3: 0 Ω Resistor / solder bridge
- RB4 & CB2 form a lowpass to smooth the externally applied voltage. Populate with components of your liking (or choose CB2= 1uF MLCC 16V, RB4 = 10kΩ for a 16 Hz bandwidth)
- External bias can now be applied to J3-OUTB. The maximum voltage is defined by the voltage rating of CB2 but should never exceed 100 V due to sparking tendencies in low pressure atmospheres)

Grounding

Grounding connection of the enclosure will be established via the gold plated screw hole .

This screw hole can be connected to different potentials via the jumpers J4 and J5.

Without this connection a metallic enclosure will not properly shield the circuit (from experience).

Without Charge Pump (PS1):

- J4 = rauscharmes Spannungsteiler *GND* von A Verstärker wenn J6 offen / beiden Verstärkern wenn J6 verbunden ist
- J5 = gebuffertes Ground *GND50* (TLE2426 =IC3) das auch an den Ausgängen mit den Shields verbunden ist.

Wenn die Ausgänge mit einem Oszi / Data Logger / etc. verbunden werden, dessen Shield Anschluss geerdet ist, ist das Problem der Masseschleifen zu beachten!

Wenn auch das Platinengehäuße geerdet ist liegt *GND50* (Shieldanschluss der Ausgänge) automatisch auf Gehäusepotential. Die Verbindung ist allerdings sehr lang (Platine -> Koax -> Oszi -> Steckdose -> Laborerdung -> Labortisch -> schirmendes Gehäuse) und kann daher Brummen, Rauschen und Schwingen induzieren. Es wird zusätzlich eine kurze Erdungsverbindung z.B. über das Schraubloch und J4 / J5 benötigt. Welche Erdung bessere Ergebnisse erzielt ist noch nicht klar, ausprobieren! Ein Kurzschluss von *GND50* und *GND* (Verbinden von J4 UND J5) ist kein Problem, es kann aber zu zusätzlichem Rauschen und Verzerrungen kommen. Das gilt immer sobald *GND* mit *GND50* verbunden wird, egal ob direkt oder über das Gehäuse und eine Erdschleife die bei den Output Shields endet.

Empfehlung: Isolierte Gehäuse mit GND verbinden (J4 verbinden)

Geerdete Gehäuse mit GND50 verbinden (J5 verbinden) -> Erdschleifen kurz, mit kleiner Fläche und stromlos halten durch optimierte Erdung des Oszis.

Mit Charge Pump:

Es existiert nur ein GND Potential, dieses kann über J4 und / oder J5 mit dem Gehäuse verbunden werden.

Empfehlung: Gehäuse mit GND50 verbinden (J4 verbinden, J5 verbinden)

Wenn das Gehäuse geerdet ist: Erdschleifen kurz, mit kleiner Fläche und stromlos halten durch optimierte Erdung des Oszis.

Ein- und Ausgänge: Ratings

Eingänge / Ausgänge von links nach rechts:

1. Ausgang Verstärker A, Innenleiter Signal, Außenleiter GND50 (Erdung)

2. Stromversorgung, Außenleiter standardmäßig (PS1) -2,5 V, Innenleiter +2,5V Alternativ (PS2): Außenleiter Erdung, Innenleiter 3,3 V
3. Ausgang Verstärker B (Innen / Außen wie A) oder Bias Signal: Außenleiter GND50 (Erdung), Innenleiter Biasspannung

Ratings:

- Betriebsspannung ohne Charge Pump: min 4 V – max 5,25 V (5V recommended)
- Betriebsspannung mit Charge Pump: min – max V -> V max kann im Vakuum zu thermischer Überlast führen.
- Biasspannung Eingang: wenn anstatt von Verstärker B konfiguriert: Max Rating von CB2 oder max 100V
- Elektroden: Eingangsratings des LTC6268-10 kommen zur Anwendung:
    - „The inputs are protected by two series connected ESD protection
  diodes to each power supply. The input current should be limited to less
  than 1mA. The input voltage should not exceed 200mV beyond [above or below] the power supply. “
    - “To prevent breakdown of internal devices in the input stage, the two op amp inputs should NOT be separated by more than 2.0V. To help protect the input stage, internal circuitry will engage automatically if the inputs are separated by >2.0V and input currents will begin to flow. In all cases, care should be taken so that these currents remain less than 1mA. Additionally, if only one input is driven, internal circuitry will prevent any breakdown condition under transient conditions. The worst-case differential input voltage usually occurs when the +input is driven and the output is accidentally shorted to ground while in a unity gain configuration.” Die Eingänge können im Fall eines gesättigten Ausganges um mehr als 2 V separiert werden. Die Photoströme sind üblicherweise << 1mA und daher kein Problem, andere Ströme sollten aber unbedingt vermieden werden.
- Stromaufnahme:
  Stromanforderungen an den Ausgängen + Ruhestrom:
    - 1 Verstärker, keine Charge Pump: (26 - 35) mA
    - 1 Verstärker, Charge Pump @ 5 V Input:
    - 1 Verstärker, Charge Pump @ 3 V Input:
    - 2 Verstärker, Charge Pump @ 5 V Input:
    - 2 Verstärker, keine Charge Pump: ~64mA ?
- Ausgangscharakteristik:
    - Max. Ausgangsspannung: $\pm \frac{U_{Betrieb}}{2}$
    - Max. Verzerrungsfreie Ausgangsspannung: $\pm \frac{U_{Betrieb}}{2} - 0.5\ V$
    - Max. Ausgangsstrom:
        - 10 mA (Verzerrungsfrei)
        - 50 mA (Reduzierte Verzerrungsfreie Ausgangsspannung)
        - 80 mA(Kurzschluss ohne Charge Pump – ohne Kühlung nur Kurzzeitig erlaubt)
        - 150 mA (Kurzschluss mit Charge Pump – ohne Kühlung nur Kurzzeitig erlaubt)
    - Empfohlener Abschlusswiderstand: >= 1 kΩ
    - Max Kapazität am Ausgang: ~100 pF, abhängig vom Abschlusswiderstand

Bauteilempfehlungen

Metallfilmwiderstände haben minimales thermisches Rauschen aller erhältlicher SMD-Widerstandsarten. Weil Metallfilmwiderstände jedoch nicht in jeder Größe erhältlich sind, muss man manchmal zu Dünnfilmwiderständen greifen. Diese sind besser als Dickfilmwiderstände. Auf alle 1206 Footprints passen auch 0805 Widerstände. Eine Ausnahme bilden dabei RA1 und RB1, hier muss bei der Montage von 0805 besonders Acht gegeben werden den darunter liegenden Erdungsstreifen nicht zu kontaktieren. 0805 könnte an dieser Position zu erhöhter parasitärer Kapazität und damit kleinerer Bandbreite führen, genau Testergebnisse liegen jedoch nicht vor. Mehr dazu im LTC6268-10 Datasheet und im Demo Manual alias Guideline von LTC.

Alle Kondensatoren im Signalpfad sollten Keramikkondensatoren mit dem Dielektrikum NP0 / C0G sein und ein Spannungsrating >> 10V aufweisen. Kondensatoren auf den Supply Lines sollten möglichst niederohmig sein, dafür sind jeweils Paare aus kleinen Keramikkondensatoren (10 nF, 100 nF) und großen Tantal Elektrolyt Kondensatoren vorgesehen (1 µF, 2.2 µF, 10 µF). Hierbei können alle 2.2 µF Kondensatoren immer auch mit 10 µF bestückt werden.

Die Kondensatoren der Charge Pump (SP2) müssen eigene Kriterien erfüllen Keramik MLCC X7R mit niedrigem ESR werden im Datenblatt des LM27762 empfohlen.

Der für PS1 benötigte Rail-Splitter IC TLE2426 hat während des Projekts den End-Of-Life Status erreicht und ist nur noch für begrenzte Zeit erhältlich. Ein Vorrat von 10 Stück (Feb. 2024) befindet sich im Büro von Daniel Hipp.

Update Dec. 2024: TLE2426 has status active on Ti product page and is still readily available.

Jumper Netze

Netznamen: PWR+ …Innenleiter des C2-PWR Eingangs, PWR-….Außenleiter des C“-PWR Eingangs, V+…Positive Spannungsversorgung für Schaltung / ICs, V-…Negative Spannungsversorgung der Schaltung / ICs, GND 50….Außenleiter der Ausgänge(wird bei PS1 von TLE2426 erzeugt), GND Amp.A / Amp. B …. GND um den jeweiligen Verstärker, normalerweise durch Spannungsteiler erzeugt

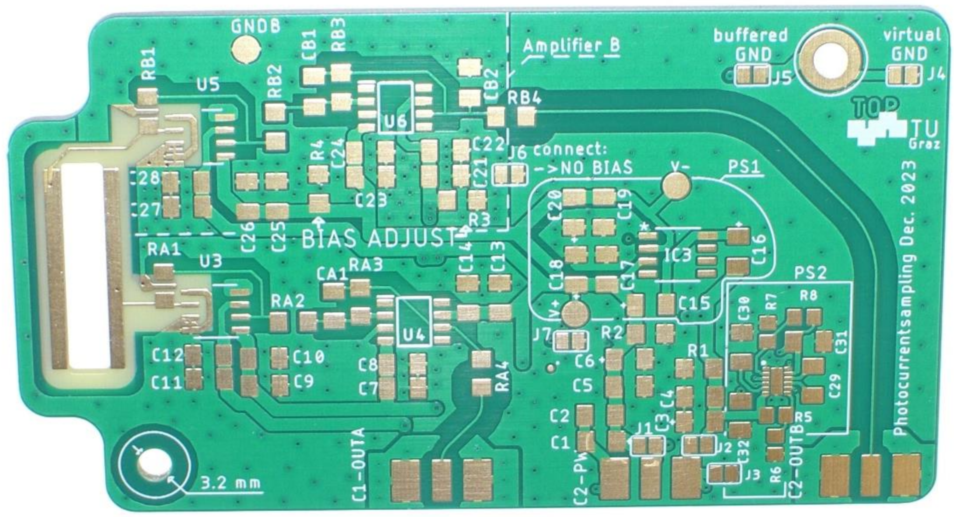
- J1: verbindet PWR+ mit V+
- J2: verbindet PWR- und V-
- J3: verbindet PWR- und GND Amp. A
- J4: verbindet Schraubloch mit GND von Amp. A (Spannungsteiler-GND)
- J5: verbindet Schraubloch mit GND 50 (von TLE2426 wenn PS1)
- J6: verbindet GND von Amp. A mit GND von Amp. B
- J7: verbindet GND von Amp. A mit GND 50

Cleaning

Bevor using the PCB in a vacuum environment, cleaning of the flux residues from soldering is necessary to prevent outgassing. Well suited for this task is the PCB cleaner “FLU, FLUXCLENE, FLU400DB” manufactured by Electrolube, which is a solvent spray can with an attached brush to loosen the residue. This rough cleaning should be followed by an ultrasonic cleaning bath in isopropyl alcohol, in order to clean under the chips and other components. After the bath the isopropyl alcohol should be allowed enough time to evaporate bevor putting the PCB in a vacuum. Otherwise boiling of the isopropyl alcohol that may be solved in the polymer casings could cause cracks in the components.

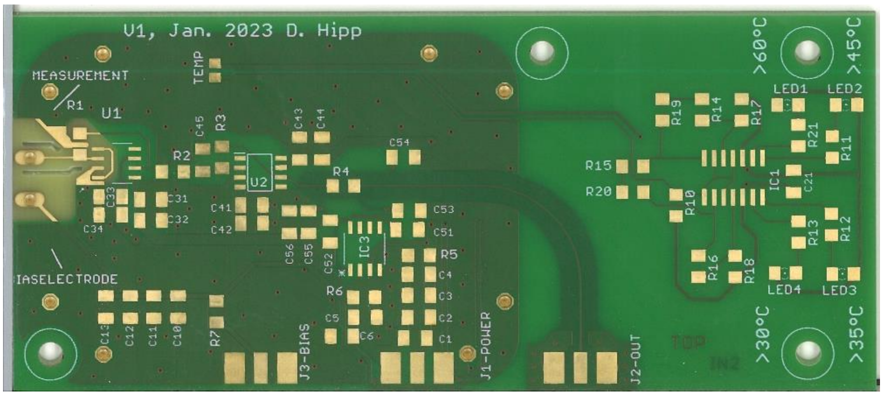
Version Identification

The PCB discussed in this document is labelled „Photocurrentsampling Dec. 2023“and is displayed in the following figure:



Die verschiedenen Bestückungsversionen lassen sich anhand der Jumper bzw. der Bestückung unterscheiden. PS1 oder PS2 ist an den entsprechend markierten Bereichen zu erkennen. Ob Amplifier B oder Bias ausgestattet ist, ist im strichlierten Bereich links oben zu erkennen. Wenn nur RB1 – RB4 und CB2 bestückt, dann ist es eine Platine mit externem Bias. Wenn dort auch ICs bestückt sind, ist ein Verstärker B verbaut.

An older version of the PCB, which is functionally identical to a configuration with PS1 and external bias voltage on electrode B is labelled: „V1, Jan. 2023 D. Hipp“. This older version is documented in the bachelor thesis XXXXXXX. The following image shows this version:



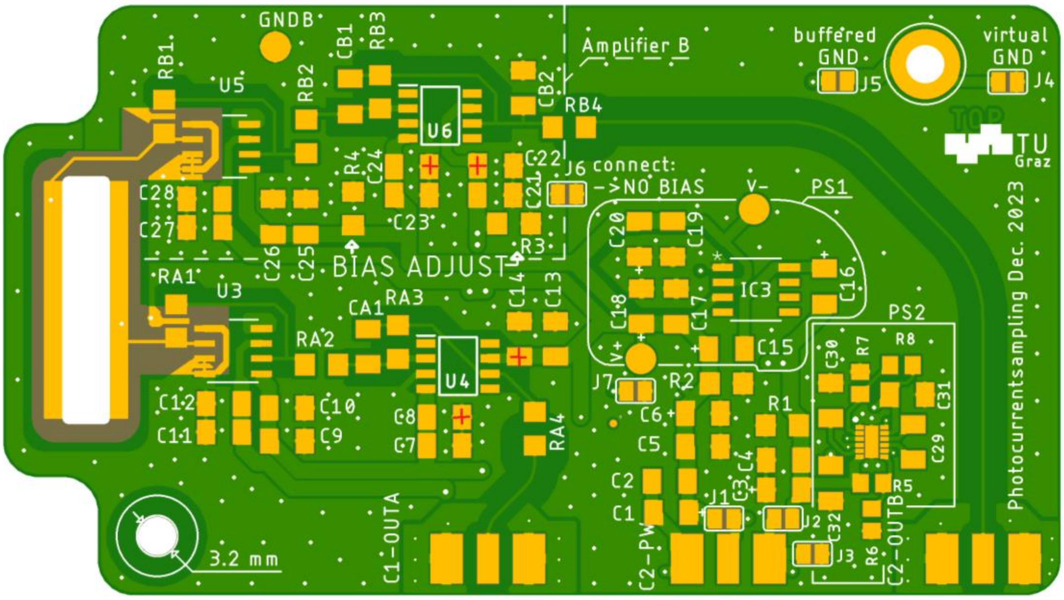
Both screw holes are on the same positions as in the Version Dec. 2023.

PCB assembly

Populate the PCB according to the configuration you have chosen. The components are listed in the bill of materials: “BOM_Photocurrentsampling_Double.xlsx”

Sheet metal electrodes can be soldered to the input electrodes. Keep in mind that the material can affect the measurement with its work function and a possibly insulating oxide layer.

Some of the 10 µF capacitors are missing the polarity marking (+) on the PCB silkscreen. The polarity of those is marked in the following picture:



ToDo:

- Bilder, bestückt,
- Schaltplan!!!