



PRIYANK KHANDELWAL

Course : M.E., Embedded Systems, 2027
 Email : h20212450@pilani.bits-pilani.ac.in
 Mobile : 8619739122
 CGPA : 8.95



ACADEMIC DETAILS

COURSE	SPECIALIZATION	INSTITUTE/COLLEGE	BOARD/UNIVERSITY	SCORE	YEAR
UG	Electrical & Electronics Engineering	BITS Pilani	BITS Pilani	7.44 CGPA	2025
CLASS XII		Bright India Public School	CBSE	84.4 %	2021
CLASS X		St. Anselms Sr Sec School	CBSE	94 %	2019

Subjects / Electives	Digital and Analog VLSI Design, Digital Electronics, Processor Design, Computer Architecture and Design, CAD for ICs, Embedded Systems Design, Reconfigurable Computing, Software for Embedded Systems, Machine Learning in Electronics, Analog Electronics, Microelectronics Circuits, Microprocessors And Interfacing, Computer Programming, Real Time Systems, Power Electronics, Electronic Devices, Control Systems, Signals and Communication Systems
Technical Proficiency	Verilog, Vivado - Xilinx, Zedboard development board, Cadence-Virtuoso, Embedded C, Keil uVision, STM32, LPC2378, Assembly Language, C Programming, Python, Simulink, MATLAB, PSpice, Arduino, Autocad 2D

WORK EXPERIENCE : <https://drive.google.com/file/d/1MUbb2ZFrLnULi-o6LpMWRZXI469r5dbe/view?usp=sharing>

Electronics Hardware Intern, SEDEMAC Mechatronics Limited	Jan 2025 - Jun 2025
<ul style="list-style-type: none"> Studied and analyzed various isolated DC-DC converter topologies for low-power applications with high-voltage input sources. Designed and simulated a dual-output regulated at 12V and 20V Flyback converter (2x6W from 400V DC) in DCM; investigated and reduced cross-regulation effects from 30 to 2.1% through load regulation and leakage modeling. 	
Design Engineering Intern, Pyrotech Electronics	
<ul style="list-style-type: none"> Designed a control system for an EV Battery Management System(BMS) and developed a fast charging algorithm that reduces charging time by approximately 25% Implemented an Electronic Charge Balance System to maintain State of Charge (SoC) of <3% across 4-cell Li-ion battery packs, through a capacitive switching network in MATLAB simulations. 	

PROJECTS : Link to my Self-designed Portfolio Website :

<https://hipsterenova.github.io/my-portfolio/>

High-Speed 8x8 modified Booth Multiplier (Modulo 255) Cadence-Virtuoso Vivado - Digital VLSI Design	Nov 2025 - Dec 2025
<ul style="list-style-type: none"> Architected an 8x8 Modified Booth Multiplier featuring a 4-unit pipeline (Encoder, PPG, Adder Tree, Modulo 255); reduced latency by 53% with a 3,147 transistor count compared to baseline array designs. Mastered the end-to-end RTL-to-VLSI flow including schematic-level verification and hardware optimization 	
MIPS-like Architecture 32-bit Processor - Computer Architecture	
<ul style="list-style-type: none"> Designed and Implemented Single cycle 32-bit MIPS like processor in Xilinx Vivado using Verilog HDL. Further implemented full fledged 5 stage Pipelined processor(RISC-V) capable of resolving the Data Hazards in minimum CPI possible along with J-type instructions. https://github.com/hipsterenova/Computer_Architecture_project 	
Medicine Dispenser Using LPC2378 Microcontroller - Embedded Systems Design	
<p>Designed and implemented an embedded system-based medicine dispenser with a stepper motor, LPC2378 development board, LCD screen, buzzer, and keyboard for user interface and control and programmed in Keil4 environment using Embedded C</p> <p>https://github.com/hipsterenova/embedded_project/tree/main</p>	
AI-Powered Library Silence Monitoring System - Machine Learning	
<p>Engineered a real-time, multimodal surveillance system integrating two custom CNN models: a Visual Speech Detector (using MediaPipe Face Mesh for ROI localization and motion-based temporal smoothing) and an Audio Voice Activity Detector (VAD) (analyzing Mel Spectrograms). Developed a cascading vision pipeline that reduced false positives (e.g., yawning) by 90% and implemented a multi-face tracking algorithm to identify active speakers in crowded environments with high precision.</p>	
FPGA Morse Code Decoder - Reconfigurable Computing	
<ul style="list-style-type: none"> Engineered a Verilog-based system on a ZedBoard Zynq 7000 FPGA to translate manual pushbutton inputs into alphanumeric text. Implemented digital debouncing filters, a multi-state FSM for pattern decoding, and a custom SPI driver to control a Pmod OLED display. 	
Fan Speed Control and Sensing System - Microprocessor and Hardware Integration	
<ul style="list-style-type: none"> Designed and executed a beginner-level project in microprocessor interfacing integrating components such as 8086 microprocessor, keyboard, PC817 optocoupler, LM2907, 8284, 8255, and 8254, TRiac(BT136B), 7447, 7Segment display, Lidar sensor, ROM(2716), RAM(6116), ADC(0808) <p>https://drive.google.com/drive/folders/1b5ENbjrUxOKXrmV2LRAGmty1AFoZGiDQ?usp=drive_link</p>	

AWARDS AND RECOGNITIONS

Secured 2 DREAM OFFERS Placement Unit	Oct 2024
Only Student in the Batch of 2021-25 to receive 2 DREAM Offers in Undergraduate OnCampus Placement Drive 2024 both in Core electronics	
Winner of 2023 Electronics Design Competition EEE Department K.K. Birla Goa Campus	
Winner of 2023 EEE Department Design Competition held at BITS Pilani KK Birla Goa Campus conducted on open day	

