SSD1331

Advance Information

96RGB x 64 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.



CONTENTS

COI	NTENTS		2
1	GERI	ENAL INFORMATION	6
2	FEAT	TURES	6
3	ORD	ERING INFORMATION	6
4	_	CK DIAGRAM	_
5		1331Z GOLD BUMP DIE PAD ASSIGNMENT	
6		DESCRIPTION	
		CTIONAL BLOCK DESCRIPTIONS	
7 7.		U Interface Selection	
7.	7.1.1	6800-series Parallel Interface	
	7.1.1	8080-series Parallel Interface	
	7.1.3	Serial Interface	
7.	-	MMAND DECODER	
7.	3 Osc	CILLATOR CIRCUIT AND DISPLAY TIME GENERATOR	18
	7.3.1	Oscillator	18
	7.3.2	FR synchronization	
7.		SET CIRCUIT	
7.		APHIC DISPLAY DATA RAM (GDDRAM)	
	7.5.1	GDDRAM structure	
	7.5.2	Data bus to RAM mapping under different input mode	
7.	7.5.3	RAM mapping and Different color depth mode	
7. 7.		G / COM DRIVING BLOCK	
7. 7.		MMON AND SEGMENT DRIVERS	
7.		WER ON AND OFF SEQUENCE	
8		MAND TABLE	
8.	1 DA	ra Read / Write	34
9		MAND DESCRIPTIONS	
9.		NDAMENTAL COMMAND	
	9.1.1	Set Column Address (15h)	
	9.1.2	Set Row Address (75h)	
	9.1.3	Set Contrast for Color A, B, C (81h, 82h, 83h)	
	9.1.4	Master Current Control (87h)	
	9.1.5	Set Second Pre-charge Speed for Color A, B, C (8Ah)	37
	9.1.6	Set Re-map & Data Format (A0h)	
	9.1.7	Set Display Start Line (A1h)	
	9.1.8	Set Display Offset (A2h)	
	9.1.9	Set Display Mode (A4h ~ A7h)	
	9.1.10	Set Multiplex Ratio (A8h)	
	9.1.11 9.1.12	Dim mode setting (ABh)	
	9.1.12	Set Display On/Off (ACh / AEh / AFh)	
	9.1.14	Power Save Mode (B0h)	
	9.1.15	Phase 1 and 2 Period Adjustment (B1h)	
	9.1.16	Set Display Clock Divide Ratio/ Oscillator Frequency (B3h)	
	9.1.17	Set Gray Scale Table (B8h)	
	9.1.18	Enable Linear Gray Scale Table (B9h)	
	9.1.19	Set Pre-charge voltage (BBh)	47
	9.1.20	Set V _{COMH} Voltage (BEh)	
	9.1.21	NOP (BCh, BDh, E3h)	
	9.1.22	Set Command Lock (FDh)	47
9.		APHIC ACCELERATION COMMAND SET DESCRIPTION	
	9.2.1	Draw Line (21h)	
	9.2.2	Draw Rectangle (22h)	4ŏ

	9.2.3	Copy (23h)	49
	9.2.4	Dim Window (24h)	49
	9.2.5	Clear Window (25h)	
	9.2.6	Fill Enable/Disable (26h)	
	9.2.7	Continuous Horizontal & Vertical Scrolling Setup (27h)	51
	9.2.8	Deactivate scrolling (2Eh)	
	9.2.9	Activate scrolling (2Fh)	51
10	MA	KIMUM RATINGS	52
11	DC	CHARACTERISTICS	EO
11	DC	UNAKAUTEKISTIUS	მა
12	AC	CHARACTERISTICS	54
13	ΔРΕ	PLICATION EXAMPLE	58
10			
14		CKAGE OPTIONS	
	14.1	SSD1331Z DIE TRAY INFORMATION	59
•	14.2	SSD1331U1R1 COF PACKAGE DIMENSIONS	60
•		SSD1331U1R1 COF PACKAGE PIN ASSIGNMENT	
•	14.4	SSD1331U3R1 COF PACKAGE DIMENSIONS	64
•		SSD1331U3R1 COF PACKAGE PIN ASSIGNMENT	

SSD1331 Rev 1.0 P 3/68 Jul 2006 **Solomon Systech**

TABLES

Table 1 - Ordering Information	6
Table 2 - SSD1331Z Die Pad Coordinates	9
Table 3 - Bus Interface selection	12
Table 4 - MCU interface assignment under different bus interface mode	15
Table 5 - Control pins of 6800 interface	15
Table 6 - Control pins of 8080 interface (Form 1)	16
Table 7 - Control pins of 8080 interface (Form 2)	16
Table 8 - Control pins of Serial interface	17
Table 9 - Data bus usage under different bus width and color depth mode	20
Table 10 - Command Table	
Table 11 - Address increment table (Automatic)	34
Table 12 - Illustration of different COM output settings	39
Table 13 - Example of Set Display Offset and Display Start Line with no Remap	43
Table 14 - Example of Set Display Offset and Display Start Line with Remap	
Table 15 - Result of Change of Brightness by Dim Window Command	49
Table 16 - Maximum Ratings	52
Table 17 - DC Characteristics	53
Table 18 - AC Characteristics	
Table 19 - 6800-Series MPU Parallel Interface Timing Characteristics	55
Table 20 - 8080-Series MPU Parallel Interface Timing Characteristics	56
Table 21 - Serial Interface Timing Characteristics	57
Table 22 - SSD1331U1R1 pin assignment	
Table 23 - SSD1331U3R1 pin assignment	67

 Solomon Systech
 Jul 2006
 P 4/68
 Rev 1.0
 SSD1331

FIGURES

Figure 1 - SSD1331 Block Diagram	7
Figure 2 - SSD1331Z Die Drawing	8
Figure 3 - SSD1331Z Alignment mark dimensions	11
Figure 4 - Display data read back procedure - insertion of dummy read	
Figure 5 – Example of Write procedure in 8080 parallel interface mode	
Figure 6 – Example of Read procedure in 8080 parallel interface mode	
Figure 7 - Display data read back procedure - insertion of dummy read	
Figure 8 - Write procedure in SPI mode	
Figure 9 - Oscillator Circuit	
Figure 10 - 65k Color Depth Graphic Display Data RAM Structure	
Figure 11 - 256-color mode mapping	
Figure 12 - Relation between GDRAM content and gray scale table entry for three colors in 65K co	
Figure 13 - Illustration of relation between graphic display RAM value and gray scale control	
Figure 14 - I _{REF} Current Setting by Resistor Value	
Figure 15 - I _{SEG} current vs V _{CC} setting at constant I _{REF} , Contrast = FFh	
Figure 16 - Segment and Common Driver Block Diagram	
Figure 17 - Segment and Common Driver Signal Waveform	
Figure 18 - Gray Scale Control by PWM in Segment	
Figure 19 : The Power ON sequence	
Figure 20 : The Power OFF sequence	
Figure 21 - Example of Column and Row Address Pointer Movement	35
Figure 22 - Segment Output Current for Different Contrast Control and Master Current Setting	36
Figure 23 - Effect of setting the second pre-charge under different speeds	
Figure 24 - Address Pointer Movement of Horizontal Address Increment Mode	
Figure 25 - Address Pointer Movement of Vertical Address Increment Mode	
Figure 26 - Example of Column Address Mapping	
Figure 27 - COM Pins Hardware Configuration (MUX ratio: 64)	
Figure 28 – Transition between different modes	
Figure 29 - Typical Oscillator frequency adjustment by B3 command (V _{DD} =2.7V)	
Figure 30 - Example of gamma correction by gray scale table setting	
Figure 31 – Typical Pre-charge voltage level setting by command BBh	47
Figure 32 - Example of Draw Line Command	
Figure 33 - Example of Draw Rectangle Command	
Figure 34 - Example of Copy Command	
Figure 35 - Example of Copy + Clear = Move Command	
Figure 36 - Examples of Continuous Horizontal and Vertical Scrolling command setup	
Figure 37 - 6800-series parallel interface characteristics	
Figure 38 - 8080-series parallel interface characteristics (Form 1)	
Figure 39 - 8080-series parallel interface characteristics (Form 2)	
Figure 40 - Serial interface characteristics	
Figure 41 - Application Example for SSD1331U1R1	
Figure 42 - Die Tray Information	
Figure 43 - SSD1331U1R1 outline drawing	
Figure 44 - SSD1331U1R1 pin assignment drawing	
Figure 45 - SSD1331U3R1 outline drawing	
Figure 46 - SSD1331U3R1 pin assignment drawing	66
g	

SSD1331 Rev 1.0 P 5/68 Jul 2006 **Solomon Systech**

1 GERENAL INFORMATION

The SSD1331 is a single chip CMOS OLED/PLED driver with 288 segments and 64 commons output, supporting up to $96RGB \times 64$ dot matrix display. This chip is designed for Common Cathode type OLED/PLED panel.

The SSD1331 had embedded Graphic Display Data RAM (GDDRAM). It supports with 8, 9, 16 bits 8080 / 6800 parallel interface as well as serial peripheral interface. It has 256-step contrast and 65K color control. To facilitate communication between lower operating voltages MCU, it has separate power for I/O interface logic. SSD1331 is suitable for mobile phones, MP3, MP4 and other industrial devices.

2 FEATURES

- Resolution: 96RGB x 64 dot matrix panel
- 65k color depth support by embedded 96x64x16 bit GDDRAM display buffer
- Power supply:
 - \circ V_{DD} = 2.4V to 3.5V for IC logic
 - \circ V_{CC} = 8.0V to 18.0V for Panel driving
 - \circ V_{DDIO} = 1.6V to V_{DD} for MCU interface
- Segment maximum source current: 200uA
- Common maximum sink current: 60mA
- 256 step contrast control for the each color component plus 16 step master current control
- Pin selectable MCU interface
 - o 8/9/16 bits 6800-series parallel Interface
 - o 8/9/16 bits 8080-series Parallel Interface
 - o Serial Peripheral Interface
- Color swapping function (RGB <-> BGR)
- Graphic Accelerating Command (GAC) set with Continuous Horizontal, Vertical and Diagonal Scrolling
- Programmable Frame Rate
- Wide range of operating temperature: -40 to 85 °C

3 ORDERING INFORMATION

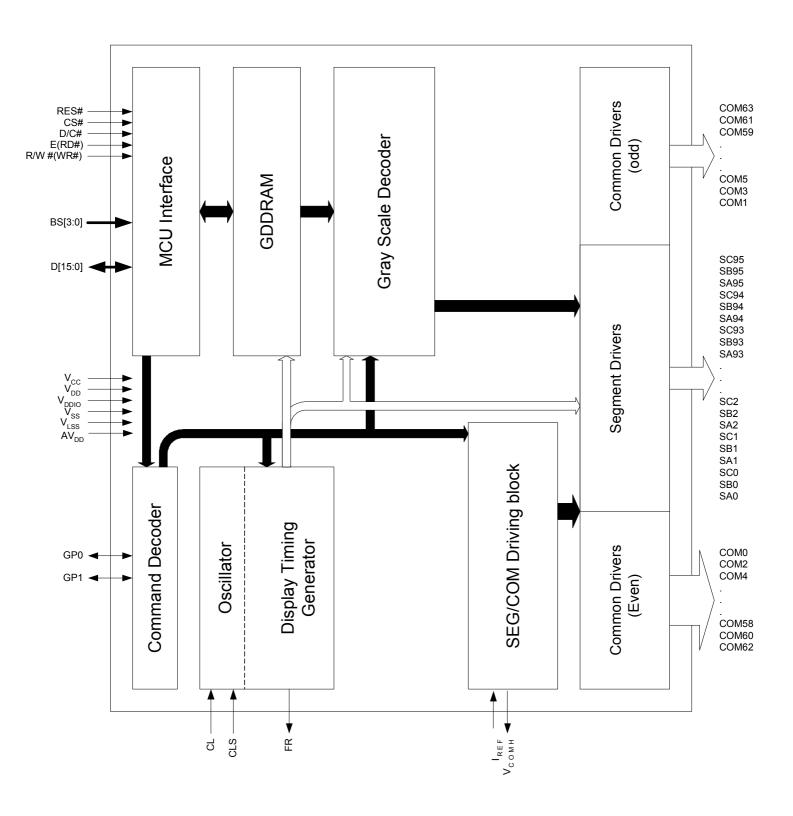
Table 1 - Ordering Information

Ordering Part Number	SEG	СОМ	Package Form	Reference	Remark
SSD1331Z	96x3	64	COG	Page 8, 59	-
SSD1331U1R1	96x3	64	COF	Page 60	 35mm film, 5 sprocket hole 8 bit or SPI interface Output lead pitch: 0.06mm for SEG, 0.09mm for COM
SSD1331U3R1	96x3	64	COF	Page 64	 35mm film, 4 sprocket hole 8 bit or SPI interface Output lead pitch: 0.06mm for SEG, 0.09mm for COM

Solomon Systech Jul 2006 | P 6/68 | Rev 1.0 | SSD1331

4 BLOCK DIAGRAM

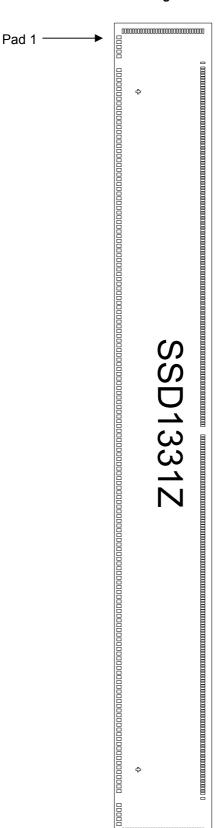
Figure 1 - SSD1331 Block Diagram



SSD1331 Rev 1.0 P 7/68 Jul 2006 **Solomon Systech**

5 SSD1331Z GOLD BUMP DIE PAD ASSIGNMENT

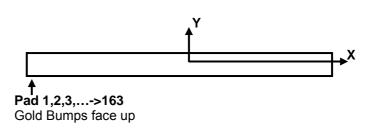
Figure 2 - SSD1331Z Die Drawing



Die size	13.1mm x 1.58mm	
Die height	457um	
Min I/O pad pitch	76.2 um	
Min SEG pad pitch	40.2 um	
Min COM pad pitch	41.8 um	
Bump height	Nominal 15um	

Bump size	
Pad 1-163	50um x 72um
Pad164-195, 486-517	72um x 28um
Pad 196-485	28um x 72um

	Alignment mark	
+ shape	(5446.0, -402.0)	75um x 75um
+ shape	(-5446.0, -402.0)	75um x 75um



 Solomon Systech
 Jul 2006
 P 8/68
 Rev 1.0
 SSD1331

Table 2 - SSD1331Z Die Pad Coordinates

Pad no.	Pad Name	X-Axis	Y-Axis
1	NC	-6319.4	-712.5
2	NC	-6243.2	-712.5
3	NC	-6167.0	-712.5
4	NC	-6090.8	-712.5
5	NC	-6014.6	-712.5
6	NC	-5791.2	-712.5
7	VCC	-5715.0	-712.5
8	VCC	-5638.8	-712.5
9	VCC	-5562.6	-712.5
10			-712.5
	VLSS	-5486.4	
11	VLSS	-5410.2	-712.5
12	VLSS	-5334.0	-712.5
13	VLSS	-5257.8	-712.5
14	VLSS	-5181.6	-712.5
15	VLSS	-5105.4	-712.5
16	VLSS	-5029.2	-712.5
17	VLSS	-4953.0	-712.5
18	VLSS	-4876.8	-712.5
19	VLSS	-4800.6	-712.5
20	VLSS	-4724.4	-712.5
21	VLSS	-4648.2	-712.5
22	VSS	-4572.0	-712.5
23	VSS	-4495.8	-712.5
24	VSS	-4419.6	-712.5
25	BGGND	-4343.4	-712.5
26	VDD	-4267.2	-712.5
27	VDD	-4191.0	-712.5
28	VDD	-4114.8	-712.5
29	VDDIO	-4038.6	-712.5
30	VDDIO		
		-3962.4	-712.5
31	VDDIO	-3886.2	-712.5
32	VCC	-3810.0	-712.5
33	VCC	-3733.8	-712.5
34	VCC	-3657.6	-712.5
35	VSSB	-3581.4	-712.5
36	VSSB	-3505.2	-712.5
37	VSSB	-3429.0	-712.5
38	GDR	-3352.8	-712.5
39	GDR	-3276.6	-712.5
40	GDR	-3200.4	-712.5
41			
	GDR	-3124.2	-712.5
42	GDR	-3048.0	-712.5
43	GDR	-2971.8	-712.5
44	GDR	-2895.6	-712.5
45	VDDB	-2819.4	-712.5
46	VDDB	-2743.2	-712.5
47	VDDB	-2667.0	-712.5
48	VDDB	-2590.8	-712.5
49	VDDB	-2514.6	-712.5
50	VDD	-2438.4	-712.5
51	VDDIO	-2362.2	-712.5
52	VDDIO		-7 12.5 -712.5
		-2286.0	
53	VDD	-2209.8	-712.5
54	FB	-2133.6	-712.5
55	VBREF	-2057.4	-712.5
56	VSS	-1981.2	-712.5
57	GP0	-1905.0	-712.5
58	GP1	-1828.8	-712.5
59	VDDIO	-1752.6	-712.5
60	VCIR	-1676.4	-712.5
61	VCIR	-1600.2	-712.5
62	VCIR	-1524.0	-712.5
63	VCIR	-1447.8	-7 L.5
64	VCIR	-1371.6	-7 L.5 -712.5
	VOR		
65		-1295.4	-712.5
66	VDD	-1219.2	-712.5
67	VDD	-1143.0	-712.5
68	VDD	-1066.8	-712.5
69	AVDD	-990.6	-712.5
70	AVDD	-914.4	-712.5
71	VDDIO	-838.2	-712.5
72	VDDIO	-762.0	-712.5
73	VDDIO	-685.8	-712.5
74	VDDIO	-609.6	-7 L.5 -712.5
75	VDDIO	-533.4	-712.5
76	VDDIO	-457.2	-712.5
77	BS0	-381.0	-712.5
78	VSS	-304.8	-712.5
79	BS1	-228.6	-712.5

Pad no. Pad Name X-Axis BS BS2 7-62 7-72.5	es			
81	Pad no.	Pad Name	X-A xis	Y-A xis
83 BS3 76.2 -72.5 84 VDDIO 152.4 -72.5 85 VDDIO 228.6 -72.5 86 IREF 304.8 -72.5 87 VCC 3810 -72.5 88 VCC 457.2 -72.5 89 VCC 457.2 -72.5 89 VCC 533.4 -72.5 90 FR 609.6 -72.5 91 CL 685.8 -72.5 91 CL 685.8 -72.5 92 VSS 762.0 -72.5 93 CLS 838.2 -72.5 94 VDDIO 914.4 -72.5 95 VDDIO 990.6 -72.5 96 VDDIO 990.6 -72.5 97 VDDIO 143.0 -72.5 98 CSB 129.2 -72.5 99 VSS 1296.4 -72.5 100 RESB 13716 -72.5 101 VDDIO 1447.8 -72.5 102 VDDIO 152.4 -72.5 103 DC 1800.2 -72.5 104 VSS 166.4 -72.5 105 RW 1752.6 -72.5 106 E 1828.8 -72.5 107 VDDIO 1905.0 -72.5 108 VDD 19812 -72.5 109 VDD 2057.4 -72.5 109 VDD 2133.6 -72.5 110 VDD 2133.6 -72.5 111 DO 2209.8 -72.5 112 D1 2286.0 -72.5 113 D2 2362.2 -72.5 114 D3 2438.4 -72.5 115 D4 258.6 -72.5 116 D4 259.6 -72.5 117 D6 2667.0 -72.5 118 D7 2743.2 -72.5 119 D8 289.4 -72.5 110 TD 29718 -72.5 111 D9 29718 -72.5 112 D1 2286.0 -72.5 113 D2 2362.2 -72.5 114 D3 2438.4 -72.5 115 D4 259.8 -72.5 116 D5 2590.8 -72.5 117 D6 2667.0 -72.5 118 D7 2743.2 -72.5 119 D8 289.4 -72.5 110 TD 29718 -72.5 111 D0 29718 -72.5 112 D1 2286.0 -72.5 113 D2 2362.2 -72.5 114 D3 2438.4 -72.5 115 D4 2514.6 -72.5 116 D4 2514.6 -72.5 117 D6 2667.0 -72.5 118 D7 2743.2 -72.5 119 D8 2895.6 -72.5 120 D9 2895.6 -72.5 121 D10 29718 -72.5 122 D11 3048.0 -72.5 123 D12 3124.2 -72.5 124 D13 3200.4 -72.5 125 D14 3276.6 -72.5 126 D15 3352.8 -72.5 127 VSS 3429.0 -72.5 128 TR11 3505.2 -72.5 139 TR1 3434.4 -72.5 130 TR8 3733.8 -72.5 131 TR8 3733.8 -72.5 132 TR7 3810.0 -72.5 134 VSS 3962.4 -72.5 135 TR6 386.2 -72.5 136 VCOMH 4572.0 -72.5 137 VSDIO 486.8 -72.5 144 VSS 3962.4 -72.5 145 VCOMH 4572.0 -72.5 155 NC 5638.8 -72.5 156 VCS 5838.9 -72.5 157 VLSS 5750.0 -72.5 158 NC 5751.2 -72.5 159 NC 6048.6 -72.5				
84 VDDIO	_			
85 VDDIO 228.6 -72.5 86 IREF 304.8 -72.5 87 VCC 3810 -72.5 88 VCC 457.2 -72.5 89 VCC 533.4 -72.5 90 FR 609.6 -72.5 91 CL 685.8 -72.5 92 VSS 762.0 -72.5 93 CLS 838.2 -72.5 94 VDDIO 914.4 -72.5 95 VDDIO 990.6 -72.5 96 VDDIO 143.0 -72.5 97 VDDIO 143.0 -72.5 98 CSB 279.2 -72.5 99 VSS 295.4 -72.5 99 VSS 295.4 -72.5 100 RESB 3716 -72.5 101 VDDIO 1447.8 -72.5 102 VDDIO 1524.0 -72.5 103 DC 1500.2 -72.5 104 VSS 1576.4 -72.5 105 RW 1752.6 -72.5 106 E 1828.8 -72.5 107 VDDIO 1905.0 -72.5 108 VDD 1981.2 -72.5 109 VDD 2057.4 -72.5 110 VDD 2133.6 -72.5 111 D0 2209.8 -72.5 112 D1 2286.0 -72.5 113 D2 2362.2 -72.5 114 D3 2438.4 -72.5 115 D4 2546 -72.5 116 D5 2590.8 -72.5 117 D6 2667.0 -72.5 118 D7 2743.2 -72.5 119 D8 2895.6 -72.5 120 D9 2895.6 -72.5 121 D10 29718 -72.5 122 D11 3048.0 -72.5 123 D2 3262.2 -72.5 134 D3 2438.4 -72.5 135 D4 2546 -72.5 136 D5 2590.8 -72.5 137 D6 2667.0 -72.5 138 D7 2743.2 -72.5 149 D8 2895.6 -72.5 150 D9 2895.6 -72.5 151 D1 29718 -72.5 152 D1 3048.0 -72.5 153 D7 3743.2 -72.5 154 D1 3291.8 -72.5 155 D14 3276.6 -72.5 156 D16 3352.8 -72.5 157 VSS 3429.0 -72.5 158 TRF 3686.2 -72.5 159 TRR 3690.4 -72.5 150 TRR 3690.4 -72.5 151 TRR 3733.8 -72.5 152 TRT 3690.0 -72.5 153 TRR 4038.6 -72.5 154 VCOMH 4572.0 -72.5 155 VCC 5346.4 -72.5 156 VCS 5363.8 -72.5 157 VLSS 575.0 -72.5 158 VCC 5363.8 -72.5 159 VC 5563.8 -72.5 150 VCC 5581.6 -72.5 151 VCC 5563.8 -72.5 152 VCC 5340.2 -72.5 153 VCC 5563.8 -72.5 154 VCC 5563.8 -72.5 155 VCS 5360.8 -72.5 156 VC				
87				
88				
89 VCC 533.4 -72.5 90 FR 609.6 -72.5 91 CL 685.8 -72.5 92 VSS 762.0 -72.5 93 CLS 838.2 -72.5 94 VDDIO 914.4 -72.5 95 VDDIO 990.6 -72.5 96 VDDIO 1943.0 -72.5 97 VDDIO 143.0 -72.5 98 CSB 129.2 -72.5 99 VSS 1295.4 -72.5 99 VSS 1295.4 -72.5 100 RESB 13716 -72.5 101 VDDIO 1447.8 -72.5 101 VDDIO 1524.0 -72.5 102 VDDIO 1524.0 -72.5 103 DC 1800.2 -72.5 104 VSS 1676.4 -72.5 105 RW 1752.6 -72.5 106 E 1828.8 -72.5 107 VDDIO 1905.0 -72.5 108 VDD 19812 -72.5 109 VDD 2057.4 -72.5 110 VDD 2057.4 -72.5 111 DO 2209.8 -72.5 112 D1 2286.0 -72.5 113 D2 2362.2 -72.5 114 D3 2438.4 -72.5 115 D4 254.6 -72.5 116 D5 2590.8 -72.5 117 D6 2667.0 -72.5 118 D7 2743.2 -72.5 119 D8 2819.4 -72.5 110 D9 29718 -72.5 111 D10 29718 -72.5 112 D1 2286.0 -72.5 113 D2 2362.2 -72.5 114 D3 2438.4 -72.5 115 D4 254.6 -72.5 116 D5 2590.8 -72.5 117 D6 2667.0 -72.5 118 D7 2743.2 -72.5 119 D8 2819.4 -72.5 120 D9 2895.6 -72.5 131 D7 2743.2 -72.5 132 D7 2743.2 -72.5 133 D7 2743.2 -72.5 134 D7 2743.2 -72.5 135 D7 3352.8 -72.5 136 TR 3352.8 -72.5 137 TR 3 300.0 -72.5 138 TR 3353.8 -72.5 139 TR 10 3581.4 -72.5 130 TR 9 3657.6 -72.5 131 TR 8 3733.8 -72.5 132 TR 7 3810.0 -72.5 133 TR 6 388.2 -72.5 134 VSS 3962.4 -72.5 135 TR 44910 -72.5 136 TR 4418.8 -72.5 137 TR 3 44910 -72.5 138 TR 6 348.8 -72.5 144 VSS 3962.4 -72.5 145 VSS 3962.4 -72.5 146 VSS 3962.4 -72.5 147 VSS 34495.8 -72.5 148 VSS 3962.4 -72.5 149 TR 0 3581.4 -72.5 150 TR 0 4849.6 -72.5 151 TR 0 4849.6 -72.5 152 TR 1 3505.2 -72.5 153 TR 1 34910 -72.5 154 VSS 3962.4 -72.5 155 TR 1 4940.0 -72.5 156 VCC 5161.6 -72.5 157 VLSS 575.0 -72.5 158 VCC 5164.6 -72.5 159 VCC 5166.6 -72.5 150 VCC 5166.6 -72.5 150 VCC 5166.6 -72.5 150 VCC 5166.6 -72.5 150 VCC 5166.6 -72.5				
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116 D5 2590.8 -72.5 117 D6 2667.0 -72.5 118 D7 2743.2 -72.5 119 D8 2849.4 -72.5 120 D9 2895.6 -72.5 121 D10 29718 -72.5 121 D10 29718 -72.5 122 D11 3048.0 -72.5 123 D12 3124.2 -72.5 124 D13 3200.4 -72.5 125 D14 3276.6 -72.5 126 D15 3352.8 -72.5 127 VSS 3429.0 -72.5 128 TR11 3505.2 -72.5 129 TR10 35814 -72.5 130 TR9 3657.6 -72.5 131 TR8 3733.8 -72.5 132 TR7 3810.0 -72.5 133 TR6 3886.2 -72.5 <td></td> <td></td> <td></td> <td></td>				
117 D6 2667.0 -72.5 118 D7 2743.2 -72.5 119 D8 2819.4 -72.5 120 D9 2895.6 -72.5 121 D10 29718 -72.5 121 D10 29718 -72.5 122 D11 3048.0 -72.5 123 D12 3124.2 -72.5 124 D13 3200.4 -72.5 125 D4 3276.6 -72.5 126 D16 3352.8 -72.5 126 D16 3352.8 -72.5 127 VSS 3429.0 -72.5 128 TR11 3505.2 -72.5 129 TR10 35814 -72.5 130 TR9 3657.6 -72.5 131 TR8 3733.8 -72.5 132 TR7 3810.0 -72.5 133 TR6 3886.2 -72.5 <td></td> <td></td> <td></td> <td></td>				
118 D7 2743.2 -72.5 119 D8 2819.4 -72.5 120 D9 2895.6 -72.5 120 D9 2895.6 -72.5 121 D10 29718 -72.5 122 D11 3048.0 -72.5 123 D12 3124.2 -72.5 124 D13 3200.4 -72.5 125 D14 3276.6 -72.5 126 D16 3352.8 -72.5 127 VSS 3429.0 -72.5 128 TR11 3505.2 -72.5 129 TR10 35814 -72.5 130 TR9 3667.6 -72.5 131 TR8 3733.8 -72.5 131 TR8 3733.8 -72.5 133 TR6 3886.2 -72.5 134 VSS 3962.4 -72.5 135 TR5 4038.6 -72.5 </td <td></td> <td></td> <td></td> <td></td>				
20 D9 2895.6 -712.5 121 D10 29718 -712.5 122 D11 3048.0 -712.5 123 D12 3124.2 -712.5 124 D13 3200.4 -712.5 125 D14 3276.6 -712.5 126 D15 3352.8 -712.5 126 D16 3352.8 -712.5 127 VSS 3429.0 -712.5 128 TR11 3505.2 -712.5 129 TR10 35814 -712.5 130 TR9 3657.6 -712.5 131 TR8 3733.8 -712.5 132 TR7 3810.0 -712.5 133 TR6 3886.2 -712.5 134 VSS 3962.4 -712.5 135 TR5 4038.6 -712.5 136 TR4 4114.8 -712.5 137 TR3 41910 <t< td=""><td>118</td><td>D7</td><td></td><td>-712.5</td></t<>	118	D7		-712.5
121 D 10 29718 -72.5 122 D 11 3048.0 -712.5 123 D 12 3124.2 -712.5 124 D 13 3200.4 -712.5 125 D 14 3276.6 -72.5 126 D 15 3352.8 -712.5 127 VSS 3429.0 -712.5 128 TR11 3505.2 -712.5 129 TR10 35814 -712.5 130 TR9 3657.6 -712.5 131 TR8 3733.8 -712.5 132 TR7 3810.0 -712.5 133 TR6 3886.2 -712.5 134 VSS 3962.4 -712.5 135 TR5 4038.6 -712.5 136 TR4 414.8 -712.5 137 TR3 41910 -712.5 138 TR2 4267.2 -712.5 140 TR0 4449.6				
T22 D11 3048.0 -772.5 T23 D12 3124.2 -772.5 T24 D13 3200.4 -772.5 T25 D14 3276.6 -772.5 T26 D16 3352.8 -72.5 T27 VSS 3429.0 -72.5 T27 VSS 3429.0 -72.5 T28 TR11 3505.2 -72.5 T29 TR10 3581.4 -72.5 T30 TR9 3657.6 -72.5 T31 TR8 3733.8 -72.5 T31 TR8 3733.8 -72.5 T31 TR8 386.2 -72.5 T33 TR6 3886.2 -72.5 T34 VSS 3962.4 -72.5 T35 TR5 4038.6 -72.5 T36 TR4 414.8 -72.5 T37 TR3 41910 -72.5 T38 TR2 4267.2 -72.5				
123 D 12 3124.2 -712.5 124 D 13 3200.4 -712.5 125 D 14 3276.6 -712.5 126 D 16 3352.8 -712.5 127 VSS 3429.0 -712.5 128 TR 11 3505.2 -712.5 129 TR 10 3581.4 -712.5 130 TR 9 3667.6 -712.5 131 TR 8 3733.8 -712.5 131 TR 8 3733.8 -712.5 131 TR 8 3733.8 -712.5 132 TR 7 3810.0 -712.5 133 TR 6 3886.2 -712.5 134 VSS 3962.4 -712.5 135 TR 5 4038.6 -712.5 136 TR 4 414.8 -712.5 137 TR 3 41910 -712.5 138 TR 2 4267.2 -712.5 139 TR 1 43				
25 D14 3276.6 -72.5 126 D16 3352.8 -72.5 127 VSS 3429.0 -72.5 128 TR11 3505.2 -72.5 129 TR10 35814 -72.5 130 TR9 3657.6 -712.5 131 TR8 3733.8 -712.5 131 TR8 3733.8 -712.5 132 TR7 3810.0 -72.5 133 TR6 3886.2 -712.5 134 VSS 3962.4 -72.5 134 VSS 3962.4 -72.5 136 TR4 414.8 -72.5 136 TR4 414.8 -72.5 137 TR3 410 -72.5 138 TR2 4267.2 -72.5 140 TR0 449.6 -72.5 141 VSS 4495.8 -72.5 142 VCOMH 4572.0 -72.5				
26 D 15 3352.8 -72.5 127 VSS 3429.0 -72.5 128 TR11 3505.2 -72.5 129 TR10 35814 -72.5 130 TR9 3657.6 -72.5 131 TR8 3733.8 -72.5 131 TR8 3733.8 -72.5 131 TR8 3733.8 -72.5 132 TR7 3810.0 -72.5 134 VSS 3962.4 -72.5 134 VSS 3962.4 -72.5 135 TR5 4038.6 -72.5 136 TR4 4148.8 -72.5 137 TR3 41910 -72.5 138 TR2 4267.2 -72.5 139 TR1 4343.4 -72.5 140 TR0 4449.6 -72.5 141 VSS 4495.8 -72.5 142 VCOMH 4572.0 -72.5	124	D13	3200.4	-712.5
127 VSS 3429.0 -712.5 128 TR11 3505.2 -712.5 129 TR10 35814 -712.5 130 TR9 3667.6 -712.5 131 TR8 3733.8 -712.5 132 TR7 3810.0 -712.5 133 TR6 3886.2 -712.5 134 VSS 3962.4 -712.5 135 TR5 4038.6 -712.5 136 TR4 4114.8 -712.5 137 TR3 41910 -712.5 138 TR2 4267.2 -712.5 139 TR1 4343.4 -712.5 140 TR0 4496.6 -712.5 141 VSS 4495.8 -712.5 143 VCOMH 4572.0 -712.5 144 VCOMH 4724.4 -712.5 144 VCOMH 4724.4 -712.5 147 VDDO 4876.8				
128 TR11 3505.2 -72.5 129 TR10 35814 -72.5 130 TR9 3657.6 -72.5 131 TR8 3733.8 -72.5 131 TR8 3733.8 -72.5 132 TR7 3810.0 -72.5 133 TR6 3886.2 -72.5 134 VSS 3962.4 -72.5 135 TR5 4038.6 -72.5 136 TR4 4118.8 -72.5 137 TR3 41910 -72.5 138 TR2 4267.2 -72.5 139 TR1 4343.4 -72.5 140 TR0 4419.6 -72.5 141 VSS 4495.8 -72.5 143 VCOMH 4572.0 -72.5 143 VCOMH 4724.4 -72.5 144 VCOMH 4724.4 -72.5 145 VDD 4876.8 -72.5 </td <td></td> <td></td> <td></td> <td></td>				
130				
131 TR8 3733.8 -72.5 132 TR7 3810.0 -72.5 133 TR6 3886.2 -72.5 134 VSS 3962.4 -72.5 135 TR5 4038.6 -72.5 136 TR4 4114.8 -72.5 137 TR3 41910 -72.5 138 TR2 4267.2 -72.5 139 TR1 4343.4 -72.5 140 TR0 449.6 -72.5 141 VSS 4495.8 -72.5 141 VSS 4495.8 -72.5 142 VCOMH 4572.0 -72.5 143 VCOMH 4724.4 -72.5 144 VCOMH 4724.4 -72.5 145 VDD 4876.8 -72.5 147 VDDIO 4953.0 -72.5 148 VDDIO 4953.0 -72.5 150 VCC 51816 -72.5<	129	TR10	3581.4	-712.5
132 TR7 3810.0 -712.5 133 TR6 3886.2 -712.5 134 VSS 3962.4 -712.5 135 TR5 4038.6 -712.5 136 TR4 4114.8 -712.5 137 TR3 41910 -712.5 138 TR2 4267.2 -712.5 139 TR1 4343.4 -712.5 140 TR0 4419.6 -712.5 141 VSS 4495.8 -712.5 141 VSS 4495.8 -712.5 142 VCOMH 4572.0 -712.5 143 VCOMH 4572.0 -712.5 144 VCOMH 4724.4 -712.5 145 VDD 4876.8 -712.5 146 VDD 4876.8 -712.5 147 VDDIO 4953.0 -712.5 148 VDDIO 5029.2 -712.5 149 VCC 51816				
133 TR6 3886.2 -712.5 134 VSS 3962.4 -712.5 135 TR5 4038.6 -712.5 136 TR4 414.8 -72.5 137 TR3 41910 -712.5 138 TR2 4267.2 -712.5 139 TR1 4343.4 -712.5 140 TR0 449.6 -72.5 141 VSS 4495.8 -72.5 142 VCOMH 4572.0 -72.5 143 VCOMH 4682.2 -72.5 144 VCOMH 4724.4 -72.5 145 VDD 4800.6 -72.5 146 VDD 4876.8 -72.5 147 VDDIO 4953.0 -72.5 148 VDDIO 5029.2 -72.5 149 VCC 51816 -72.5 150 VCC 51816 -72.5 151 VCC 5257.8 -7				
134 VSS 3962.4 -712.5 135 TR5 4038.6 -712.5 136 TR4 4114.8 -712.5 137 TR3 41910 -712.5 138 TR2 4267.2 -712.5 139 TR1 4343.4 -712.5 140 TR0 4449.6 -712.5 141 VSS 4495.8 -712.5 142 VCOMH 4572.0 -712.5 143 VCOMH 4648.2 -712.5 144 VCOMH 4724.4 -712.5 145 VDD 4800.6 -712.5 146 VDD 4876.8 -712.5 147 VDDIO 4953.0 -712.5 148 VDDIO 5029.2 -712.5 150 VCC 5154 -712.5 150 VCC 5154 -712.5 151 VCC 5257.8 -712.5 152 VCC 5334.0				
136 TR4 4114.8 -72.5 137 TR3 41910 -72.5 138 TR2 4267.2 -72.5 139 TR1 4343.4 -72.5 140 TR0 449.6 -72.5 141 VSS 4495.8 -72.5 141 VSS 4495.8 -72.5 142 VCOMH 4572.0 -72.5 143 VCOMH 4572.0 -72.5 144 VCOMH 4724.4 -72.5 145 VDD 4800.6 -72.5 146 VDD 4876.8 -72.5 147 VDDIO 4953.0 -72.5 148 VDDIO 5029.2 -72.5 149 VCC 51816 -72.5 150 VCC 51816 -72.5 151 VCC 5257.8 -72.5 152 VCC 5334.0 -72.5 154 VCC 5486.4 -72.5 </td <td></td> <td></td> <td></td> <td></td>				
137 TR3 41910 -712.5 138 TR2 4267.2 -712.5 139 TR1 4343.4 -712.5 140 TR0 4419.6 -712.5 141 VSS 4495.8 -712.5 141 VSS 4495.8 -712.5 142 VCOMH 4572.0 -712.5 143 VCOMH 468.2 -712.5 144 VCOMH 4724.4 -712.5 145 VDD 4800.6 -712.5 146 VDD 4876.8 -712.5 147 VDDIO 4953.0 -712.5 148 VDDIO 5029.2 -712.5 149 VCC 5105.4 -712.5 150 VCC 51816 -712.5 151 VCC 5257.8 -712.5 152 VCC 5334.0 -712.5 153 VCC 540.2 -712.5 154 VCC 5486.4				
138 TR2 4267.2 -72.5 139 TR1 4343.4 -72.5 140 TR0 449.6 -72.5 141 VSS 4495.8 -72.5 142 VCOMH 4572.0 -72.5 143 VCOMH 4572.0 -72.5 143 VCOMH 468.2 -72.5 144 VCOMH 4724.4 -72.5 145 VDD 4800.6 -72.5 146 VDD 4876.8 -72.5 147 VDDIO 4953.0 -72.5 148 VDDIO 5029.2 -72.5 150 VCC 5105.4 -72.5 150 VCC 5105.4 -72.5 151 VCC 5257.8 -712.5 152 VCC 5334.0 -712.5 153 VCC 540.2 -72.5 154 VCC 5486.4 -72.5 155 NC 5562.6 -72				
139 TR1 4343.4 -712.5 140 TR0 4419.6 -712.5 141 VSS 4495.8 -712.5 142 VCOMH 4572.0 -712.5 143 VCOMH 4648.2 -712.5 144 VCOMH 4724.4 -712.5 145 VDD 4800.6 -712.5 146 VDD 4876.8 -712.5 147 VDDIO 4953.0 -712.5 148 VDDIO 5029.2 -712.5 150 VCC 51816 -712.5 150 VCC 51816 -712.5 151 VCC 5257.8 -712.5 152 VCC 5334.0 -712.5 153 VCC 5410.2 -712.5 154 VCC 5486.4 -712.5 155 NC 5562.6 -712.5 156 VLSS 5638.8 -712.5 157 VLSS 5715.0 <td></td> <td></td> <td></td> <td></td>				
140 TR0 4419.6 -712.5 141 VSS 4495.8 -712.5 142 VCOMH 4572.0 -712.5 143 VCOMH 4572.0 -712.5 144 VCOMH 4648.2 -712.5 144 VCOMH 4724.4 -712.5 145 VDD 4800.6 -712.5 146 VDD 4876.8 -712.5 147 VDDIO 4953.0 -712.5 148 VDDIO 5029.2 -712.5 150 VCC 51816 -712.5 150 VCC 51816 -712.5 151 VCC 5257.8 -712.5 152 VCC 5334.0 -712.5 153 VCC 5486.4 -712.5 154 VCC 5486.4 -712.5 155 NC 5562.6 -712.5 156 VLSS 5638.8 -712.5 157 VLSS 5715.0 </td <td></td> <td></td> <td></td> <td></td>				
142 VCOMH 4572.0 -712.5 143 VCOMH 4648.2 -712.5 144 VCOMH 4724.4 -712.5 145 VDD 4800.6 -712.5 146 VDD 4876.8 -712.5 147 VDDIO 4953.0 -712.5 148 VDDIO 5029.2 -712.5 150 VCC 5105.4 -712.5 151 VCC 5257.8 -712.5 151 VCC 5257.8 -712.5 152 VCC 5334.0 -712.5 153 VCC 5410.2 -712.5 154 VCC 5486.4 -712.5 155 NC 5562.6 -712.5 156 VLSS 5638.8 -712.5 157 VLSS 5715.0 -712.5 158 NC 57912 -712.5 159 NC 6014.6 -712.5			4419.6	
143 VCOMH 4648.2 -72.5 144 VCOMH 4724.4 -72.5 145 VDD 4800.6 -72.5 146 VDD 4876.8 -72.5 147 VDDIO 4953.0 -72.5 148 VDDIO 5029.2 -72.5 149 VCC 51816 -72.5 150 VCC 51816 -72.5 151 VCC 5257.8 -712.5 152 VCC 5334.0 -72.5 153 VCC 5410.2 -72.5 154 VCC 5486.4 -72.5 155 NC 5562.6 -72.5 156 VLSS 5638.8 -72.5 157 VLSS 5715.0 -72.5 158 NC 57912 -72.5 159 NC 6014.6 -72.5				
144 VCOMH 4724.4 -72.5 145 VDD 4800.6 -72.5 146 VDD 4876.8 -72.5 147 VDDIO 4953.0 -72.5 148 VDDIO 5029.2 -72.5 149 VCC 5105.4 -72.5 150 VCC 51816 -72.5 151 VCC 5257.8 -72.5 152 VCC 5334.0 -72.5 153 VCC 5486.4 -72.5 154 VCC 5486.4 -72.5 155 NC 5562.6 -72.5 156 VLSS 5638.8 -72.5 157 VLSS 575.0 -72.5 158 NC 57912 -72.5 159 NC 604.6 -72.5				
145 VDD 4800.6 -712.5 146 VDD 4876.8 -712.5 147 VDDIO 4953.0 -712.5 148 VDDIO 5029.2 -712.5 149 VCC 5105.4 -712.5 150 VCC 51816 -712.5 151 VCC 5257.8 -712.5 152 VCC 5340.0 -712.5 153 VCC 5410.2 -712.5 154 VCC 5486.4 -712.5 155 NC 562.6 -712.5 156 VLSS 5638.8 -712.5 157 VLSS 5715.0 -712.5 158 NC 57912 -712.5 159 NC 6014.6 -712.5				
147 VDDIO 4953.0 -72.5 148 VDDIO 5029.2 -72.5 149 VCC 5105.4 -72.5 150 VCC 51816 -72.5 151 VCC 5257.8 -72.5 152 VCC 5334.0 -72.5 153 VCC 5410.2 -72.5 154 VCC 5486.4 -72.5 155 NC 5562.6 -72.5 156 VLSS 5638.8 -72.5 157 VLSS 5715.0 -72.5 158 NC 57912 -72.5 159 NC 6014.6 -712.5				
148 VDDIO 5029.2 -72.5 149 VCC 5105.4 -72.5 150 VCC 51816 -72.5 151 VCC 5257.8 -72.5 152 VCC 5334.0 -72.5 153 VCC 5410.2 -72.5 154 VCC 5486.4 -72.5 155 NC 5562.6 -72.5 156 VLSS 5638.8 -72.5 157 VLSS 5715.0 -72.5 158 NC 57912 -72.5 159 NC 604.6 -712.5				
149 VCC 5105.4 -712.5 150 VCC 51816 -712.5 151 VCC 5257.8 -712.5 152 VCC 5334.0 -712.5 153 VCC 5410.2 -712.5 154 VCC 5486.4 -712.5 155 NC 5562.6 -712.5 156 VLSS 5638.8 -712.5 157 VLSS 5715.0 -712.5 158 NC 57912 -712.5 159 NC 6014.6 -712.5				
150 VCC 51816 -712.5 151 VCC 5257.8 -712.5 152 VCC 5334.0 -712.5 153 VCC 5410.2 -712.5 154 VCC 5486.4 -712.5 155 NC 5562.6 -712.5 156 VLSS 5638.8 -712.5 157 VLSS 5715.0 -712.5 158 NC 57912 -712.5 159 NC 6014.6 -712.5				
151 VCC 5257.8 -712.5 152 VCC 5334.0 -712.5 153 VCC 5410.2 -712.5 154 VCC 5486.4 -712.5 155 NC 5562.6 -712.5 156 VLSS 5638.8 -712.5 157 VLSS 5715.0 -712.5 158 NC 57912 -712.5 159 NC 6014.6 -712.5				
153 VCC 5410.2 -712.5 154 VCC 5486.4 -712.5 155 NC 5562.6 -712.5 156 VLSS 5638.8 -712.5 157 VLSS 5715.0 -712.5 158 NC 57912 -712.5 159 NC 6014.6 -712.5	151			-712.5
154 VCC 5486.4 -712.5 155 NC 5562.6 -712.5 156 VLSS 5638.8 -712.5 157 VLSS 5715.0 -712.5 158 NC 57912 -712.5 159 NC 6014.6 -712.5				
155 NC 5562.6 -712.5 156 VLSS 5638.8 -712.5 157 VLSS 5715.0 -712.5 158 NC 57912 -712.5 159 NC 6014.6 -712.5				
156 VLSS 5638.8 -712.5 157 VLSS 5715.0 -712.5 158 NC 57912 -712.5 159 NC 6014.6 -712.5				
158 NC 57912 -712.5 159 NC 6014.6 -712.5	156	VLSS	5638.8	-712.5
159 NC 6014.6 -712.5				
3350.0 7 2.0				
	.50		2230.0	. 2.0

Pad no.	Pad Name	X-Axis	Y-Axis
161	NC NC	6167.0	-712.5 -712.5
162 163	NC NC	6243.2 6319.4	-7 12.5 -712.5
164	COM 31	6420.1	-647.9
165	COM30	6420.1	-606.1
166	COM 29	6420.1	-564.3
167	COM 28	6420.1	-522.5
168	COM 27	6420.1	-480.7
169 170	COM 26	6420.1	-438.9
171	COM 25 COM 24	6420.1 6420.1	-397.1 -355.3
172	COM 23	6420.1	-313.5
173	COM 22	6420.1	-271.7
174	COM 21	6420.1	-229.9
175	COM 20	6420.1	-188.1
176 177	COM 19	6420.1 6420.1	-146.3 -104.5
178	COM 18 COM 17	6420.1	-62.7
179	COM 16	6420.1	-20.9
180	COM 15	6420.1	20.9
181	COM 14	6420.1	62.7
182	COM 13	6420.1	104.5
183	COM 12	6420.1	146.3
184 185	COM 11 COM 10	6420.1 6420.1	188.1 229.9
186	COM D	6420.1	2717
187	COM8	6420.1	313.5
188	COM7	6420.1	355.3
189	COM6	6420.1	397.1
190	COM 5	6420.1	438.9
191 192	COM4	6420.1	480.7 522.5
193	COM3 COM2	6420.1 6420.1	564.3
194	COM 1	6420.1	606.1
195	COM 0	6420.1	647.9
196	VLSS	5908.5	643.6
197	SA0	5828.1	643.6
198	SB0	5787.9	643.6
199 200	SC0 SA1	5747.7 5707.5	643.6 643.6
200	SB1	5667.3	643.6
202	SC1	5627.1	643.6
203	SA2	5586.9	643.6
204	SB2	5546.7	643.6
205	SC2	5506.5	643.6
206 207	SA3 SB3	5466.3 5426.1	643.6 643.6
208	SC3	5385.9	643.6
209	SA4	5345.7	643.6
210	SB4	5305.5	643.6
211	SC4	5265.3	643.6
212	SA5	5225.1	643.6
213 214	SB5 SC5	5184.9 5144.7	643.6 643.6
215	SA6	5 H4.7 5104.5	643.6
216	SB6	5064.3	643.6
217	SC6	5024.1	643.6
218	SA7	4983.9	643.6
219	SB7	4943.7	643.6
220 221	SC7 SA8	4903.5 4863.3	643.6 643.6
222	SB8	4823.1	643.6
223	SC8	4782.9	643.6
224	SA9	4742.7	643.6
225	SB9	4702.5	643.6
226	SC9	4662.3	643.6
227 228	SA 10 SB 10	4622.1 4581.9	643.6 643.6
228	SC 10	458 l.9 4541.7	643.6
230	SA 11	4501.5	643.6
231	SB 11	44613	643.6
232	SC 11	44211	643.6
233	SA 12	4380.9	643.6
234	SB 12	4340.7	643.6
235 236	SC 12 SA 13	4300.5	643.6 643.6
236	SA 13 SB 13	4260.3 4220.1	643.6
238	SC 13	4179.9	643.6
239	SA 14	4139.7	643.6
240	SB 14	4099.5	643.6

SSD1331 Rev 1.0 P 9/68 Jul 2006 **Solomon Systech**

Pad no.	Pad Name	X-Axis	Y-Axis
241	SC14	4059.3	643.6
242	SA 15	4019.1	643.6
243	SB 15	3978.9	643.6
244	SC 15	3938.7	643.6
245	SA 16	3898.5	643.6
246	SB 16	3858.3	643.6
247	SC 16	3818.1	643.6
248	SA 17	3777.9	643.6
249	SB 17	3737.7	643.6
250	SC 17	3697.5	643.6
251	SA 18	3657.3	643.6
252	SB 18	3617.1	643.6
253	SC 18	3576.9	643.6
254	SA 19	3536.7	643.6
255	SB 19	3496.5	643.6
256	SC 19	3456.3	643.6
257	SA 20	3416.1	643.6
258	SB 20	3375.9	643.6
259	SC20	3335.7	643.6
260	SA 21	3295.5	643.6
261	SB 21	3255.3	643.6
262	SC21	3215.1	643.6
263	SA 22	3174.9	643.6
264	SB 22	3134.7	643.6
265	SC22	3094.5	643.6
266	SA 23	3054.3	643.6
267	SB 23	3014.1	643.6
268	SC23	2973.9	643.6
269	SA 24	2933.7	643.6
270	SB 24	2893.5	643.6
271	SC24	2853.3	643.6
272	SA 25	2813.1	643.6
273	SB 25	2772.9	643.6
274	SC25	2732.7	643.6
275	SA26	2692.5	643.6
276	SB 26	2652.3	643.6
277	SC26	2612.1	643.6
278	SA 27		643.6
		2571.9	
279	SB 27	2531.7	643.6
280	SC27	2491.5	643.6
281	SA 28	2451.3	643.6
282	SB 28	2411.1	643.6
283	SC28	2370.9	643.6
284	SA 29	2330.7	643.6
285	SB 29	2290.5	643.6
286	SC29	2250.3	643.6
287	SA 30	2210.1	643.6
288	SB 30	2169.9	643.6
289	SC30	2129.7	643.6
290	SA31	2089.5	643.6
291	SB31	2049.3	643.6
292	SC31	2009.1	643.6
293	SA 32	1968.9	643.6
294	SB 32	1928.7	643.6
295	SC32	1888.5	643.6
296	SA 33	1848.3	643.6
297	SB 33	1808.1	643.6
298	SC33	1767.9	643.6
299	SA 34	1727.7	643.6
300	SB 34	1687.5	643.6
301	SC34	1647.3	643.6
302	SA 35	1607.1	643.6
303	SB 35	1566.9	643.6
304			
	SC35	1526.7	643.6
305	SC35 SA36	1526.7 1486.5	643.6 643.6
305	SA 36	1486.5	643.6
305 306	SA 36 SB 36	1486.5 1446.3	643.6 643.6
305 306 307	SA 36 SB 36 SC 36	1486.5 1446.3 1406.1	643.6 643.6 643.6
305 306 307 308	SA36 SB36 SC36 SA37	1486.5 1446.3 1406.1 1365.9	643.6 643.6 643.6 643.6
305 306 307 308 309	SA36 SB36 SC36 SA37 SB37	1486.5 1446.3 1406.1 1365.9 1325.7	643.6 643.6 643.6 643.6 643.6
305 306 307 308 309 310 311	SA36 SB36 SC36 SA37 SB37 SC37 SA38	1486.5 1446.3 1406.1 1365.9 1325.7 1285.5 1245.3	643.6 643.6 643.6 643.6 643.6 643.6 643.6
305 306 307 308 309 310 311 312	SA36 SB36 SC36 SA37 SB37 SC37 SA38 SB38	1486.5 1446.3 1406.1 1365.9 1325.7 1285.5 1245.3 1205.1	643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6
305 306 307 308 309 310 311 312 313	SA36 SB36 SC36 SA37 SB37 SC37 SA38 SB38 SC38	1486.5 1446.3 1406.1 1365.9 1325.7 1285.5 1245.3 1205.1 1164.9	643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6
305 306 307 308 309 310 311 312 313	SA36 SB36 SC36 SA37 SB37 SC37 SA38 SB38 SC38 SA39	1486.5 1446.3 1406.1 1365.9 1325.7 1285.5 1245.3 1205.1 1164.9 1124.7	643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6
305 306 307 308 309 310 311 312 313 314 315	SA36 SB36 SC36 SA37 SB37 SC37 SA38 SB38 SC38 SC38 SA39 SB39	1486.5 1446.3 1406.1 1365.9 1325.7 1285.5 1245.3 1205.1 1164.9 1124.7 1084.5	643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6
305 306 307 308 309 310 311 312 313 314 315 316	SA36 SB36 SC36 SA37 SB37 SC37 SA38 SB38 SC38 SA39 SB39 SC39	1486.5 1446.3 1406.1 1365.9 1325.7 1285.5 1245.3 1205.1 1164.9 1124.7 1084.5	643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6
305 306 307 308 309 310 311 312 313 314 315 316	SA36 SB36 SC36 SA37 SB37 SC37 SA38 SB38 SC38 SA39 SB39 SC39	1486.5 1446.3 1406.1 1365.9 1325.7 1285.5 1245.3 1205.1 1164.9 1124.7 1084.5 1044.3	643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6
305 306 307 308 309 310 311 312 313 314 315 316 317 318	SA36 SB36 SC36 SA37 SB37 SC37 SA38 SB38 SC38 SC38 SC39 SC39 SC39 SC40 SB40	1486.5 1446.3 1406.1 1365.9 1325.7 1285.5 1245.3 1205.1 1164.9 1124.7 1084.5 1044.3 1004.1 963.9	643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6
305 306 307 308 309 310 311 312 313 314 315 316	SA36 SB36 SC36 SA37 SB37 SC37 SA38 SB38 SC38 SA39 SB39 SC39	1486.5 1446.3 1406.1 1365.9 1325.7 1285.5 1245.3 1205.1 1164.9 1124.7 1084.5 1044.3	643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6 643.6

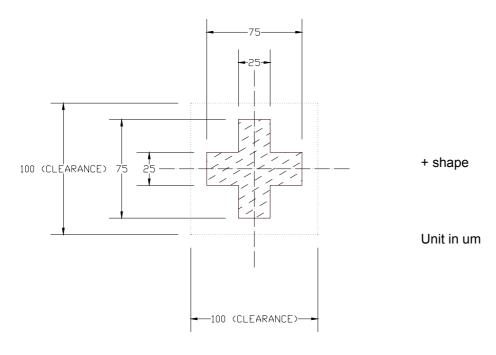
Pad no.	Pad Name	X-Axis	Y-Axis
321	SB41 SC41	843.3	643.6
322 323	SA42	803.1 762.9	643.6 643.6
324	SB42	722.7	643.6
325	SC42	682.5	643.6
326	SA43	642.3	643.6
327	SB43	602.1	643.6
328	SC43	5619	643.6
329 330	SA44 SB44	521.7 481.5	643.6 643.6
331	SC44	4413	643.6
332	SA45	4011	643.6
333	SB45	360.9	643.6
334	SC45	320.7	643.6
335 336	SA46 SB46	280.5 240.3	643.6 643.6
337	SC46	200.1	643.6
338	SA47	159.9	643.6
339	SB47	119.7	643.6
340	SC47	79.5	643.6
341	SA48	-81.3	643.6
342 343	SB48 SC48	-121.5 -161.7	643.6 643.6
344	SA49	-2019	643.6
345	SB49	-242.1	643.6
346	SC49	-282.3	643.6
347	SA50	-322.5	643.6
348 349	SB50	-362.7	643.6
349	SC50 SA51	-402.9 -443.1	643.6 643.6
351	SB51	-443.1	643.6
352	SC51	-523.5	643.6
353	SA52	-563.7	643.6
354	SB52	-603.9	643.6
355 356	SC52 SA53	-644.1 -684.3	643.6 643.6
357	SB53	-724.5	643.6
358	SC53	-764.7	643.6
359	SA54	-804.9	643.6
360	SB54	-845.1	643.6
361	SC54	-885.3	643.6
362 363	SA55 SB55	-925.5 -965.7	643.6 643.6
364	SC55	-905.7 -1005.9	643.6
365	SA56	-1046.1	643.6
366	SB56	-1086.3	643.6
367	SC56	-1126.5	643.6
368	SA57	-1166.7	643.6
369 370	SB57 SC57	-1206.9 -1247.1	643.6 643.6
371	SA58	-1287.3	643.6
372	SB58	-1327.5	643.6
373	SC58	-1367.7	643.6
374	SA59	-1407.9	643.6
375 376	SB59 SC59	-1448.1 -1488.3	643.6 643.6
377	SA60	- H66.3 -1528.5	643.6
378	SB60	-1568.7	643.6
379	SC60	-1608.9	643.6
380	SA61	-1649.1	643.6
381 382	SB61 SC61	-1689.3 -1729.5	643.6 643.6
383	SA62	-1769.7	643.6
384	SB62	-1809.9	643.6
385	SC62	-1850.1	643.6
386	SA63	-1890.3	643.6
387	SB63	-1930.5	643.6
388 389	SC63 SA64	-1970.7 -2010.9	643.6 643.6
390	SB 64	-2051.1	643.6
391	SC64	-20913	643.6
392	SA65	-2131.5	643.6
393	SB 65	-2171.7	643.6
394	SC65	-2211.9	643.6
395 396	SA 66 SB 66	-2252.1 -2292.3	643.6 643.6
397	SC66	-2332.5	643.6
398	SA67	-2372.7	643.6
399	SB67	-2412.9	643.6
400	SC67	-2453.1	643.6

Pad no.	Pad Name	X-A xis	Y-Axis
401 402	SA 68 SB 68	-2493.3 -2533.5	643.6 643.6
403	SC68	-2573.7	643.6
404	SA 69	-2613.9	643.6
405	SB 69	-2654.1	643.6
406	SC69	-2694.3	643.6
407	SA 70	-2734.5	643.6
408 409	SB 70	-2774.7 -2814.9	643.6
410	SC70 SA71	-2855.1	643.6 643.6
411	SB71	-2895.3	643.6
412	SC71	-2935.5	643.6
413	SA72	-2975.7	643.6
414	SB 72	-3015.9	643.6
415 416	SC72 SA73	-3056.1 -3096.3	643.6 643.6
417	SB 73	-3136.5	643.6
418	SC73	-3176.7	643.6
419	SA 74	-3216.9	643.6
420	SB 74	-3257.1	643.6
421	SC74	-3297.3	643.6
422	SA 75	-3337.5	643.6
423 424	SB 75 SC 75	-3377.7 -3417.9	643.6 643.6
425	SA76	-3458.1	643.6
426	SB 76	-3498.3	643.6
427	SC76	-3538.5	643.6
428	SA77	-3578.7	643.6
429	SB 77	-3618.9	643.6
430	SC77	-3659.1	643.6
431 432	SA 78 SB 78	-3699.3 -3739.5	643.6 643.6
433	SC78	-3779.7	643.6
434	SA 79	-3819.9	643.6
435	SB 79	-3860.1	643.6
436	SC79	-3900.3	643.6
437	SA 80	-3940.5	643.6
438	SB 80	-3980.7	643.6
439 440	SC80 SA81	-4020.9 -4061.1	643.6 643.6
441	SB81	-4101.3	643.6
442	SC81	-4141.5	643.6
443	SA 82	-4181.7	643.6
444	SB 82	-4221.9	643.6
445	SC82	-4262.1	643.6
446 447	SA 83 SB 83	-4302.3 -4342.5	643.6 643.6
448	SC83	-4342.7	643.6
449	SA 84	-4422.9	643.6
450	SB 84	-4463.1	643.6
451	SC84	-4503.3	643.6
452	SA 85	-4543.5	643.6
453 454	SB 85 SC 85	-4583.7 -4623.9	643.6 643.6
455	SA 86	-4623.9 -4664.1	643.6
456	SB 86	-4704.3	643.6
457	SC86	-4744.5	643.6
458	SA 87	-4784.7	643.6
459	SB 87	-4824.9	643.6
460 461	SC87 SA88	-4865.1 -4905.3	643.6 643.6
462	SB 88	-4905.5 -4945.5	643.6
463	SC88	-4985.7	643.6
464	SA 89	-5025.9	643.6
465	SB 89	-5066.1	643.6
466	SC89	-5106.3	643.6
467 468	SA 90	-5146.5 -5186.7	643.6
468 469	SB 90 SC 90	-5186.7	643.6 643.6
470	SA91	-5267.1	643.6
471	SB91	-5307.3	643.6
472	SC91	-5347.5	643.6
473	SA 92	-5387.7	643.6
474	SB 92	-5427.9	643.6
475 476	SC92 SA93	-5468.1 -5508.3	643.6
476	SB 93	-5508.3 -5548.5	643.6 643.6
478	SC93	-5588.7	643.6
479	SA 94	-5628.9	643.6
480	SB 94	-5669.1	643.6

 Solomon Systech
 Jul 2006
 P 10/68
 Rev 1.0
 SSD1331

Pad no.	Pad Name	X-Axis	Y-Axis
481	SC94	-5709.3	643.6
482	SA95	-5749.5	643.6
483	SB 95	-5789.7	643.6
484	SC95	-5829.9	643.6
485	VLSS	-5910.3	643.6
486	COM 32	-6420.1	647.9
487	COM 33	-6420.1	606.1
488	COM 34	-6420.1	564.3
489	COM 35	-6420.1	522.5
490	COM 36	-6420.1	480.7
491	COM 37	-6420.1	438.9
492	COM 38	-6420.1	397.1
493	COM 39	-6420.1	355.3
494	COM 40	-6420.1	313.5
495	COM41	-6420.1	271.7
496	COM 42	-6420.1	229.9
497	COM 43	-6420.1	188.1
498	COM 44	-6420.1	146.3
499	COM 45	-6420.1	104.5
500	COM 46	-6420.1	62.7
501	COM 47	-6420.1	20.9
502	COM 48	-6420.1	-20.9
503	COM 49	-6420.1	-62.7
504	COM 50	-6420.1	-104.5
505	COM 51	-6420.1	-146.3
506	COM 52	-6420.1	-188.1
507	COM 53	-6420.1	-229.9
508	COM 54	-6420.1	-271.7
509	COM 55	-6420.1	-313.5
510	COM 56	-6420.1	-355.3
511	COM 57	-6420.1	-397.1
512	COM 58	-6420.1	-438.9
513	COM 59	-6420.1	-480.7
514	COM 60	-6420.1	-522.5
515	COM 61	-6420.1	-564.3
516	COM 62	-6420.1	-606.1
517	COM 63	-6420.1	-647.9

Figure 3 - SSD1331Z Alignment mark dimensions



SSD1331 Rev 1.0 P 11/68 Jul 2006 **Solomon Systech**

6 PIN DESCRIPTION

Pin Name	Pin Type	Description
V_{DD}	Power	Power supply pin for core V _{DD}
AV_{DD}	Power	Analog power supply. It must be connected to V _{DD} during operation.
V _{DDIO}	Power	Power supply for interface logic level. It should be match with the MCU interface voltage level. V_{DDIO} must always be equal or lower than V_{DD} .
V _{CC}	Power	Power supply for panel driving voltage. This is also the most positive power voltage supply pin.
V_{SS}	Power	Ground pin
V_{LSS}	Power	Analog system ground pin.
V _{COMH}	0	COM signal deselected voltage level. A capacitor should be connected between this pin and V _{SS} .
BGGND	Power	Connect to Ground
V_{DDB}	Power	Reserved pin. It should be connect to V_{DD} externally.
V_{SSB}	Power	Reserved pin. It should be connected to V _{SS} externally.
GDR	0	Reserved pin. Keep NC (i.e. no connection).
FB	I	Reserved pin. Keep NC (i.e. no connection).
V_{BREF}	0	Reserved pin. Keep NC (i.e. no connection).
GP0	I/O	Reserved pin. Keep NC (i.e. no connection).
GP1	I/O	Reserved pin. Keep NC (i.e. no connection).
V _{CIR}	0	Reserved pin. Keep NC (i.e. no connection).
BS[3:0]	1	MCU bus interface selection pins.
		Table 3 - Bus Interface selection
		BS[3:0] Bus Interface Selection
		Document Document
I _{REF}	I	This pin is the segment output current reference pin. A resistor should be connected between this pin and Vas to maintain the last
		A resistor should be connected between this pin and $V_{\rm SS}$ to maintain the I _{REF} current at 10uA. Please refer to Figure 14 for the details formula of resistor value.

 Solomon Systech
 Jul 2006
 P 12/68
 Rev 1.0
 SSD1331

Pin Name	Pin Type	Description
FR	0	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieve to prevent tearing effect. Keep NC if not used. Refer to section 7.3.2 for details usage.
CL	I	External clock input pin. When internal clock is enable, this pin is not used and should be kept NC. When internal clock is disable, this pin is the external clock source input pin.
CLS	I	Internal clock selection pin. When this pin is pulled high (i.e. connect to V _{DDIO}), internal oscillator is enable (normal operation). When this pin is pulled low, an external clock signal should be connected to CL.
CS#	I	This pin is the chip select input connecting to the MCU.
RES#	I	This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin high (i.e. connect to V_{DDIO}) during normal operation.
D/C#	I	This pin is Data/Command control pin connecting to the MCU. When the pin is pulled high (i.e. connect to V_{DDIO}), the data at D[15:0]will be interpreted as display data. When the pin is pulled low, the data at D[15:0] will be interpreted as command.
R/W# (WR#)	l	This pin is read / write control input pin connecting to the MCU interface. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled high (i.e. connect to V_{DDIO}) and write mode when low. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin R/W#(WR#) must be connected to V_{SS} .
E (RD#)	I	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high (i.e. connect to V_{DDIO}) and the chip is selected. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin E(RD#) must be connected to V_{SS} .
D[15:0]	I/O	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie low. (Except for D2 pin in serial mode) Refer to Section 7.1 for different bus interface connection.
SA[95:0] SB[95:0] SC[95:0]	0	These pins provide the OLED segment driving signals. These pins are in high impedance state when display is off by command Set Display Off. These 288 segment pins are divided into 3 groups, SA, SB and SC. Each group can have different color settings for color A, B and C.

SSD1331 Rev 1.0 P 13/68 Jul 2006 **Solomon Systech**

Pin Name	Pin Type	Description
COM[63:0]	I/O	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is off by command Set Display Off.
TR[11:0]	1	Testing reserved pins. These pins should be kept float.
NC		Dummy pins. These pins should be kept float and should not be connected to any other signal pins nor any electrical signal. Do not connect NC pins together.

 Solomon Systech
 Jul 2006
 P 14/68
 Rev 1.0
 SSD1331

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 MCU Interface Selection

SSD1331 MCU interface consist of 16 data pin and 5 control pins. The pin assignment at different interface mode is summarized in Table 4. Different MCU mode can be set by hardware selection on BS[3:0] pins (refer to Table 3 for BS pins setting)

Table 4 - MCU interface assignment under different bus interface mode

Pin Name	Data / Co	Control Signal							
Bus Interface	D15 D14 D13 D12 D11 D10 D9 D8	B D7 D6 D5 D4 D3	D2 D1	D0	Е	R/W#	CS#	D/C#	RES#
8ь / 8080	Tie Low	D7-D0	D7-D0					D/C#	RES#
8ь / 6800	Tie Low	D7-D0	D7-D0					D/C#	RES#
9ь / 8080	Tie Low	D8-D0	D8-D0					D/C#	RES#
9ь / 6800	Tie Low	D8-D0	D8-D0					D/C#	RES#
16b / 8080	•	D15-D0						D/C#	RES#
16b / 6800				Е	R/W#	CS#	D/C#	RES#	
SPI	Tie Low		NC SDIN	SCLK	Tie	Low	CS#	D/C#	RES#

7.1.1 6800-series Parallel Interface

A low in R/W# indicates WRITE operation and high in R/W# indicates READ operation.

A low in D/C# indicates COMMAND read/write and high in D/C# indicates DATA read/write.

The E input serves as data latch signal while CS# is low. Data is latched at the falling edge of E signal.

Table 5 - Control pins of 6800 interface

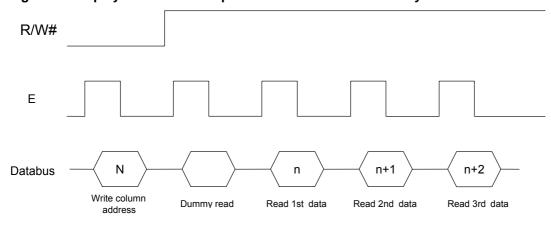
Function	E	R/W#	CS#	D/C#
Write command	\downarrow	L	L	L
Read status	\downarrow	Н	L	L
Write data	\downarrow	L	L	Н
Read data	\downarrow	Н	L	Н

Note

(1) ↓ stands for falling edge of signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 4

Figure 4 - Display data read back procedure - insertion of dummy read



SSD1331 | Rev 1.0 | P 15/68 | Jul 2006 | **Solomon Systech**

⁽²⁾ H stands for high in signal

⁽³⁾ L stands for low in signal

7.1.2 8080-series Parallel Interface

A low in D/C# indicates COMMAND read/write and high in D/C# indicates DATA read/write. A rising edge of RD# input serves as a data READ latch signal while CS# is kept low. A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept low.

Figure 5 – Example of Write procedure in 8080 parallel interface mode

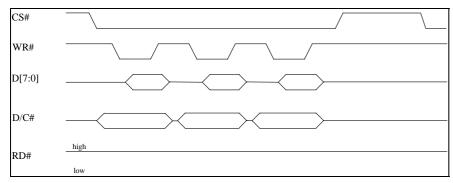


Figure 6 - Example of Read procedure in 8080 parallel interface mode

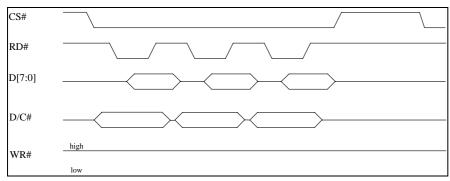


Table 6 - Control pins of 8080 interface (Form 1)

Function	RD#	WR#	CS#	D/C#
Write command	Н	1	L	L
Read status	1	Н	L	L
Write data	Н	\uparrow	L	Н
Read data	\uparrow	Н	L	Н

Note

Alternatively, E(RD#) and R/W#(WR#) can be keep stable while CS# is serve as the data/command latch signal.

Table 7 - Control pins of 8080 interface (Form 2)

Function	RD#	WR#	CS#	D/C#
Write command	Н	L	1	L
Read status	L	Н	1	L
Write data	Н	L	\uparrow	Н
Read data	Ĺ	Н	1	Н

Note

(1) ↑ stands for rising edge of signal

Solomon Systech Jul 2006 P 16/68 Rev 1.0 SSD1331

 $^{^{(1)}}$ \uparrow stands for rising edge of signal

H stands for high in signal

⁽³⁾ L stands for low in signal

⁽⁴⁾ Refer to Figure 38 for Form 1 8080-Series MPU Parallel Interface Timing Characteristics

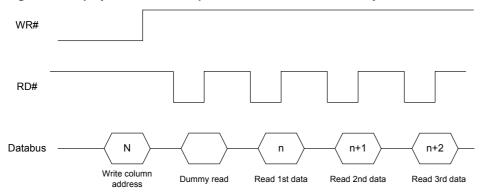
⁽²⁾ H stands for high in signal

⁽³⁾ L stands for low in signal

⁽⁴⁾ Refer to Figure 39 for Form 2 8080-Series MPU Parallel Interface Timing Characteristics

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7.

Figure 7 - Display data read back procedure - insertion of dummy read



7.1.3 Serial Interface

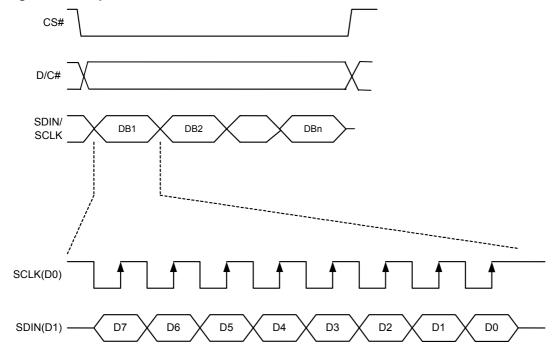
The serial interface consists of serial clock SCLK (D0), serial data SDIN (D1), D/C# and CS#. SCLK is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock.

Under serial mode, only write operations are allowed.

Table 8 - Control pins of Serial interface

Function	Е	R/W#	CS#	D/C#
Write command	Tie low	Tie low	L	L
Write data	Tie low	Tie low	L	Н

Figure 8 - Write procedure in SPI mode



SSD1331 | Rev 1.0 | P 17/68 | Jul 2006 | Solomon Systech

7.2 Command Decoder

This module determines whether the input should be interpreted as data or command based upon the input of the D/C# pin.

If D/C# pin is high, data is written to Graphic Display Data RAM (GDDRAM). If it is low, the inputs at D0-D15 are interpreted as a Command and it will be decoded and be written to the corresponding command register.

7.3 Oscillator Circuit and Display Time Generator

7.3.1 Oscillator

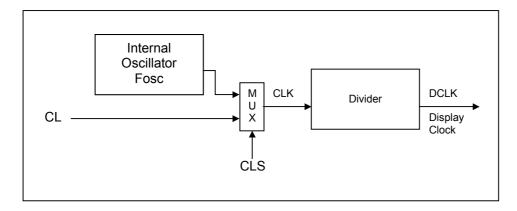


Figure 9 - Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 9). The operation clock (CLK) can be generated either from internal oscillator or external source CL pin by CLS pin. If CLS pin is high, internal oscillator is selected. If CLS pin is low, external clock from CL pin will be used for CLK. The frequency of internal oscillator F_{OSC} can be programmed by command B3h (Set oscillator frequency).

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command B3h.

$$DCLK = F_{osc} / D$$

The frame frequency of display is determined by the following formula.

$$F_{FRM} = \frac{F_{osc}}{D \times K \times No. \text{ of Mux}}$$

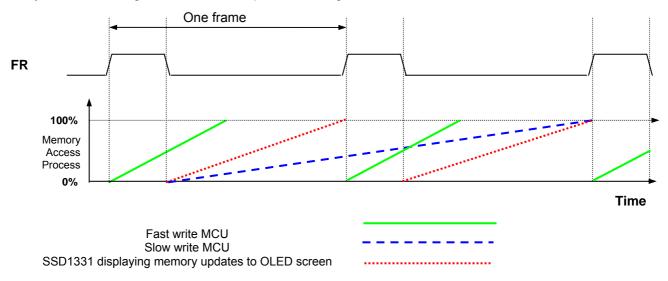
where

- D stands for clock divide ratio. It is set by command B3h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by
 K = Phase 1 period + Phase 2 period + PW63 (longest current drive pulse width)
 = 4 + 7 + 125 = 136 at power on reset
- Number of multiplex ratio is set by command A8h. The power on reset value is 64
- F_{OSC} is the oscillator frequency. It can be adjusted by command B3h A[7:4]

Solomon Systech Jul 2006 P 18/68 Rev 1.0 SSD1331

7.3.2 FR synchronization

FR synchronization signal can be used to prevent tearing effect.



The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete(more than one frame but within two frames), it is a slow write one.

For fast write MCU: MCU should start to write new frame of ram data just after rising edge of FR pulse and should be finished well before the rising edge of the next FR pulse.

For slow write MCU: MCU should start to write new frame ram data after the falling edge of the 1st FR pulse and must be finished before the rising edge of the 3rd FR pulse.

7.4 Reset Circuit

When RES# input is pulled low, the chip is initialized with the following status:

- 1. Display is OFF
- 2. 64 MUX Display Mode
- 3. Display start line is set at display RAM address 0
- 4. Display offset set to 0
- 5. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00H and COM0 mapped to address 00H)
- 6. Column address counter is set at 0
- 7. Master contrast control register is set at 0FH
- 8. Individual contrast control registers of color A, B, and C are set at 80H
- 9. Shift register data clear in serial interface
- 10. Normal display mode (Equivalent to A4 command)

SSD1331 | Rev 1.0 | P 19/68 | Jul 2006 | **Solomon Systech**

7.5 Graphic Display Data RAM (GDDRAM)

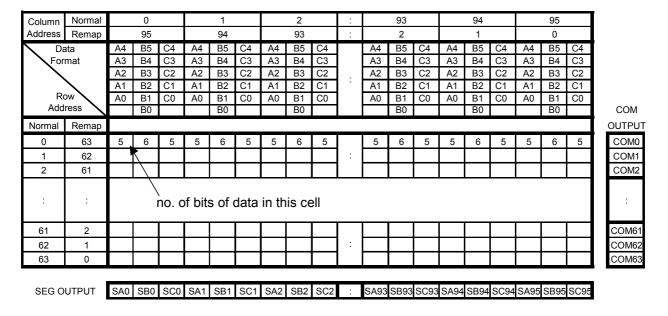
7.5.1 GDDRAM structure

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 96 x 64 x 16bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Each pixel has 16-bit data. Three sub-pixels for color A, B and C have 6 bits, 5 bits and 6 bits respectively. The arrangement of data pixel in graphic display data RAM is shown below.

Figure 10 - 65k Color Depth Graphic Display Data RAM Structure



7.5.2 Data bus to RAM mapping under different input mode

Table 9 - Data bus usage under different bus width and color depth mode

				Data	a bus														
Bus	width	Color Depth	Input order	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8	bits	256		X	X	X	X	X	X	X	X	C_4	C_3	\mathbb{C}_2	B_5	B_4	B_3	A_4	A_3
8	bits	65k format 1	1st	X	X	X	X	X	X	X	X	C ₄	C ₃	C_2	C_1	C ₀	B ₅	B ₄	\mathbf{B}_3
			2nd	X	X	X	X	X	X	X	X	\mathbf{B}_2	B_1	\mathbf{B}_0	A_4	A_3	A_2	A_1	A_0
8	bits	65k format 2	1st	X	X	X	X	X	X	X	X	X	X	C ₄	C ₃	C_2	C ₁	C_0	X
			2nd	X	X	X	X	X	X	X	X	X	X	B_5	B_4	\mathbf{B}_3	\mathbf{B}_2	\mathbf{B}_1	\mathbf{B}_0
			3rd	X	X	X	X	X	X	X	X	X	X	A_4	A_3	A_2	A_1	A_0	X
16	bits	65k		C_4	C_3	C_2	C_1	C_0	B_5	B_4	\mathbf{B}_3	\mathbf{B}_2	B_1	\mathbf{B}_0	A_4	A_3	A_2	A_1	A_0
9	bits	65k	1st	X	X	X	X	X	X	X	C_4	C_3	C_2	C_1	C_0	X	B_5	B_4	\mathbf{B}_3
			2nd	X	X	X	X	X	X	X	\mathbf{B}_2	\mathbf{B}_1	B_0	A_4	A_3	A_2	A_1	A_0	X

Solomon Systech Jul 2006 | P 20/68 | Rev 1.0 | SSD1331

7.5.3 RAM mapping and Different color depth mode

At 65k color depth mode, color A, B, C are directly mapped to the RAM content. At 256-color mode, the RAM content will be filled up to 65k format.

Figure 11 - 256-color mode mapping

			SCn			SBn						SAn					
65k color	C_4	C_3	C_2	C_1	\mathbf{B}_{5}	B_4	\mathbf{B}_3	B_2	\mathbf{B}_1	B_0	A_4	A_3	A_2	A_1	A_0		
256 color	C_4	C_3	C_2	*C ₄	*C ₄	B_5	B_4	\mathbf{B}_3	B_5	*B ₅	*B ₅	A_4	A_3	*A ₄	*A ₄	*A ₄	

Note:

 $^{(1)}$ n = 0 ~ 95

7.6 Gray Scale Decoder

The gray scale effect is generated by controlling the pulse width of segment drivers in current drive phase. The gray scale table stores the corresponding pulse widths of the 63 gray scale levels (GS0~GS63). The wider the pulse width, the brighter the pixel will be. A single gray scale table supports all the three colors A, B and C. The pulse widths can be set by software commands.

As shown in Figure 12, color B sub-pixel RAM data has 6 bits, represent the 64 gray scale levels from GS0 to GS63. color A and color C sub-pixel RAM data has only 5 bits, represent 32 gray scale levels from GS0, GS2, ..., GS62.

Figure 12 - Relation between GDRAM content and gray scale table entry for three colors in 65K color mode

Color A, C	Color B	Gray Scale	Default pulse width of GS[0:63]
RAM data (5 bits)	RAM data (6 bits)		in terms of DCLK
00000	000000	GS0	0
-	000001	GS1	1
00001	000010	GS2	3
-	000011	GS3	5
00010	000100	GS4	7
:	••	:	:
:	••	:	:
:	••	:	:
11110	111100	GS60	119
-	111101	GS61	121
11111	111110	GS62	123
-	111111	GS63	125

The duration of different GS are programmable.

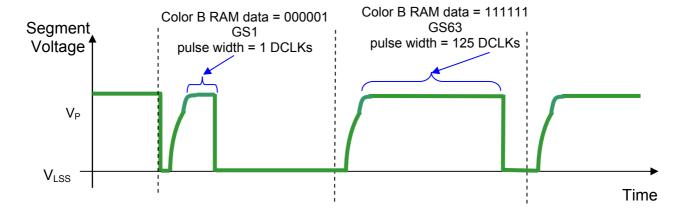
SSD1331 | Rev 1.0 | P 21/68 | Jul 2006 | **Solomon Systech**

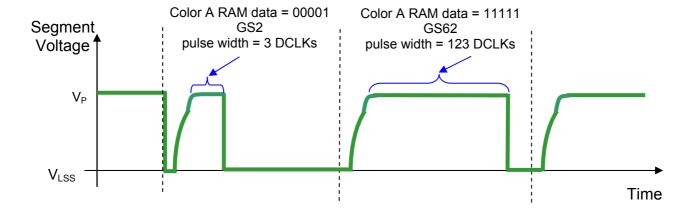
⁽²⁾ bits with * are copied from corresponding bits in order to fill up 65K format.

Figure 13 - Illustration of relation between graphic display RAM value and gray scale control

Gray scale table

Gray Scale	Value/DCLKs
GS0	0
GS1	1
GS2	3
:	:
GS62	123
GS63	125





 Solomon Systech
 Jul 2006
 P 22/68
 Rev 1.0
 SSD1331

7.7 SEG / COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

 I_{SEG} = Contrast / 256 x I_{REF} x scale factor

in which

the contrast $(0\sim255)$ is set by Set Contrast command; and the scale factor $(1\sim16)$ is set by Master Current Control command.

For example, in order to achieve I_{SEG} = 160uA at maximum contrast 255, I_{REF} is set to around 10uA. This current value is obtained by connecting an appropriate resistor from I_{REF} pin to V_{SS} as shown in Figure 14.

Recommended range for $I_{REF} = 10uA +/- 2uA$

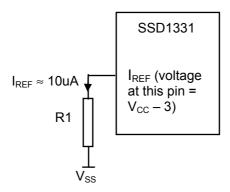
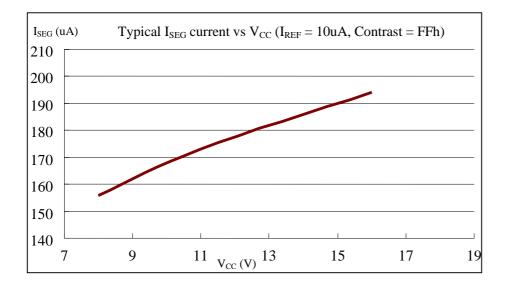


Figure 14 - I_{REF} Current Setting by Resistor Value

Since the voltage at I_{REF} pin is $V_{CC}-3V$, the value of resistor R1 can be found as below. R1 = (Voltage at $I_{REF}-V_{SS}$) / I_{REF} = ($V_{CC}-3$) / $10uA \approx 1.3M\Omega$ for V_{CC} = 16V.

Figure 15 - I_{SEG} current vs V_{CC} setting at constant I_{REF} , Contrast = FFh

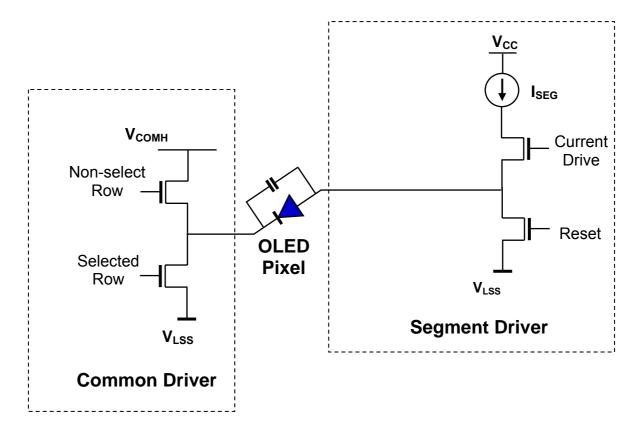


SSD1331 | Rev 1.0 | P 23/68 | Jul 2006 | **Solomon Systech**

7.8 Common and Segment Drivers

Segment drivers consist of 288 (96 x 3 colors) current sources to drive OLED panel. The driving current can be adjusted from 0 to 160uA with 256 steps by contrast setting command (81h,82h,83h). Common drivers generate scanning voltage pulse. The block diagrams and waveforms of the segment and common driver are shown as follow.

Figure 16 - Segment and Common Driver Block Diagram

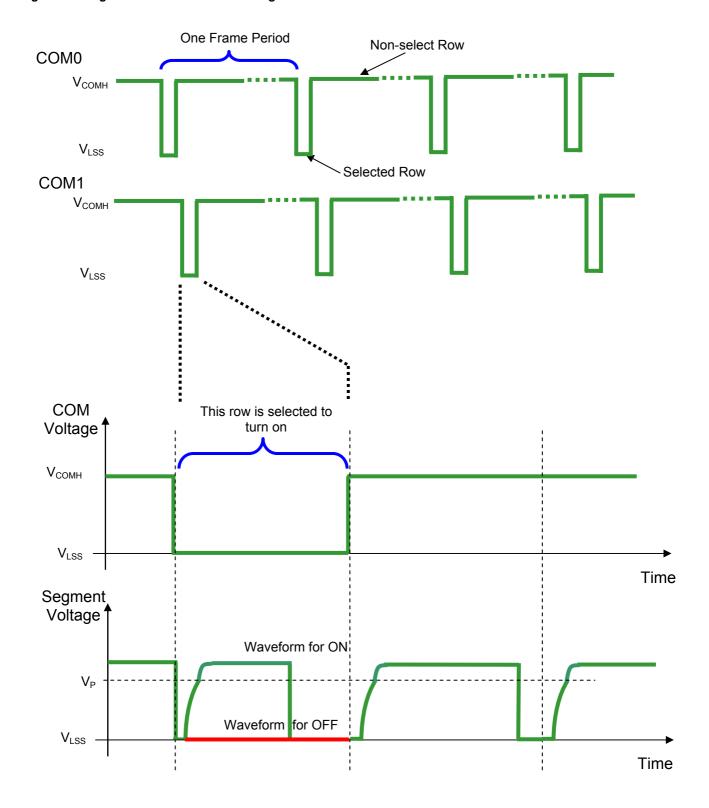


The commons are scanned sequentially, row by row. If a row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH} as shown in Figure 17

In the scanned row, the pixels on the row will be turned ON or OFF by sending the corresponding data signal to the segment pins. If the pixel is turned OFF, the segment current is kept at 0. On the other hand, the segment drives to I_{SEG} when the pixel is turned ON.

Solomon Systech Jul 2006 P 24/68 Rev 1.0 SSD1331

Figure 17 - Segment and Common Driver Signal Waveform



SSD1331 Rev 1.0 P 25/68 Jul 2006 **Solomon Systech**

There are four phases to driving an OLED a pixel. In phase 1, the pixel is reset by the segment driver to V_{LSS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command B1h A[3:0] from 1 to 16 DCLK. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, first pre-charge is performed. The pixel is driven to attain the corresponding voltage level V_P from V_{LSS} . The amplitude of V_P can be programmed by the command BBh. The period of phase 2 can be programmed in length from 1 to 16 DCLK by command B1h A[7:4]. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.

In phase 3, the OLED pixel is driven to the targeted driving voltage through second pre-charge. The second pre-charge can control the speed of the charging process. The period of phase 3 can be programmed by commands 8Ah, 8Bh and 8Ch.

Last phase (phase 4) is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs Pulse Width Modulation (PWM) method to control the gray scale of each pixel individually. The wider pulse widths in the current drive stage results in brighter pixels and vice versa. This is shown in the following figure.

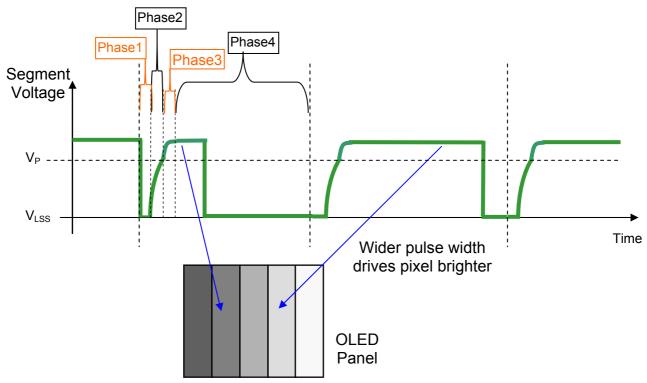


Figure 18 - Gray Scale Control by PWM in Segment

After finishing phase 4, the driver IC will go back to phase 1 to display the next row image data. This four-step cycle is run continuously to refresh image display on OLED panel.

The length of phase 4 is defined by command B8h "Set Gray Scale Table" or B9h "Enable Linear Gray Scale Table". In the table, the gray scale is defined in incremental way, with reference to the length of previous table entry.

Solomon Systech Jul 2006 | P 26/68 | Rev 1.0 | SSD1331

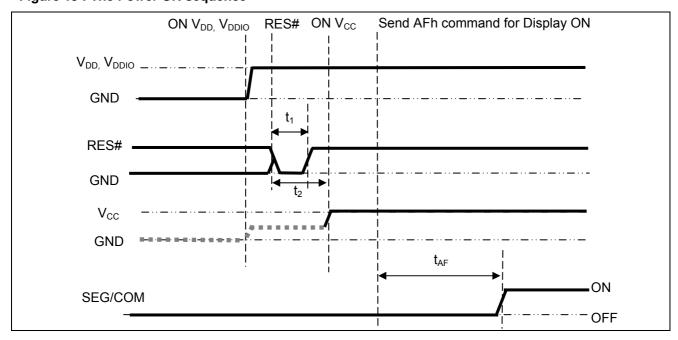
7.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1331 (assume V_{DD} and V_{DDIO} are at the same voltage level).

Power ON sequence:

- 1. Power ON V_{DD}, V_{DDIO},
- 2. After V_{DD}, V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 3us (t₁) and then HIGH (logic high).
- 3. After set RES# pin LOW (logic low), wait for at least 3us (t₂). Then Power ON V_{CC.}⁽¹⁾
- 4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

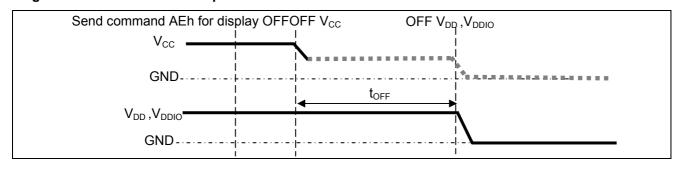
Figure 19: The Power ON sequence



Power OFF sequence:

- 1. Send command AEh for display OFF.
- 2. Power OFF V_{CC} (1), (2)
- 3. Wait for t_{OFF} . Power OFF V_{DD_i} , V_{DDIO_i} (where Minimum t_{OFF} =0ms, Typical t_{OFF} =100ms)

Figure 20: The Power OFF sequence



Note:

SSD1331 | Rev 1.0 | P 27/68 | Jul 2006 | Solomon Systech

⁽¹⁾ Since an ESD protection circuit is connected between V_{DD}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD}, V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 19 and Figure 20 . (2) V_{CC} should be kept float when it is OFF.

8 COMMAND TABLE

Table 10 - Command Table

Fund	undamental Commands /C# Hex D7 D6 D5 D4 D3 D2 D1 D0 Command Description Default											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description	Default
0	15	0	0	0	1	0	1	0	1		Setup Column start and end address	
0	A[6:0]	*	A ₆	A_5	A_4	A ₃	A ₂	A ₁	A ₀		A[6:0] start address from 00d-95d	00d (00h)
0	B[6:0]	*	B ₆	B_5	B ₄	Вз	B ₂	B ₁	B ₀		B[6:0] end address from 00d-95d	95d (5Fh)
										Set Column Address		
0	75	0	1	1	1	0	1	0	1		Setup Row start and end address	
0	A[5:0]	*	*	A_5	A_4	A_3	A ₂	A ₁	A_0		A[5:0] start address from 00d-63d	00d (00h)
0	B[5:0]	*	*	B ₅	B ₄	Вз	B ₂	B ₁	B ₀		B[5:0] end address from 00d-63d	63d (3Fh)
										Set Row Address		
0	81	1	0	0	0	0	0	0	1		Set contrast for all color "A" segment	
	0.							ľ			(Pins:SA0 – SA95)	
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:0] valid range: 00d to 255d	128d (80h)
										Set Contrast for Color "A"		
0	82	1	0	0	0	0	0	1	0		Set contrast for all color "B" segment	
	۸ (7 ۰01	^	^	^	_	_	_	_	_		(Pins:SB0 – SB95).	1004 (006)
0	A[7:0]	Α ₇	A ₆	A ₅	A4	A ₃	A ₂	A ₁	A ₀	Set Contrast for Color "B"	A[7:0] valid range: 00d to 255d	128d (80h)
0	83	1	0	0	0	0	0	1	1		Set contrast for all color "C" segment	
	۸[٦،٥١	٨	٨	٨	٨	٨	_	_	٨		(Pins:SC0 – SC95).	1004 (005)
0	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Set Contrast for Color "C"	A[7:0] valid range: 00d to 255d	128d (80h)
0	87	1	0	0	0	0	1	1	1		Set master current attenuation factor	
0	A[3:0]	0	0	0	0	A ₃	A ₂	A ₁	A ₀		A[3:0] from 00d to 15d corresponding to 1/16, 2/16 to 16/16 attenuation.	15d (0Fh)
										Master Current Control		

 Solomon Systech
 Jul 2006
 P 28/68
 Rev 1.0
 SSD1331

Fund	ndamental Commands C# Hex D7 D6 D5 D4 D3 D2 D1 D0 Command Description Descr											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description	Default
0 0 0 0 0	8A A[7:0] 8B A[7:0] 8C A[7:0]	1 A ₇ 1 A ₇ 1 A ₇	0 A ₆ 0 A ₆ 0 A ₆	0 A ₅ 0	0 A ₄ 0 A ₄ 0 A ₄	1 A ₃ 1 A ₃ 1 A ₃	0 A ₂ 1	1 A ₁ 1 A ₁ 0 A ₁	0 A ₀ 1 A ₀ 0 A ₀	Set Second Pre-charge Speed for Color "A", "B" and "C"	A[7:0]: Set Second Pre-charge Speed Ranges: 0000000b to 1111111b, a higher value of A[7:0] gives a higher Second Pre-charge speed. Note (1) The default values of A[7:0] in 8Ah, A[7:0] in 8Bh and A[7:0] in 8Ch are equal to the contrast values for color A, B and C(refer to commands: 81h, 82h, 83h) respectively. (2) All six bytes (8Ah A[7:0], 8Bh A[7:0] and 8Ch A[7:0]) must be inputted together. For example: the original value is like that Original value 8Ah A[7:0]: 80h 8Ch A[7:0]: 80h 1f it is wanted to change the value of 8Bh A[7:0] to 75h, then all the following 6 bytes must be inputted: 8Ah,80h, 8Bh,75h, 8Ch,80h.	A[7:0] of 81h A[7:0] of 82h A[7:0] of 83h
0 0	A0 A[7:0]	1 A ₇	0 A ₆	1 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁			Set driver remap and color depth A[0]=0, Horizontal address increment A[0]=1, Vertical address increment A[1]=0, RAM Column 0 to 95 maps to Pin Seg (SA,SB,SC) 0 to 95 A[1]=1, RAM Column 0 to 95 maps to Pin Seg (SA,SB,SC) 95 to 0 A[2]=0, normal order SA,SB,SC (e.g. RGB) A[2]=1, reverse order SC,SB,SA (e.g. BGR) A[3]=0, Disable left-right swapping on COM A[3]=1, Set left-right swapping on COM	
											A[4]=0, Scan from COM 0 to COM [N -1] A[4]=1, Scan from COM [N-1] to COM0. Where N is the multiplex ratio. A[5]=0, Disable COM Split Odd Even (RESET) A[5]=1, Enable COM Split Odd Even A[7:6] = 00; 256 color format A[7:6] = 01; 65k color format A[7:6] = 10; 65k color format 2 If 9 / 18 bit mode is selected, color depth will be fixed to 65k regardless of the setting.	A[4]=0 A[5]=0 A[7:6]=01
0	A1 A[5:0]	1	0	1 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Display Start Line	Set display start line register by Row A[5:0]: from 00d to 63d	00d (00h)
0	A2 A[5:0]	1	0	1 A ₅	0 A ₄	0 A ₃	0 A ₂	1 A ₁	0 A ₀	Set Display Offset	Set vertical offset by Com A[5:0]: from 00d to 63d	00d (00h)

SSD1331 Rev 1.0 P 29/68 Jul 2006 **Solomon Systech**

Fund	ndamental Commands											
D/C#	Hex	D7		D5	D4	D3	D2			Command	Description	Default
0 0 0	A4 / A5 / A6 / A7 /	1	0	1	0	0	1	X ₁	X ₀	Set Display Mode	A4h=Normal Display A5h=Entire Display On, all pixels turn on at GS63 A6h=Entire Display Off, all pixels turn off A7h=Inverse Display	A4h
	4.0			4		4	•	_				
0	A8 A[5:0]	0	0	1 A ₅	0 A ₄	1 A ₃	0 A ₂	0 A ₁	0 A ₀	Set Multiplex Ratio	Set MUX ratio to N+1 Mux N = A[5:0] from 15d to 63d A[5:0] from 00d to 14d are invalid entry	63d (3Fh)
0 0 0 0	AB A[7:0] B[7:0] C[7:0] D[7:0] E[4:0]	1 A ₇ B ₇ C ₇ D ₇ 0	B ₆ C ₆		0 A ₄ B ₄ C ₄ D ₄ E ₄	B ₃ C ₃ D ₃	B ₂ C ₂ D ₂	B ₁	C ₀	Dim Mode Setting Set Master Configuration	Configure dim mode setting A[7:0] = Reserved. (Set as 00h) B[7:0] = Contrast setting for Color A, valid range 0 to 255d. C[7:0] = Contrast setting for Color B, valid range 0 to 255d. D[7:0] = Contrast setting for Color C, valid range 0 to 255d. E[4:0] = Precharge voltage setting, valid range 0 to 31d. A[0]=0b, Select external V _{CC} supply A[0]=1b, Reserved (RESET) Note (1) Bit A[0] must be set to 0b after RESET.	A[0] = 1
0	AC AE AF	1	0	1	0	1	1	A ₁	A ₀	Set Display On/Off	(2) The setting will be activated after issuing Set Display ON command (AFh) ACh = Display ON in dim mode AEh = Display off (sleep mode) AFh = Display on in normal mode	AEh
0	B0 A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	0 A ₃	0 A ₂	0 A ₁	0 A ₀	Power Save Mode	A[7:0]=1Ah, Enable Power save mode (RESET) A[7:0]=0Bh, Disable Power save mode	1Ah
0	B1 A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Phase 1 and 2 period adjustment	A[3:0] Phase 1 period in N DCLK. 1~15 DCLK allowed. A[7:4] Phase 2 period in N DCLK. 1~15 DCLK allowed	74h
0	B3 A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	0 A ₃	0 A ₂	1 A ₁	1 A ₀	Display Clock Divider / Oscillator Frequency	A[3:0]: Define the divide ratio (D) of the display clocks (DCLK): Divide ratio (D) = A[3:0] + 1 (i.e., 1 to 16) A[7:4] Fosc frequency. Frequency increases as setting value increases	D0h

 Solomon Systech
 Jul 2006
 P 30/68
 Rev 1.0
 SSD1331

Fund	ndamental Commands											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description	Default
0 0 0 0 0 0	B8 A[6:0] B[6:0] C[6:0] AE[6:0] AF[6:0]			B ₅ C ₅ AE ₅		B ₃ C ₃ AE ₃	B ₂ C ₂ AE ₂	 AE₁	B ₀ C ₀ AE ₀	Set Gray Scale Table	These 32 parameters define pulse widths of GS1 to GS63 in terms of DCLK A[6:0]: Pulse width for GS1, RESET=01d B[6:0]: Pulse width for GS3, RESET=05d C[6:0]: Pulse width for GS5, RESET=09d AE[6:0]: Pulse width for GS61, RESET=121d AF[6:0]: Pulse width for GS63, RESET=125d Note: (1) GS0 has no pre-charge and current drive stages. (2) GS2, GS4GS62 are derived by Pn = (Pn-1+Pn+1)/2 (3) Pn will be truncated to integer if it is with decimal point. (4) Pn+1 should always be set to larger than Pn-1 (5) Max pulse width is 125	
0	В9	1	0	1	1	1	0	0	1	Enable Linear Gray Scale Table	Reset built in gray scale table (Linear) Pulse width for GS1 = 1d; Pulse width for GS2 = 3d; Pulse width for GS3 = 5d; Pulse width for GS61 = 121d; Pulse width for GS62 = 123d; Pulse width for GS63 = 125d.	\
0	BB A[5:0]	1 0	0	1 A ₅	1 A ₄	1 A ₃	0 A ₂	1 A ₁	0	Set Pre-charge level	Set pre-charge voltage level. All three color share the same pre-charge voltage. A[5:1] Hex code pre-charge voltage	3Eh
0	BC-BD	1	0	1	1	1	1	0	X ₀	NOP	Command for No operation	١
0	BE A[5:1]	1 0	0 0	1 A ₅	1 A ₄	1 A ₃	1 A ₂	1 A ₁	0 0	Set V _{COMH}	Set COM deselect voltage level (V COMH) A[5:1] Hex code V COMH 00000 00h 0.44 x V _{CC} 01000 10h 0.52 x V _{CC} 10000 20h 0.61 x V _{CC} 11000 30h 0.71 x V _{CC} 11111 3Eh 0.83 x V _{CC}	3Eh
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No operation	\
0 0	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A ₂	0 1	1 0	Set Command Lock	A[2]: MCU protection status A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [reset] A[2] = 1b, Lock OLED driver IC MCU interface from entering command Note (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command.	12h

SSD1331 Rev 1.0 P 31/68 Jul 2006 **Solomon Systech**

Grap	raphic Acceleration Commands C# Hex D7 D6 D5 D4 D3 D2 D1 D0 Command Description Descrip										
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	21	0	0	1	0	0	0	0	1		A[6:0]: Column Address of Start
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A ₁	A_0		B[5:0]: Row Address of Start
0	B[5:0]	*	*	B ₅	B ₄	B_3	B_2	B ₁	B ₀		C[6:0]: Column Address of End
0	C[6:0]	*	C_6	C_5	C ₄	C_3	C_2	C ₁	Co		D[5:0]: Row Address of End
0	D[5:0]	*	*	D_5	D_4	D_3	D_2	D ₁	D_0	Draw Line	E[5:1]: Color C of the line
0	E[5:1]	*	*	E ₅				Εı	*		F[5:0]: Color B of the line
0	F[5:0]	*	*	F_5					F_0		G[5:1]: Color A of the line
0	G[5:1]	*	*	_					*		G[5.1]. Color A of the line
0	22	0	0	1	0	0	0	1	0		A[6:0]: Column Address of Start
0	A[6:0]	*	A ₆	A ₅	A_4	A ₃	A_2	A ₁	A ₀		B[5:0]: Row Address of Start
0	B[5:0]	*	*	B ₅	B ₄	B ₃			B ₀		C[6:0]: Column Address of End
0	C[6:0]	*	C ₆	C ₅	C ₄	C ₃			C ₀		D[5:0]: Row Address of End
0	D[5:0]	*	*	D ₅	D ₄	D_3			D_0		E[5:1]: Color C of the line
0	E[5:1]	*	*	E ₅	E ₄	E ₃			*	Drawing	F[5:0]: Color B of the line
0	F[5:0]	*	*	F ₅	F ₄	F ₃			Fo	Rectangle	G[5:1]: Color A of the line
0	G[5:1]	*	*	G ₅	G ₄	G ₃			*		H[5:1]: Color C of the fill area
0	H[5:1]	*	*	H ₅	H ₄	H ₃			*		I[5:0]: Color B of the fill area
	I[5:0]	*	*	١.	_				10		-
0		*	*	l ₅	l ₄	l ₃	l ₂	l ₁	*		J[5:1]: Color A of the fill area
	J[5:1]			J ₅	J ₄	J ₃	J ₂	J ₁			AFOOD Column Address of Otto
0	23	0	0	1	0	0	0	1	1		A[6:0]: Column Address of Start
0	A[6:0]	*	A ₆	A ₅	A ₄	A ₃			A ₀		B[5:0]: Row Address of Start
0	B[5:0]	*	*	B ₅	B ₄	B ₃			B ₀		C[6:0]: Column Address of End
0	C[6:0]	*	C ₆	C ₅	C ₄	C ₃			C ₀	Сору	D[5:0]: Row Address of End
0	D[5:0]	*	*	D ₅	D ₄	D ₃	D ₂		D ₀		E[6:0]: Column Address of New Start
0	E[6:0]	*	E ₆	E ₅	E ₄	E ₃	E ₂		E ₀		F[5:0]: Row Address of New Start
0	F[5:0]	*	*	F ₅	F ₄	F ₃	F ₂	F ₁	F ₀		
0	24	0	0	1	0	0	1	0	0		A[6:0]: Column Address of Start
0	A[6:0]	*	A_6	A_5		A_3	A_2	A ₁	A_0		B[5:0]: Row Address of Start
0	B[5:0]	*	*	B_5	B ₄	B ₃	B ₂	B ₁	B_0		C[6:0]: Column Address of End
0	C[6:0]	*	C ₆	C_5	C ₄	C_3	C_2	C ₁	C_0		D[5:0]: Row Address of End
0	D[5:0]	*	*	D_5	D ₄	D_3	D_2	D ₁	D_0	Dim Window	The effect of dim window:
										Dim Window	GS15~GS0 no change
											GS19~GS16 become GS4
											GS23~GS20 become GS5
											GS63~GS60 become GS15
0	25	0	0	1	0	0	1	0	1		A[6:0]: Column Address of Start
0	A[6:0]	*	A ₆	A ₅	A ₄	A ₃	A_2	A ₁	A ₀		B[5:0]: Row Address of Start
0	B[5:0]	*	*	B ₅	B ₄	B ₃			B ₀		C[6:0]: Column Address of End
0	C[6:0]	*	C ₆	C ₅	C ₄	C ₃			C ₀		D[5:0]: Row Address of End
0	D[5:0]	*	*	D ₅	D ₄	D ₃		D ₁	D_0		
0	26	0	0	1	0	0	1	1	0		A0 0 : Disable Fill for Draw Rectangle
								-			Command (RESET)
0	A[4:0]	*	*	*	A_4	0	0	0	A_0		1 : Enable Fill for Draw Rectangle
										Fill Enable /	Command A[3:1] 000: Reserved values
										Disable	A4 0 : Disable reverse copy (RESET)
											1 : Enable reverse during copy
											command.

 Solomon Systech
 Jul 2006
 P 32/68
 Rev 1.0
 SSD1331

Grap	hic Acce	elera	ation	ı Co	mm	nanc	ls				
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	27 A[6:0]	0	0 A ₆	1 A ₅	0 A ₄	0 A ₃	1 A ₂	1 A ₁	1 A ₀		A[6:0]: Set number of column as horizontal scroll offset Range: 0d-95d (no horizontal scroll if
0	B[5:0]	*	*	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		equals to 0) B[5:0]: Define start row address
0	C[6:0]	*	C ₆	C ₅	C ₄	Сз	C ₂	C ₁	C ₀		C[6:0]: Set number of rows to be horizontal scrolled B[5:0]+C[6:0] <=64
0	D[5:0]	*	*	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Continuous	D[5:0]: Set number of row as vertical scroll offset Range: 0d-63d (no vertical scroll if equals to 0)
0	E[1:0]	*	*	*	*	*	*	E ₁	E ₀	Horizontal & Vertical Scrolling Setup	E[1:0]: Set time interval between each scroll step 00b 6 frames 01b 10 frames 10b 100 frames 11b 200 frames
											Note: (1) Vertical scroll is run with 64MUX setting only (2) The parameters should not be changed after scrolling is activated
0	2E	0	0	1	0	1	1	1	0	Deactivate scrolling	This command deactivates the scrolling action. Note (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Activate scrolling	This command activates the scrolling function according to the setting done by Continuous Horizontal & Vertical Scrolling Setup command 27h.

 SSD1331
 Rev 1.0
 P 33/68
 Jul 2006
 Solomon Systech

8.1 Data Read / Write

To read data from the GDDRAM, input HIGH to R/W#(WR#)# pin and D/C# pin for 6800-series parallel mode, LOW to E (RD#) pin and HIGH to D/C# pin for 8080-series parallel mode. No data read is provided in serial mode operation.

In normal data read mode, GDDRAM column address pointer will be increased by one automatically after each data read.

Also, a dummy read is required before the first data read.

To write data to the GDDRAM, input LOW to R/W#(WR#) pin and HIGH to D/C# pin for 6800-series parallel mode AND 8080-series parallel mode. For serial interface mode, it is always in write mode. GDDRAM column address pointer will be increased by one automatically after each data write.

Table 11 - Address increment table (Automatic)

D/C#	R/W#(WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

Solomon Systech Jul 2006 | P 34/68 | Rev 1.0 | SSD1331

9 COMMAND DESCRIPTIONS

9.1 Fundamental Command

9.1.1 Set Column Address (15h)

This command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address.

9.1.2 **Set Row Address (75h)**

This command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

The figure below shows the way of column and row address pointer movement through the example: column start address is set to 2 and column end address is set to 93, row start address is set to 1 and row end address is set to 62. Horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 93 and from row 1 to row 62 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line in* Figure 21). Whenever the column address pointer finishes accessing the end column 93, it is reset back to column 2 and row address is automatically increased by 1 (*solid line in* Figure 21). While the end row 62 and end column 93 RAM location is accessed, the row address is reset back to 1 (*dotted line in* Figure 21).

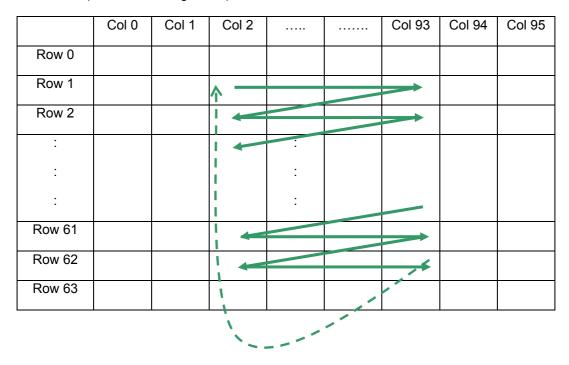


Figure 21 - Example of Column and Row Address Pointer Movement

SSD1331 | Rev 1.0 | P 35/68 | Jul 2006 | Solomon Systech

9.1.3 Set Contrast for Color A, B, C (81h, 82h, 83h)

This command is to set Contrast Setting of each color A, B and C. The chip has three contrast control circuits for color A, B and C. Each contrast circuit has 256 contrast steps from 00h to FFh. The segment output current I_{SEG} increases linearly with the contrast step, which results in brighter of the color. This relation is shown in Figure 22.

9.1.4 Master Current Control (87h)

This command is to control the segment output current by a scaling factor. This factor is common to color A, B and C. The chip has 16 master control steps. The factor is ranged from 1 [0000b] to 16 [1111b]. RESET is 16 [1111b]. The smaller the master current value, the dimmer the OLED panel display is set. For example, if original segment output current of a color is 160uA at scale factor = 16, setting scale factor to 8 to reduce the current to 80uA. Please see Figure 22.

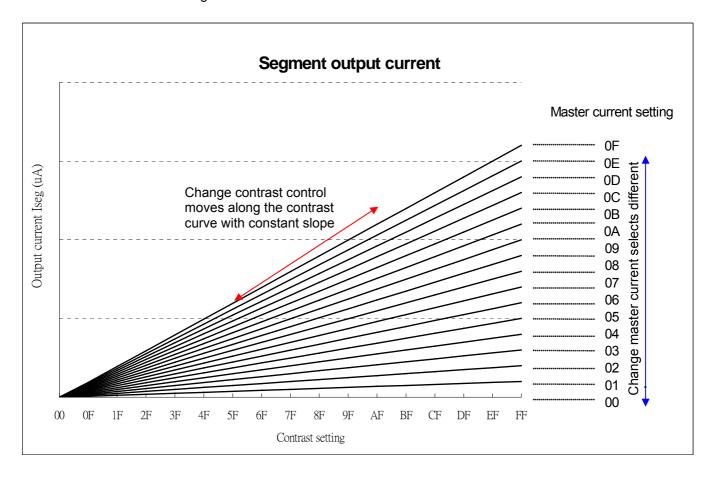


Figure 22 - Segment Output Current for Different Contrast Control and Master Current Setting

Solomon Systech Jul 2006 | P 36/68 | Rev 1.0 | SSD1331

9.1.5 Set Second Pre-charge Speed for Color A, B, C (8Ah)

The value set should match with the contrast of the color A, B, C. An initial trial should be the value same as the contrast A, B, C. When faster speed is needed, higher value can be set and vice versa. Figure 23 shows the effect of setting second pre-charge under different speeds through using command 8Ah, 8Bh and 8Ch.

Second Pre-charge speed = 255

Phase2

Phase3

Phase3

Phase3

Phase3

Phase4

Phase4

Phase4

Phase4

Phase5

Phase5

Phase6

Phase7

Phase6

Phase6

Phase6

Phase6

Phase6

Phase6

Phase7

Phase7

Phase6

Phase6

Phase6

Phase6

Phase6

Phase7

Phase6

Phase6

Phase6

Phase7

Phase6

Phase6

Phase6

Phase7

Phase8

Figure 23 - Effect of setting the second pre-charge under different speeds

9.1.6 Set Re-map & Data Format (A0h)

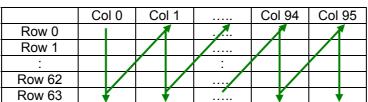
This command has multiple configurations and each bit setting is described as follows.

Address increment mode (A[0])
When it is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 24.

Figure 24 - Address Pointer Movement of Horizontal Address Increment Mode

When A[0] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read/written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 25.

Figure 25 - Address Pointer Movement of Vertical Address Increment Mode

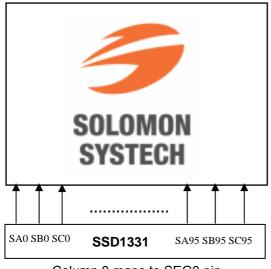


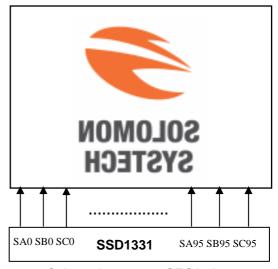
SSD1331 | Rev 1.0 | P 37/68 | Jul 2006 | Solomon Systech

Column Address Mapping (A[1])

This command bit is made for flexible layout of segment signals in OLED module with segment arranged from left to right or vice versa. The display direction is either mapping display data RAM column 0 to SEG0 pin (A[1] = 0), or mapping display data RAM column 95 to SEG0 pin (A[1] = 1). The effects of both are shown in Figure 26.

Figure 26 - Example of Column Address Mapping





Column 0 maps to SEG0 pin

Column 95 maps to SEG0 pin

RGB Mapping (A[2])

This command bit is made for flexible layout of segment signals in OLED module to match filter design.

COM Left / Right Remap (A[3])

This command bit is made for flexible layout of common signals in OLED module with COM0 arranged on either left or right side. Details of pin arrangement can be found in Table 12 and Figure 27.

COM Scan Direction Remap (A[4])

This bit determines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down or vice versa. Details of pin arrangement can be found in Table 12 and Figure 27.

Odd Even Split of COM pins (A[5])

This bit can set the odd even arrangement of COM pins.

A[5] = 0: Disable COM split odd even, pin assignment of common is in sequential as COM63 COM62 COM 33 COM32..SC95..SA0..COM0 COM1.... COM30 COM31

A[5] = 1: Enable COM split odd even, pin assignment of common is in odd even split as COM63 COM61.... COM3 COM1..SC95..SA0..COM0 COM2.... COM60 COM62 Details of pin arrangement can be found in Table 12 and Figure 27.

Display color mode (A[7:6])

Select either 65k or 256 color mode. The display RAM data format in different mode is described in section 7.5

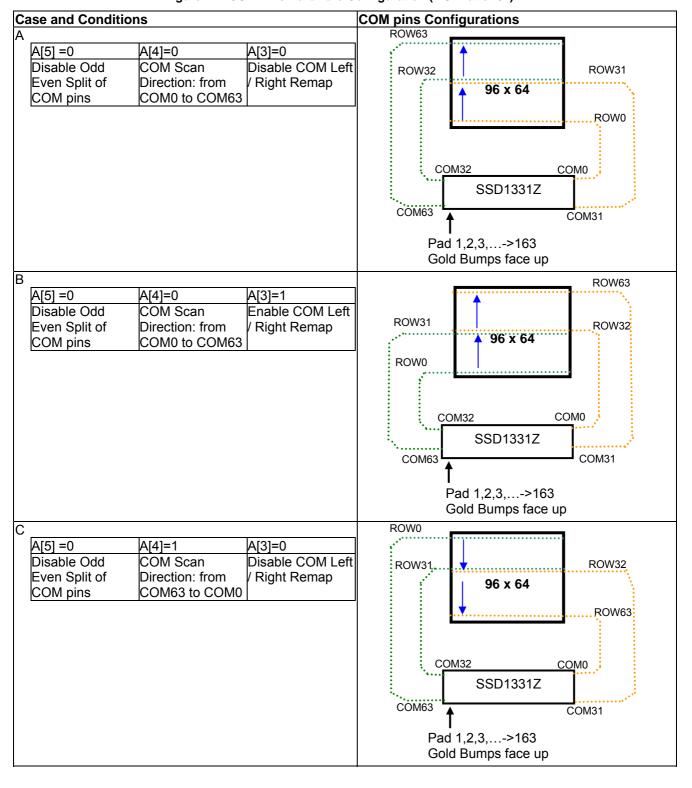
Solomon Systech Jul 2006 | P 38/68 | Rev 1.0 | SSD1331

Table 12 - Illustration of different COM output settings

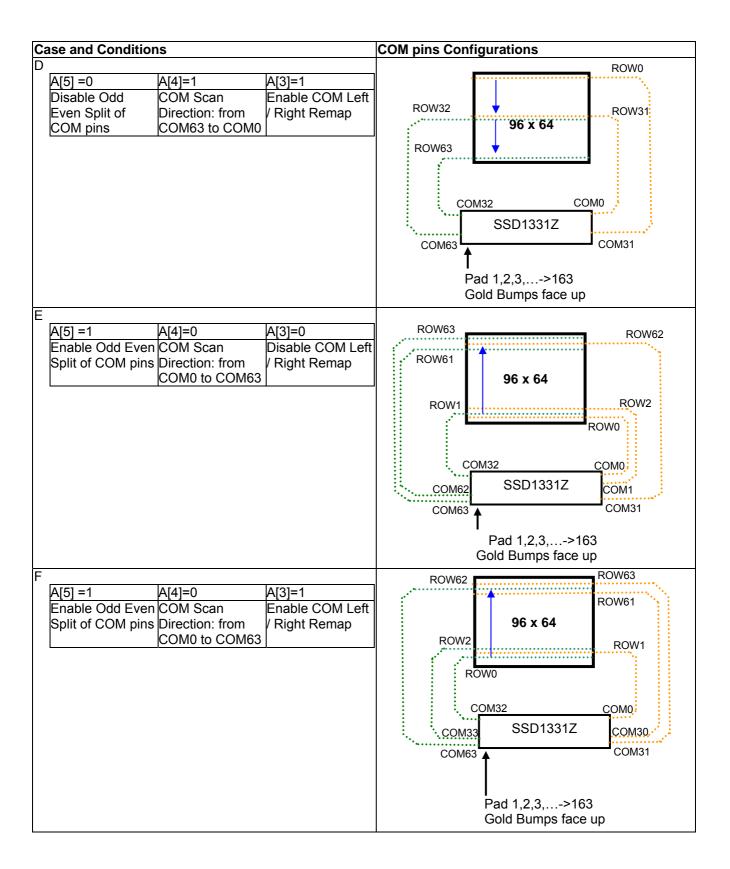
		Case A	Case B	Case C	Case D	Case E	Case F	Case G	Case H
		A[5:3]=000	A[5:3]=001	A[5:3]=010	A[5:3]=011	A[5:3]=100	A[5:3]=101	A[5:3]=110	A[5:3]=111
IC Pad no.	Pin name				Output	t signal			
195	COM0	Row0	Row32	Row63	Row31	Row0	Row1	Row63	Row62
194	COM1	Row1	Row33	Row62	Row30	Row2	Row3	Row61	Row60
193	COM2	Row2	Row34	Row61	Row29	Row4	Row5	Row59	Row58
192	СОМ3	Row3	Row35	Row60	Row28	Row6	Row7	Row57	Row56
191	COM4	Row4	Row36	Row59	Row27	Row8	Row9	Row55	Row54
190	COM5	Row5	Row37	Row58	Row26	Row10	Row11	Row53	Row52
169	COM26	Row26	Row58	Row37	Row5	Row52	Row53	Row11	Row10
168	COM27	Row27	Row59	Row36	Row4	Row54	Row55	Row9	Row8
167	COM28	Row28	Row60	Row35	Row3	Row56	Row57	Row7	Row6
166	COM29	Row29	Row61	Row34	Row2	Row58	Row59	Row5	Row4
165	COM30	Row30	Row62	Row33	Row1	Row60	Row61	Row3	Row2
164	COM31	Row31	Row63	Row32	Row0	Row62	Row63	Row1	Row0
488	COM32	Row32	Row0	Row31	Row63	Row1	Row0	Row62	Row63
489	COM33	Row33	Row1	Row30	Row62	Row3	Row2	Row60	Row61
490	COM34	Row34	Row2	Row29	Row61	Row5	Row4	Row58	Row59
491	COM35	Row35	Row3	Row28	Row60	Row7	Row6	Row56	Row57
492	COM36	Row36	Row4	Row27	Row59	Row9	Row8	Row54	Row55
493	COM37	Row37	Row5	Row26	Row58	Row11	Row10	Row52	Row53
514	COM58	Row58	Row26	Row5	Row37	Row53	Row52	Row10	Row11
515	COM59	Row59	Row27	Row4	Row36	Row55	Row54	Row8	Row9
516	COM60	Row60	Row28	Row3	Row35	Row57	Row56	Row6	Row7
517	COM61	Row61	Row29	Row2	Row34	Row59	Row58	Row4	Row5
518	COM62	Row62	Row30	Row1	Row33	Row61	Row60	Row2	Row3
519	COM63	Row63	Row31	Row0	Row32	Row63	Row62	Row0	Row1

SSD1331 Rev 1.0 P 39/68 Jul 2006 **Solomon Systech**

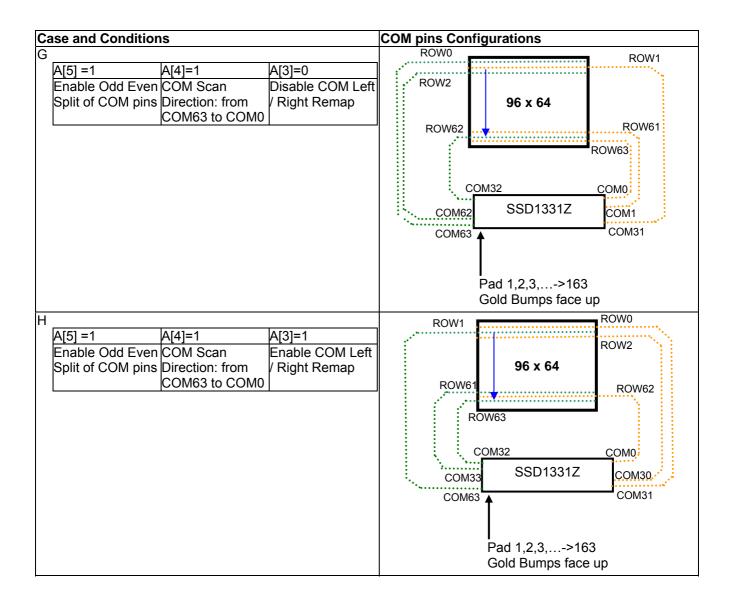
Figure 27 - COM Pins Hardware Configuration (MUX ratio: 64)



Solomon Systech Jul 2006 | P 40/68 | Rev 1.0 | SSD1331



SSD1331 | Rev 1.0 | P 41/68 | Jul 2006 | **Solomon Systech**



9.1.7 Set Display Start Line (A1h)

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 63. Table 13 and Table 14 show examples of this command. In there, "Row" means the graphic display data RAM row.

9.1.8 Set Display Offset (A2h)

This command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-63. For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second command should be given by 0010000b. Table 13 and Table 14 show examples of this command. In there, "Row" means the graphic display data RAM row.

Solomon Systech Jul 2006 P 42/68 Rev 1.0 SSD1331

Table 13 - Example of Set Display Offset and Display Start Line with no Remap

	-	4		i4		4	itput 5	56		56	,	56	Set MUX ratio(A8h)
ŀ)))		0		0		0	COM Scan Direction Rem
lardware pin)		3)		0		8		0	Display offset (A2h)
name COM0	Row0	RAM0	Row8	RAM8	Row0	RAM8	Row0	0 RAM0	Row8	0 RAM8	Row0	8 RAM8	Display start line (A1h)
COM1	Row1	RAM1	Row9	RAM9	Row1	RAM9	Row1	RAM1	Row9	RAM9	Row1	RAM9	
COM2 COM3	Row2 Row3	RAM2 RAM3	Row10 Row11	RAM10 RAM11	Row2 Row3	RAM10 RAM11	Row2	RAM2 RAM3	Row10	RAM10 RAM11	Row2 Row3	RAM10 RAM11	
COM3 COM4	Row4	RAM4	Row12	RAM12	Row4	RAM12	Row3 Row4	RAM4	Row11 Row12	RAM12	Row4	RAM12	
COM5	Row5	RAM5	Row13	RAM13	Row5	RAM13	Row5	RAM5	Row13	RAM13	Row5	RAM13	
COM6	Row6	RAM6	Row14	RAM14	Row6	RAM14	Row6	RAM6	Row14	RAM14	Row6	RAM14	
COM7 COM8	Row7 Row8	RAM7 RAM8	Row15 Row16	RAM15 RAM16	Row7 Row8	RAM15 RAM16	Row7 Row8	RAM7 RAM8	Row15 Row16	RAM15 RAM16	Row7 Row8	RAM15 RAM16	
COM9	Row9	RAM9	Row17	RAM17	Row9	RAM17	Row9	RAM9	Row17	RAM17	Row9	RAM17	
COM10	Row10	RAM10	Row18	RAM18	Row10	RAM18	Row10	RAM10	Row18	RAM18	Row10	RAM18	
COM11 COM12	Row11 Row12	RAM11 RAM12	Row19 Row20	RAM19 RAM20	Row11 Row12	RAM19 RAM20	Row11 Row12	RAM11 RAM12	Row19 Row20	RAM19 RAM20	Row11 Row12	RAM19 RAM20	
COM13	Row13	RAM13	Row21	RAM21	Row13	RAM21	Row13	RAM13	Row21	RAM21	Row13	RAM21	
COM14 COM15	Row14	RAM14	Row22	RAM22	Row14	RAM22	Row14	RAM14	Row22	RAM22	Row14	RAM22	
COM15 COM16	Row15 Row16	RAM15 RAM16	Row23 Row24	RAM23 RAM24	Row15 Row16	RAM23 RAM24	Row15 Row16	RAM15 RAM16	Row23 Row24	RAM23 RAM24	Row15 Row16	RAM23 RAM24	
COM17	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row17	RAM17	Row25	RAM25	Row17	RAM25	
COM18	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row18	RAM18	Row26	RAM26	Row18	RAM26	
COM19 COM20	Row19 Row20	RAM19 RAM20	Row27 Row28	RAM27 RAM28	Row19 Row20	RAM27 RAM28	Row19 Row20	RAM19 RAM20	Row27 Row28	RAM27 RAM28	Row19 Row20	RAM27 RAM28	
COM21	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row21	RAM21	Row29	RAM29	Row21	RAM29	
COM22	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row22	RAM22	Row30	RAM30	Row22	RAM30	
COM23 COM24	Row23 Row24	RAM23 RAM24	Row31 Row32	RAM31 RAM32	Row23 Row24	RAM31 RAM32	Row23 Row24	RAM23 RAM24	Row31 Row32	RAM31 RAM32	Row23 Row24	RAM31 RAM32	
COM25	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row25	RAM25	Row33	RAM33	Row25	RAM33	
COM26	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row26	RAM26	Row34	RAM34	Row26	RAM34	
COM27 COM28	Row27 Row28	RAM27 RAM28	Row35 Row36	RAM35 RAM36	Row27 Row28	RAM35 RAM36	Row27 Row28	RAM27 RAM28	Row35 Row36	RAM35 RAM36	Row27 Row28	RAM35 RAM36	
COM29	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row29	RAM29	Row37	RAM37	Row29	RAM37	
COM30 COM31	Row30 Row31	RAM30 RAM31	Row38 Row39	RAM38 RAM39	Row30 Row31	RAM38 RAM39	Row30 Row31	RAM30 RAM31	Row38 Row39	RAM38 RAM39	Row30 Row31	RAM38	
COM31 COM32	Row31	RAM31 RAM32	Row40	RAM39 RAM40	Row31 Row32	RAM40	Row31 Row32	RAM31	Row40	RAM39 RAM40	Row31 Row32	RAM39 RAM40	
COM33	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row33	RAM33	Row41	RAM41	Row33	RAM41	
COM34 COM35	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row34	RAM34	Row42	RAM42	Row34	RAM42	
COM35	Row35 Row36	RAM35 RAM36	Row43 Row44	RAM43 RAM44	Row35 Row36	RAM43 RAM44	Row35 Row36	RAM35 RAM36	Row43 Row44	RAM43 RAM44	Row35 Row36	RAM43 RAM44	
COM37	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row37	RAM37	Row45	RAM45	Row37	RAM45	
COM38	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row38	RAM38	Row46	RAM46	Row38	RAM46	
COM39 COM40	Row39 Row40	RAM39 RAM40	Row47 Row48	RAM47 RAM48	Row39 Row40	RAM47 RAM48	Row39 Row40	RAM39 RAM40	Row47 Row48	RAM47 RAM48	Row39 Row40	RAM47 RAM48	
COM41	Row41	RAM41	Row49	RAM49	Row41	RAM49	Row41	RAM41	Row49	RAM49	Row41	RAM49	
COM42	Row42	RAM42	Row50	RAM50	Row42	RAM50	Row42	RAM42	Row50	RAM50	Row42	RAM50	
COM43 COM44	Row43 Row44	RAM43 RAM44	Row51 Row52	RAM51 RAM52	Row43 Row44	RAM51 RAM52	Row43 Row44	RAM43 RAM44	Row51 Row52	RAM51 RAM52	Row43 Row44	RAM51 RAM52	
COM45	Row45	RAM45	Row53	RAM53	Row45	RAM53	Row45	RAM45	Row53	RAM53	Row45	RAM53	
COM46 COM47	Row46 Row47	RAM46 RAM47	Row54 Row55	RAM54 RAM55	Row46 Row47	RAM54 RAM55	Row46 Row47	RAM46 RAM47	Row54 Row55	RAM54 RAM55	Row46 Row47	RAM54 RAM55	
COM48	Row48	RAM48	Row56	RAM56	Row48	RAM56	Row48	RAM48		-	Row48	RAM56	
COM49	Row49	RAM49	Row57	RAM57	Row49	RAM57	Row49	RAM49	-	-	Row49	RAM57	
COM50 COM51	Row50 Row51	RAM50 RAM51	Row58 Row59	RAM58 RAM59	Row50 Row51	RAM58 RAM59	Row50 Row51	RAM50 RAM51	_	-	Row50 Row51	RAM58 RAM59	
COM51	Row52	RAM52	Row60	RAM60	Row52	RAM60	Row52	RAM52	-	-	Row52	RAM60	
COM53	Row53	RAM53	Row61	RAM61	Row53	RAM61	Row53	RAM53	-	-	Row53	RAM61	
COM54 COM55	Row54 Row55	RAM54 RAM55	Row62 Row63	RAM62 RAM63	Row54 Row55	RAM62 RAM63	Row54 Row55	RAM54 RAM55	-	-	Row54 Row55	RAM62 RAM63	
COM56	Row56	RAM56	Row03	RAM0	Row56	RAM0	-	-	Row0	RAM0	-	-	
COM57	Row57	RAM57	Row1	RAM1	Row57	RAM1	-	-	Row1	RAM1	-	-	
COM58 COM59	Row58 Row59	RAM58 RAM59	Row2 Row3	RAM2 RAM3	Row58 Row59	RAM2 RAM3	-	-	Row2 Row3	RAM2 RAM3	-	-	
COM60	Row60	RAM60	Row4	RAM4	Row60	RAM4	-	-	Row4	RAM4	-	-	
COM61	Row61	RAM61	Row5	RAM5	Row61	RAM5	-	-	Row5	RAM5	-	-	
COM62 COM63	Row62 Row63	RAM62 RAM63	Row6 Row7	RAM6 RAM7	Row62 Row63	RAM6 RAM7	-	-	Row6 Row7	RAM6 RAM7	-	-	
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SSD1331 Rev 1.0 P 43/68 Jul 2006 **Solomon Systech**

Table 14 - Example of Set Display Offset and Display Start Line with Remap

	6	4	6	4		i4		tput I8		18	4	-8		18	Set MUX ratio(A8h)
			6			1		1		1	4			1	COM Scan Direction Remap (A
Hardw are	(8			0		0		8		0		8	Display offset (A2h)
pin name	((8		0		0		8		16	Display start line (A1h)
COM0	Row 63	RAM63	Row 7	RAM7	Row 63	RAM7	Row 47	RAM47	-	-	Row 47	RAM7	-	-	
COM1	Row 62	RAM62	Row 6	RAM6	Row 62	RAM6	Row 46	RAM46	-	-	Row 46	RAM6	-	-	
COM2	Row 61	RAM61	Row 5	RAM5	Row 61	RAM5	Row 45	RAM45	-	-	Row 45	RAM5	-	-	
COM3	Row 60	RAM60	Row 4	RAM4	Row 60	RAM4	Row 44	RAM44	-	-	Row 44	RAM4	-	-	
COM4	Row 59	RAM59	Row 3	RAM3	Row 59	RAM3	Row 43	RAM43	-	-	Row 43	RAM3	-	-	
COM5	Row 58	RAM58	Row 2	RAM2	Row 58	RAM2	Row 42	RAM42	-	-	Row 42	RAM2	-	-	
COM6	Row 57	RAM57	Row 1	RAM1	Row 57	RAM1	Row 41	RAM41	-	-	Row 41	RAM1	-	-	
COM7 COM8	Row 56 Row 55	RAM56 RAM55	Row 0 Row 63	RAM0 RAM63	Row 56 Row 55	RAM0 RAM63	Row 40 Row 39	RAM40 RAM39	- Row 47	RAM47	Row 40 Row 39	RAM0 RAM47	- Row 47	RAM63	
COM9	Row 54	RAM54	Row 62	RAM62	Row 54	RAM62	Row 38	RAM38	Row 46	RAM46	Row 38	RAM46	Row 46	RAM62	
COM10	Row 53	RAM53	Row 61	RAM61	Row 53	RAM61	Row 37	RAM37	Row 45	RAM45	Row 37	RAM45	Row 45	RAM61	
COM11	Row 52	RAM52	Row 60	RAM60	Row 52	RAM60	Row 36	RAM36	Row 44	RAM44	Row 36	RAM44	Row 44	RAM60	
COM12	Row 51	RAM51	Row 59	RAM59	Row 51	RAM59	Row 35	RAM35	Row 43	RAM43	Row 35	RAM43	Row 43	RAM59	
COM13	Row 50	RAM50	Row 58	RAM58	Row 50	RAM58	Row 34	RAM34	Row 42	RAM42	Row 34	RAM42	Row 42	RAM58	
COM14	Row 49	RAM49	Row 57	RAM57	Row 49	RAM57	Row 33	RAM33	Row 41	RAM41	Row 33	RAM41	Row 41	RAM57	
COM15	Row 48	RAM48	Row 56	RAM56	Row 48	RAM56	Row 32	RAM32	Row 40	RAM40	Row 32	RAM40	Row 40	RAM56	
COM16	Row 47	RAM47	Row 55	RAM55	Row 47	RAM55	Row 31	RAM31	Row 39	RAM39	Row 31	RAM39	Row 39	RAM55	
COM17	Row 46	RAM46	Row 54	RAM54	Row 46	RAM54	Row 30	RAM30	Row 38	RAM38	Row 30	RAM38	Row 38	RAM54	
COM18 COM19	Row 45 Row 44	RAM45 RAM44	Row 53 Row 52	RAM53 RAM52	Row 45 Row 44	RAM53 RAM52	Row 29 Row 28	RAM29 RAM28	Row 37 Row 36	RAM37 RAM36	Row 29 Row 28	RAM37 RAM36	Row 37 Row 36	RAM53 RAM52	
COM20	Row 43	RAM43	Row 52	RAM51	Row 43	RAM51	Row 27	RAM27	Row 35	RAM35	Row 27	RAM35	Row 35	RAM51	
COM21	Row 42	RAM42	Row 50	RAM50	Row 42	RAM50	Row 26	RAM26	Row 34	RAM34	Row 26	RAM34	Row 34	RAM50	
COM22	Row 41	RAM41	Row 49	RAM49	Row 41	RAM49	Row 25	RAM25	Row 33	RAM33	Row 25	RAM33	Row 33	RAM49	
COM23	Row 40	RAM40	Row 48	RAM48	Row 40	RAM48	Row 24	RAM24	Row 32	RAM32	Row 24	RAM32	Row 32	RAM48	
COM24	Row 39	RAM39	Row 47	RAM47	Row 39	RAM47	Row 23	RAM23	Row 31	RAM31	Row 23	RAM31	Row 31	RAM47	
COM25	Row 38	RAM38	Row 46	RAM46	Row 38	RAM46	Row 22	RAM22	Row 30	RAM30	Row 22	RAM30	Row 30	RAM46	
COM26	Row 37	RAM37	Row 45	RAM45	Row 37	RAM45	Row 21	RAM21	Row 29	RAM29	Row 21	RAM29	Row 29	RAM45	
COM27	Row 36	RAM36	Row 44	RAM44	Row 36	RAM44	Row 20	RAM20	Row 28	RAM28	Row 20	RAM28	Row 28	RAM44	
COM28	Row 35	RAM35	Row 43	RAM43	Row 35	RAM43	Row 19	RAM19	Row 27	RAM27	Row 19	RAM27	Row 27	RAM43	
COM29	Row 34	RAM34	Row 42	RAM42	Row 34	RAM42	Row 18	RAM18	Row 26	RAM26	Row 18	RAM26	Row 26	RAM42	
COM30	Row 33	RAM33	Row 41	RAM41	Row 33	RAM41	Row 17	RAM17	Row 25	RAM25	Row 17	RAM25	Row 25	RAM41	
COM31 COM32	Row 32 Row 31	RAM32 RAM31	Row 40 Row 39	RAM40 RAM39	Row 32 Row 31	RAM40 RAM39	Row 16 Row 15	RAM16 RAM15	Row 24 Row 23	RAM24 RAM23	Row 16 Row 15	RAM24 RAM23	Row 24 Row 23	RAM40 RAM39	
COM33	Row 30	RAM30	Row 38	RAM38	Row 30	RAM38	Row 13	RAM14	Row 22	RAM22	Row 14	RAM22	Row 22	RAM38	
COM34	Row 29	RAM29	Row 37	RAM37	Row 29	RAM37	Row 13	RAM13	Row 21	RAM21	Row 13	RAM21	Row 21	RAM37	
COM35	Row 28	RAM28	Row 36	RAM36	Row 28	RAM36	Row 12	RAM12	Row 20	RAM20	Row 12	RAM20	Row 20	RAM36	
COM36	Row 27	RAM27	Row 35	RAM35	Row 27	RAM35	Row 11	RAM11	Row 19	RAM19	Row 11	RAM19	Row 19	RAM35	
COM37	Row 26	RAM26	Row 34	RAM34	Row 26	RAM34	Row 10	RAM10	Row 18	RAM18	Row 10	RAM18	Row 18	RAM34	
COM38	Row 25	RAM25	Row 33	RAM33	Row 25	RAM33	Row 9	RAM9	Row 17	RAM17	Row 9	RAM17	Row 17	RAM33	
COM39	Row 24	RAM24	Row 32	RAM32	Row 24	RAM32	Row 8	RAM8	Row 16	RAM16	Row 8	RAM16	Row 16	RAM32	
COM40	Row 23	RAM23	Row 31	RAM31	Row 23	RAM31	Row 7	RAM7	Row 15	RAM15	Row 7	RAM15	Row 15	RAM31	
COM41	Row 22	RAM22	Row 30	RAM30	Row 22	RAM30	Row 6	RAM6	Row 14	RAM14	Row 6	RAM14	Row 14	RAM30	
COM42	Row 21	RAM21	Row 29	RAM29	Row 21	RAM29	Row 5	RAM5	Row 13	RAM13	Row 5	RAM13	Row 13	RAM29	
COM43	Row 20	RAM20	Row 28	RAM28	Row 20	RAM28	Row 4	RAM4	Row 12	RAM12	Row 4	RAM12	Row 12	RAM28	
COM44 COM45	Row 19	RAM19	Row 27	RAM27 RAM26	Row 19	RAM27 RAM26	Row 3	RAM3 RAM2	Row 11	RAM11 RAM10	Row 3	RAM11 RAM10	Row 11	RAM27 RAM26	
COM46	Row 18 Row 17	RAM18 RAM17	Row 26 Row 25	RAM25	Row 18 Row 17	RAM25	Row 2 Row 1	RAM1	Row 10 Row 9	RAM9	Row 2 Row 1	RAM9	Row 9	RAM25	
COM47	Row 16	RAM16	Row 24	RAM24	Row 16	RAM24	Row 0	RAM0	Row 8	RAM8	Row 0	RAM8	Row 8	RAM24	
COM48	Row 15	RAM15	Row 23	RAM23	Row 15	RAM23	-	-	Row 7	RAM7	-	-	Row 7	RAM23	
COM49	Row 14	RAM14	Row 22	RAM22	Row 14	RAM22	-	-	Row 6	RAM6	-	-	Row 6	RAM22	
COM50	Row 13	RAM13	Row 21	RAM21	Row 13	RAM21	-	-	Row 5	RAM5	-	-	Row 5	RAM21	
COM51	Row 12	RAM12	Row 20	RAM20	Row 12	RAM20	-	-	Row 4	RAM4	-	-	Row 4	RAM20	
COM52	Row 11	RAM11	Row 19	RAM19	Row 11	RAM19	-	-	Row 3	RAM3	-	-	Row 3	RAM19	
COM53	Row 10	RAM10	Row 18	RAM18	Row 10	RAM18	-	-	Row 2	RAM2	-	-	Row 2	RAM18	
COM54	Row 9	RAM9	Row 17	RAM17	Row 9	RAM17	-	-	Row 1	RAM1	-	-	Row 1	RAM17	
COM55	Row 8	RAM8	Row 16	RAM16	Row 8	RAM16	-	-	Row 0	RAM0	-	-	Row 0	RAM16	
COM56 COM57	Row 6	RAM7	Row 15	RAM15 RAM14	Row 7 Row 6	RAM15 RAM14	-	-	-	-	-	-	-	-	
COM57 COM58	Row 6 Row 5	RAM6 RAM5	Row 14 Row 13	RAM14 RAM13	Row 5	RAM14 RAM13	-	-	-	-	-	-	-	-	
COM59	Row 5	RAM4	Row 13	RAM12	Row 4	RAM12	-	-	-	-	-	-	-	-	
COM60	Row 3	RAM3	Row 12	RAM11	Row 3	RAM11	-	-	-	-	-	-	-	-	
COM61	Row 2	RAM2	Row 10	RAM10	Row 2	RAM10	-	-	-	-	-	-	-	-	
COM62	Row 1	RAM1	Row 9	RAM9	Row 1	RAM9	-	-	-	-	-	-	-	-	
COM63	Row 0	RAM0	Row 8	RAM8	Row 0	RAM8		-	-	-	-	-	-	-	
s refe)	a)	(l	0)	(0	C)	(d)	(e)	(1	f)	(g)	
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 Solomon Systech
 Jul 2006
 P 44/68
 Rev 1.0
 SSD1331

9.1.9 Set Display Mode (A4h ~ A7h)

These are single byte command and they are used to set Normal Display, Entire Display On, Entire Display Off and Inverse Display.

- Normal Display (A4h)
 - Reset the above effect and turn the data to ON at the corresponding gray level.
- Set Entire Display On (A5h)
 - Forces the entire display to be at "GS63" regardless of the contents of the display data RAM.
- Set Entire Display Off (A6h)
 - Forces the entire display to be at gray level "GS0" regardless of the contents of the display data RAM.
- Inverse Display (A7h)
 - The gray level of display data are swapped such that "GS0" <-> "GS63", "GS1" <-> "GS62",

9.1.10 Set Multiplex Ratio (A8h)

This command switches default 1:64 multiplex mode to any multiplex mode from 16 to 64. For example, when multiplex ratio is set to 16, only 16 common pins are enabled. The starting and the ending of the enabled common pins are depended on the setting of "Display Offset" register programmed by command A2h.

9.1.11 Dim mode setting (ABh)

This command contains multiple bits to configure the dim mode display parameters. Contrast setting of color A, B, C and precharge voltage can be set different to normal mode (AFh).

9.1.12 Set Master Configuration (ADh)

This command selects the external V_{CC} power supply. External V_{CC} power should be connected to the V_{CC} pin. A[0] bit must be set to 0b after RESET.

This command will be activated after issuing Set Display ON command (AFh)

9.1.13 Set Display On/Off (ACh / AEh / AFh)

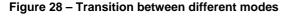
These single byte commands are used to turn the OLED panel display on or off.

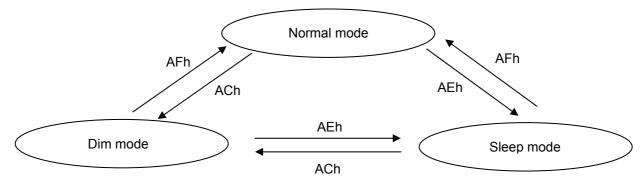
When the display is on, the selected circuits by Set Master Configuration command will be turned on. When the display is off, those circuits will be turned off and the segment and common output are in high impedance state.

These commands set the display to one of the three states:

- o ACh: Dim Mode Display On
- o AEh: Display Off (sleep mode)
- o AFh: Normal Brightness Display On

where the dim mode settings are controlled by command ABh.





SSD1331 | Rev 1.0 | P 45/68 | Jul 2006 | Solomon Systech

9.1.14 Power Save Mode (B0h)

This command is used in enabling or disabling the power save mode.

9.1.15 Phase 1 and 2 Period Adjustment (B1h)

This command sets the length of phase 1 and 2 of segment waveform of the driver.

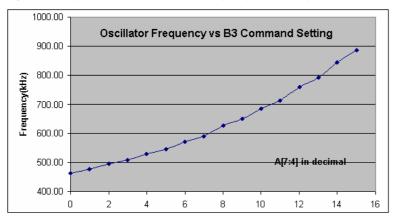
- Phase 1 (A[3:0]): Set the period from 1 to 15 in the unit of DCLKs. A larger capacitance of the OLED pixel may require longer period to discharge the previous data charge completely.
- Phase 2 (A[7:4]): Set the period from 1 to 15 in the unit of DCLKs. A longer period is needed to charge up a larger capacitance of the OLED pixel to the target voltage V_P for color A, B and C.

9.1.16 Set Display Clock Divide Ratio/ Oscillator Frequency (B3h)

This command consists of two functions:

- Display Clock Divide Ratio (A[3:0])
 Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with power on reset value = 1. Please refer to section 7.3.1 for the details relationship of DCLK and CLK.
- Oscillator Frequency (A[7:4])
 Program the oscillator frequency Fosc that is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency settings available as shown below. The default setting is 1101b

Figure 29 - Typical Oscillator frequency adjustment by B3 command (V_{DD} =2.7V)



9.1.17 Set Gray Scale Table (B8h)

This command is used to set the gray scale table for the display. Except gray scale entry 0, which is zero as it has no pre-charge and current drive, each odd entry gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK. The longer the length of the pulse width, the brighter is the OLED pixel when it's turned on. Please refer to section 7.6 for more detailed explanation of relation of display data RAM, gray scale table and the pixel brightness.

Following the command B8h, the user has to set the pulse width for GS1, GS3, GS5, ..., GS59, GS61, and GS63 one by one in sequence and complies the following conditions.

Afterwards, the driver automatically derives the pulse width of even entry of gray scale table GS2, GS4, ..., GS62 with the formula like below.

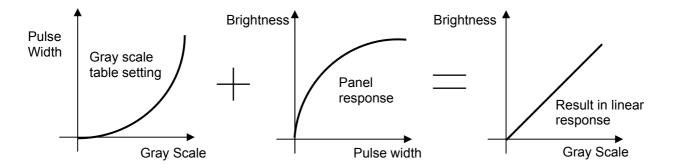
$$GSn = (GSn-1 + GSn+1)/2$$

For example, if GS1 = 3 DCLKs and GS3 = 7 DCLKs, GS2 = (3+7)/2 = 5 DCLKs

The setting of gray scale table entry can perform gamma correction on OLED panel display. Normally, it is desired that the brightness response of the panel is linearly proportional to the image data value in display data RAM. However, the OLED panel is somehow responded in non-linear way. Appropriate gray scale table setting like example below can compensate this effect.

Solomon Systech Jul 2006 | P 46/68 | Rev 1.0 | SSD1331

Figure 30 - Example of gamma correction by gray scale table setting



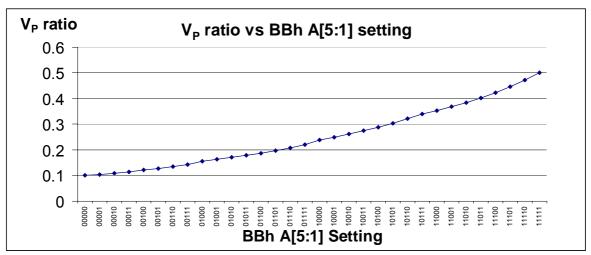
9.1.18 Enable Linear Gray Scale Table (B9h)

This command reloads the preset linear gray scale table as GS1 = 1, GS2 = 3, GS3 = 5,, GS62 = 123, GS63 = 125 DCLKs.

9.1.19 Set Pre-charge voltage (BBh)

This command sets the pre-charge voltage level of segment pins. The level of V_P is programmed with reference to V_{CC} . Figure 31 shows the details of setting Pre-charge voltage level by command BBh A[5:1].

Figure 31 – Typical Pre-charge voltage level setting by command BBh.



Note

9.1.20 Set V_{COMH} Voltage (BEh)

This command sets the high voltage level of common pins. The level of V_{COMH} is programmed with reference to V_{CC} .

9.1.21 NOP (BCh, BDh, E3h)

These are command for no operation.

9.1.22 Set Command Lock (FDh)

This command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is call "Lock" state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the "Lock" state.

Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resume from the "Lock" state. And the driver IC will then respond to the command and memory access.

SSD1331 | Rev 1.0 | P 47/68 | Jul 2006 | Solomon Systech

^(!) V_P ratio = 0.1 refers to V_P voltage = 0.1 x V_{CC}

9.2 GRAPHIC ACCELERATION COMMAND SET DESCRIPTION

9.2.1 Draw Line (21h)

This command draws a line by the given start, end column and row coordinates and the color of the line.

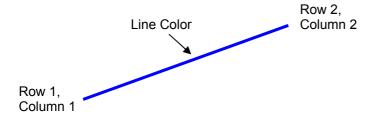


Figure 32 - Example of Draw Line Command

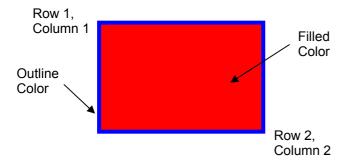
For example, the line above can be drawn by the following command sequence.

- 1. Enter into draw line mode by command 21h
- 2. Send column start address of line, column1, for example = 1h
- 3. Send row start address of line, row 1, for example = 10h
- 4. Send column end address of line, column 2, for example = 28h
- 5. Send row end address of line, row 2, for example = 4h
- 6. Send color C, B and A of line, for example = 35d, 0d, 0d for blue color

9.2.2 Draw Rectangle (22h)

Given the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2), specify the outline and fill area colors, a rectangle that will be drawn with the color specified. Remarks: If fill color option is disabled, the enclosed area will not be filled.

Figure 33 - Example of Draw Rectangle Command



The following example illustrates the rectangle drawing command sequence.

- 1. Enter the "draw rectangle mode" by execute the command 22h
- 2. Set the starting column coordinates, Column 1. e.g., 03h.
- 3. Set the starting row coordinates, Row 1. e.g., 02h.
- 4. Set the finishing column coordinates, Column 2. e.g., 12h
- 5. Set the finishing row coordinates, Row 2. e.g., 15h
- 6. Set the outline color C, B and A. e.g., (28d, 0d, 0d) for blue color
- 7. Set the filled color C, B and A. e.g., (0d, 0d, 40d) for red color

Solomon Systech Jul 2006 | P 48/68 | Rev 1.0 | SSD1331

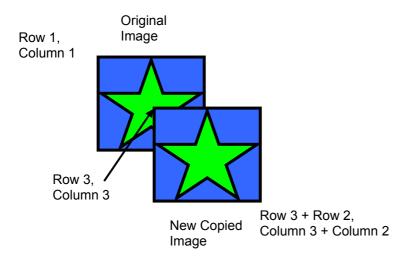
9.2.3 Copy (23h)

Copy the rectangular region defined by the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to location (Row 3, Column 3). If the new coordinates are smaller than the ending points, the new image will overlap the original one.

The following example illustrates the copy procedure.

- 1. Enter the "copy mode" by execute the command 23h
- 2. Set the starting column coordinates, Column 1. E.g., 00h.
- 3. Set the starting row coordinates, Row 1. E.g., 00h.
- 4. Set the finishing column coordinates, Column 2. E.g., 05h
- 5. Set the finishing row coordinates, Row 2. E.g., 05h
- 6. Set the new column coordinates, Column 3. E.g., 03h
- 7. Set the new row coordinates, Row 3. E.g., 03h

Figure 34 - Example of Copy Command



9.2.4 Dim Window (24h)

This command will dim the window area specify by starting point (Row 1, Column 1) and the ending point (Row 2, Column 2). After the execution of this command, the selected window area will become darker as follow.

Table 15 - Result of Change of Brightness by Dim Window Command

Original gray scale	New gray scale after dim window command
GS0 ~ GS15	No change
GS16 ~ GS19	GS4
GS20 ~ GS23	GS5
:	:
GS60 ~ GS63	GS15

Additional execution of this command over the same window area will not change the data content.

SSD1331 | Rev 1.0 | P 49/68 | Jul 2006 | **Solomon Systech**

9.2.5 Clear Window (25h)

This command sets the window area specify by starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to clear the window display. The graphic display data RAM content of the specified window area will be set to zero.

This command can be combined with Copy command to make as a "move" result. The following example illustrates the copy plus clear procedure and results in moving the window object.

- 1. Enter the "copy mode" by execute the command 23h
- 2. Set the starting column coordinates, Column 1. E.g., 00h.
- 3. Set the starting row coordinates, Row 1. E.g., 00h.
- 4. Set the finishing column coordinates, Column 2. E.g., 05h
- 5. Set the finishing row coordinates, Row 2. E.g., 05h
- 6. Set the new column coordinates, Column 3. E.g., 06h
- 7. Set the new row coordinates, Row 3. E.g., 06h
- 8. Enter the "clear mode" by execute the command 25h
- 9. Set the starting column coordinates, Column 1. E.g., 00h.
- 10. Set the starting row coordinates, Row 1. E.g., 00h.
- 11. Set the finishing column coordinates, Column 2. E.g., 05h
- 12. Set the finishing row coordinates, Row 2. E.g., 05h

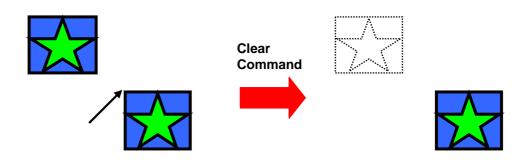


Figure 35 - Example of Copy + Clear = Move Command

9.2.6 Fill Enable/Disable (26h)

This command has two functions.

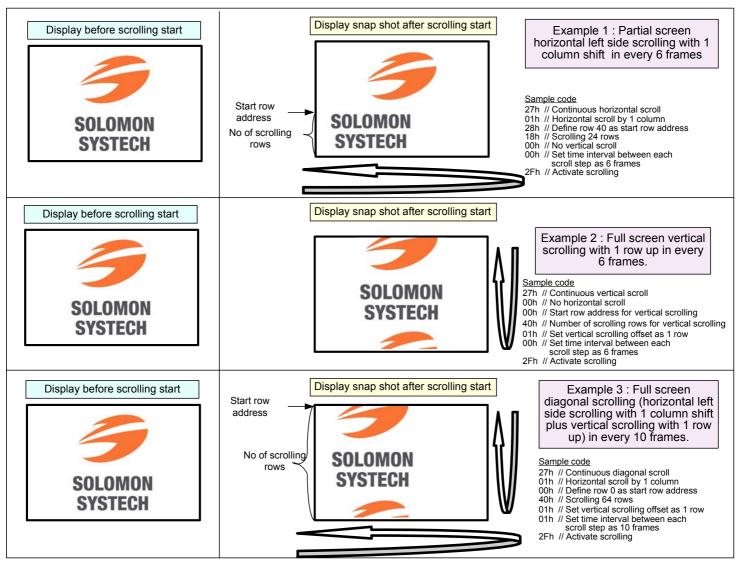
- Enable/Disable fill (A[0])
 - 0 = Disable filling of color into rectangle in draw rectangle command. (RESET)
 - 1 = Enable filling of color into rectangle in draw rectangle command.
- Enable/Disable reverse copy (A[4])
 - 0 = Disable reverse copy (RESET)
 - 1 = During copy command, the new image colors are swapped such that "GS0" <-> "GS63", "GS1" <-> "GS62", \dots

Solomon Systech Jul 2006 P 50/68 Rev 1.0 SSD1331

9.2.7 Continuous Horizontal & Vertical Scrolling Setup (27h)

This command setup the parameters required for horizontal and vertical scrolling. The parameters should not be changed after scrolling is activated

Figure 36 - Examples of Continuous Horizontal and Vertical Scrolling command setup



9.2.8 Deactivate scrolling (2Eh)

This command deactivates the scrolling action. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

9.2.9 Activate scrolling (2Fh)

This command activates the scrolling function according to the setting done by Continuous Horizontal & Vertical Scrolling Setup command 27h.

 SSD1331
 Rev 1.0
 P 51/68
 Jul 2006
 Solomon Systech

10 MAXIMUM RATINGS

Table 16 - Maximum Ratings

(Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}		-0.3 to +4	V
V_{DDIO}	Supply Voltage	-0.3 to V _{DD} +0.5	V
V_{CC}		0 to 19.0	V
V _{SEG} / V _{COM}	SEG/COM output voltage	0 to 19.0	V
I _{SEG}	SEG output current	0 to 220	uA
V_{in}	Input voltage	V_{SS} -0.3 to V_{DD} +0.3	V
T _A	Operating Temperature	-40 to +85	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

^{*}Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

 Solomon Systech
 Jul 2006
 P 52/68
 Rev 1.0
 SSD1331

11 DC CHARACTERISTICS

Table 17 - DC Characteristics

Conditions (unless specified):

Voltage referenced to V_{SS} V_{DD} = 2.7, V_{DDIO} = 1.8V, V_{CC} = 11.0V, I_{REF} = 10uA, at T_A = 25°C.

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit
V_{CC}	Operating Voltage	-	8	11	18	V
V_{DD}	Logic Supply Voltage	-	2.4	2.7	3.5	V
V_{DDIO}	Power Supply for I/O pins	-	1.6	1.8	V_{DD}	V
V _{OH}	High Logic Output Level	I _{OUT} = 100uA, 3.3MHz	$0.9 \times V_{DDIO}$	-	V_{DDIO}	V
V_{OL}	Low Logic Output Level	I _{OUT} = 100uA, 3.3MHz	0	-	$0.1 \times V_{DDIO}$	V
V_{IH}	High Logic Input Level	-	$0.8 \times V_{DDIO}$	-	V_{DDIO}	V
V_{IL}	Low Logic Input Level	-	0	-	$0.2 \times V_{DDIO}$	V
I _{DD_SLEEP}	Sleep mode V _{DD} Current	Display OFF, No panel attached	-	0	10	uA
I _{DDIO} SLEEP	Sleep mode V _{DDIO} Current	Display OFF, No panel attached	-	0	10	uA
I _{CC_SLEEP}	Sleep mode V _{CC} Current	Display OFF, No panel attached	-	0	10	uA
I _{CC}	V _{CC} Supply Current	Display ON, Contrast = FFh, No panel attached	-	700	1200	uA
I _{DD}	V _{DD} Supply Current	Display ON, Contrast = FFh, No panel attached	-	170	500	uA
	Segment Output Current: V _{CC} = 8V, Display ON, All	Contrast = FFh	142	155	168	uA
I _{SEG}	1's pattern. (Segment pin under test is	Contrast = 7Fh	-	78	-	uA
	connected with a 20K Ω resistive load to V_{SS})	Contrast = 3Fh	-	39	-	uA
Dev	Segment Output Current Uniformity:	Contrast = FFh	-3	-	+3	%
Adj. Dev	Adjacent pin output current uniformity: Adj Dev = (I[n] - I[n+1]) / (I[n]+I[n+1])	Contrast = FFh	-2	-	+2	%
R _{COM_ON}	COM pin output resistance	COM[0:63], I = 20mA	-	25	30	Ω

SSD1331 Rev 1.0 P 53/68 Jul 2006 **Solomon Systech**

12 AC CHARACTERISTICS

Table 18 - AC Characteristics

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS} $V_{DD} = V_{DDIO} = 2.4V$ to 3.5V $V_{CC} = 8.0V$ to 18.0V $T_A = 25^{\circ}C$

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit
F _{osc}	Oscillation Frequency of Display Timing Generator	V _{DD} = 2.7V	774	860	946	KHz
F_{FRM}	Frame Frequency	Display ON, Internal Oscillator Enabled	ı	F _{OSC} x 1 / (D x K x N)	ı	Hz
RES#	Reset low pulse width	-	3	-	-	us
INLO#	Reset completion time	-	-	-	2	us

Jul 2006 | P 54/68 | Rev 1.0 SSD1331 Solomon Systech

Note

(1) Fosc stands for the frequency value of the internal oscillator and the value is measured when command B3h A[7:4]=1101b [default value]

⁽²⁾ D stands for divide ratio

⁽³⁾ K stands for total number of display clocks per row. (RESET=136, i.e. phase1 DCLK+phase2 DCLK + phase3 DCLK =4+7+125)

(4) N stands for number of MUX selected by command A8h

Table 19 - 6800-Series MPU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4V to 3.5V, V_{DDIO} = 2.4V to V_{DD}, T_A = -40 to +85°C)

Symbol	Parameter	Min	Тур	Max	Unit
t _{cycle}	Clock Cycle Time (write cycle)	130	-	1	ns
PW _{CSL}	Control Pulse Low Width (write cycle)	60	-	ı	ns
PW _{CSH}	Control Pulse High Width (write cycle)	60	-	ı	ns
t _{cycle}	Clock Cycle Time (read cycle)	200	-		ns
PW _{CSL}	Control Pulse Low Width (read cycle)	100	-	-	ns
PW _{CSH}	Control Pulse High Width (read cycle)	100	-	-	ns
t _{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t _{DSW}	Data Setup Time	40	-	1	ns
t_{DHW}	Data Hold Time	10	-	1	ns
t _{ACC}	Data Access Time	-	-	140	ns
t _{OH}	Output Hold time	-	-	70	ns
t _R	Rise Time	-	-	15	ns
t _⊨	Fall Time	-	-	15	ns

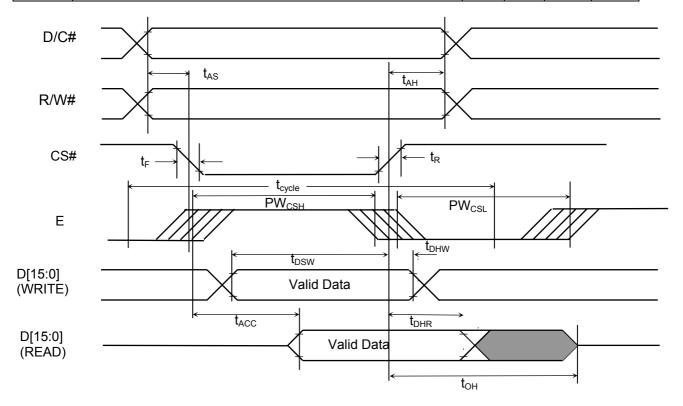


Figure 37 - 6800-series parallel interface characteristics

SSD1331 Rev 1.0 P 55/68 Jul 2006 **Solomon Systech**

(V_{DD} - V_{SS} = 2.4V to 3.5V, V_{DDIO} = 2.4V to V_{DD} , T_A = -40 to 85°C)

Symbol	Parameter	Min	Тур	Max	Unit
t _{cycle}	Clock Cycle Time	130	-	-	ns
t _{AS}	Address Setup Time	10	-	-	ns
t _{AH}	Address Hold Time	0	-	-	ns
t _{DSW}	Write Data Setup Time	40	-	-	ns
t _{DHW}	Write Data Hold Time	10	-	-	ns
t _{DHR}	Read Data Hold Time	20	-	-	ns
t _{OH}	Output Disable Time	-	-	70	ns
t _{ACC}	Access Time	-	-	140	ns
t _{PWLR}	Read Low Time	150	-	-	ns
t _{PWLW}	Write Low Time	60	-	-	ns
t _{PWHR}	Read High Time	60	-	-	ns
t _{PWHW}	Write High Time	60	-	-	ns
t _R	Rise Time	-	-	15	ns
t _F	Fall Time	-	-	15	ns
t _{CS}	Chip select setup time	0	-	-	ns
t _{CSH}	Chip select hold time to read signal	0	-	-	ns
t _{CSF}	Chip select hold time	20	-	-	ns

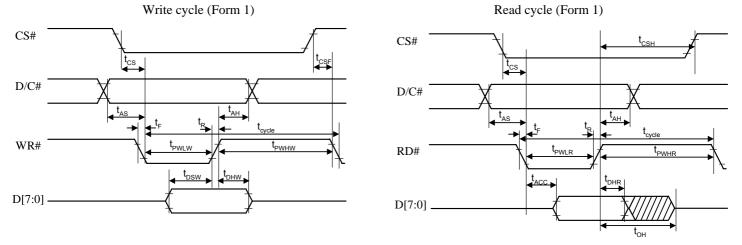


Figure 38 - 8080-series parallel interface characteristics (Form 1)

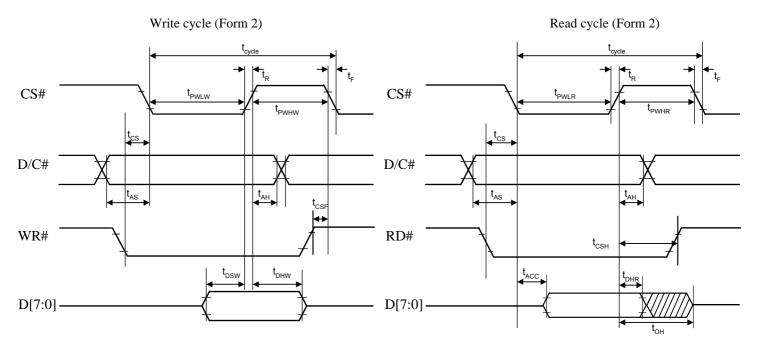


Figure 39 - 8080-series parallel interface characteristics (Form 2)

 Solomon Systech
 Jul 2006
 P 56/68
 Rev 1.0
 SSD1331

Table 21 - Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4V to 3.5V, V_{DDIO} = 2.4V to V_{DD}, T_A = -40 to 85°C)

Symbol	Parameter	Min	Тур	Max	Unit
t _{cycle}	Clock Cycle Time	150	-	•	ns
t_{AS}	Address Setup Time	40	-	ı	ns
t _{AH}	Address Hold Time	40	-	-	ns
t _{css}	Chip Select Setup Time	75	-	-	ns
t _{CSH}	Chip Select Hold Time	60	-	-	ns
t _{DSW}	Write Data Setup Time	40	-	-	ns
t _{DHW}	Write Data Hold Time	40	-	-	ns
t _{CLKL}	Clock Low Time	75	-	-	ns
t _{CLKH}	Clock High Time	75	-	•	ns
t_R	Rise Time	-	-	15	ns
t _F	Fall Time	-	-	15	ns

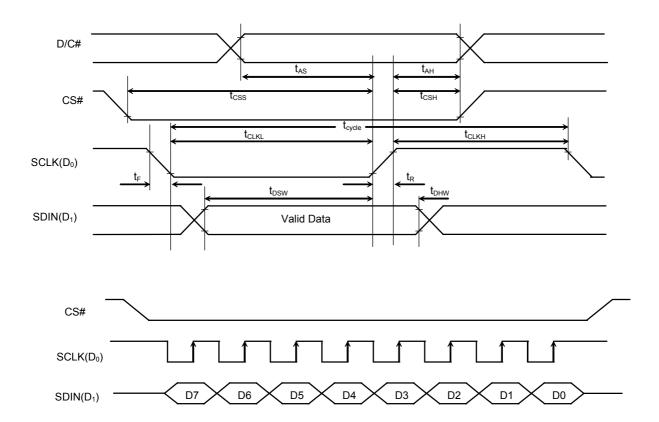


Figure 40 - Serial interface characteristics

SSD1331 Rev 1.0 P 57/68 Jul 2006 **Solomon Systech**

13 APPLICATION EXAMPLE

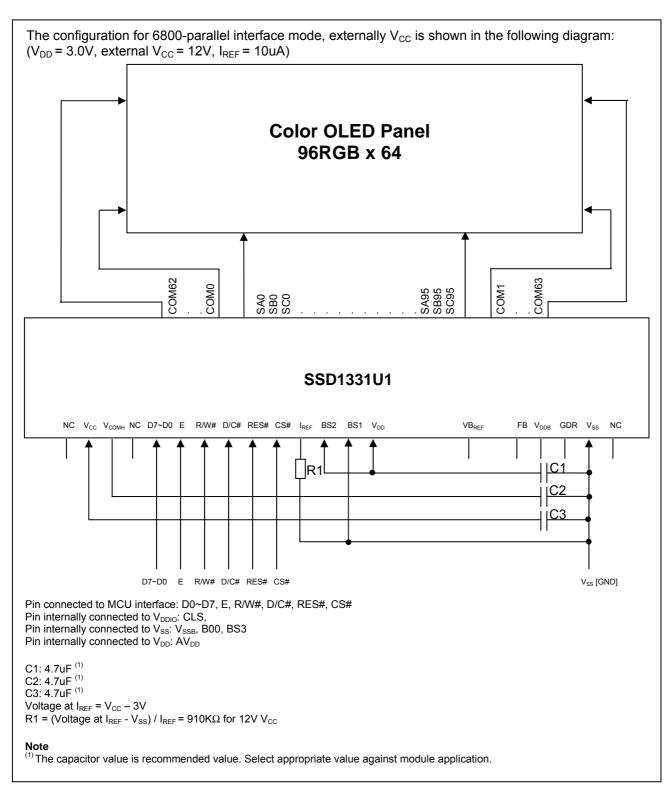


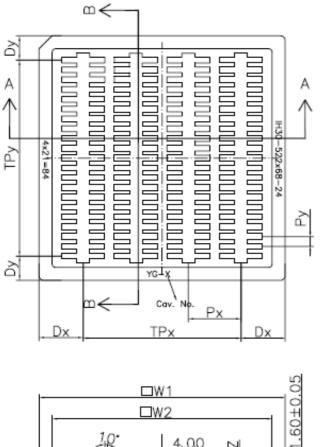
Figure 41 - Application Example for SSD1331U1R1

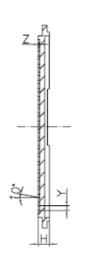
 Solomon Systech
 Jul 2006 | P 58/68 | Rev 1.0 |
 SSD1331

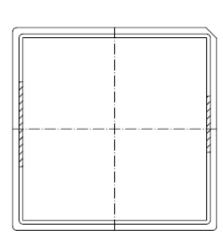
14 PACKAGE OPTIONS

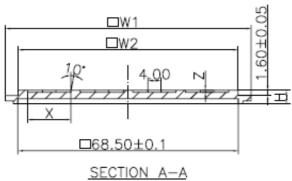
14.1 SSD1331Z Die Tray Information

Figure 42 - Die Tray Information







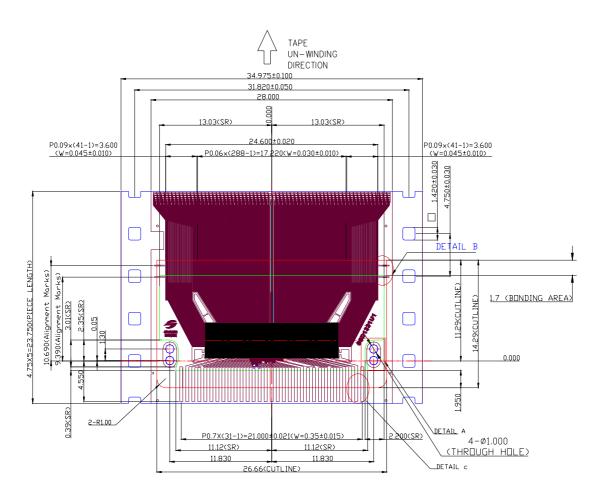


	Spec	
	mm	(mil)
W 1	76.00 ± 0.10	(2992)
W2	68.00 ± 0.10	(2677)
Н	4.20± 0.10	(165)
Dx	13.66±0.10	(538)
TPx	48.78±0.10	(1920)
Dy	7.55±0.10	(297)
ТРу	61.00±0.10	(2402)
Рх	16.26 ± 0.05	(640)
Ру	3.05 ± 0.05	(120)
X	13.25 ± 0.01	(522)
Υ	1.73 ± 0.01	(68)
Z	0.62 ± 0.05	(24)
N	84 (Pocket number)	

SSD1331 Rev 1.0 P 59/68 Jul 2006 **Solomon Systech**

14.2 SSD1331U1R1 COF PACKAGE DIMENSIONS

Figure 43 - SSD1331U1R1 outline drawing



NOTE:

1. GENERAL TOLERANCE: ±0.05mm

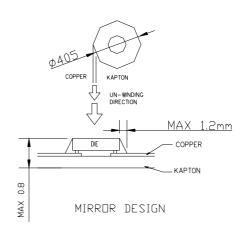
2. MATERIAL PI: 38±4um CU: 8±2um

SR: 15±10um

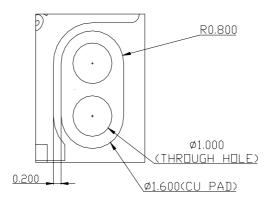
(OTHER TOLERANCE: ±0.200mm)

3. SN PLATING: 0.23±0.05um

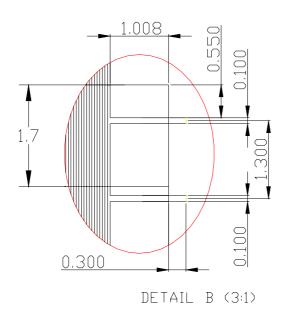
4. TAPSITE: 5 SPH, 23.75mm

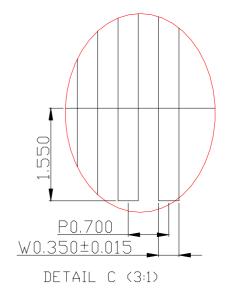


Solomon Systech Jul 2006 P 60/68 Rev 1.0 SSD1331



DETAIL A (3:1)





SSD1331 Rev 1.0 P 61/68 Jul 2006 **Solomon Systech**

14.3 SSD1331U1R1 COF PACKAGE PIN ASSIGNMENT

Figure 44 - SSD1331U1R1 pin assignment drawing

N N C C C C C C C C C C C C C C C C C C		0000N 0000N 400	MANGONG MANGON	SCI	<14	V N N N N N N N N N N N N N N N N N N N	2222	0000 888 888 888		COM59	N N N N N N N N N N N N N N N N N N N	길
401 400 3999 398 397 396		369 368 367 366 366	364 363 362 360 360	358	75	74 73 72	71 70 69 68	65 65 65 65	o 4	37. 37.	0 8 8 6 0 0 4 6 6	32,000
			8 대 대 대 대 대 대 대 대 대 대 대 대 대 대 대 대 대 대 대	ว 4 เก ฬ) Γ & σ	20	. ଅ ଅ	ر ا ا		.9 13		
												1
N (33 S S S S S S S S S S S S S S S S S S S	, 9 , 2 , 4 , 5		R/V# D/C#	CO# IREF	BS1 VDD	999	V BREF NC	, r B	GDR VSS NC		

 Solomon Systech
 Jul 2006
 P 62/68
 Rev 1.0
 SSD1331

Table 22 - SSD1331U1R1 pin assignment

Pin no.	Pin name	Pin no.	Pin name	Pin	no.	Pin name	1	Pin no.	Pin name	Pin no.	Pin name
1	NC	81	SA93		61	SB66		241	SC39	321	SA13
2	VCC	82	SC92		62	SA66	1	242	SB39	322	SC12
3	VCOMH	83	SB92	1	63	SC65	1	243	SA39	323	SB12
4	NC	84	SA92	1	64	SB65	1	244	SC38	324	SA12
5	D7	85	SC91	1	65	SA65		245	SB38	325	SC11
6	D6	86	SB91		66	SC64		246	SA38	326	SB11
7	D5	87	SA91		67	SB64	1	247	SC37	327	SA11
8	D4	88	SC90		68	SA64		248	SB37	328	SC10
9	D3	89	SB90		69	SC63		249	SA37	329	SB10
10	D2	90	SA90		70	SB63		250	SC36	330	SA10
11	D1	91	SC89		71	SA63		251	SB36	331	SC9
12	D0	92	SB89		72	SC62		252	SA36	332	SB9
13	E	93	SA89		73	SB62		253	SC35	333	SA9
14	R/W#	94	SC88		74	SA62		254	SB35	334	SC8
15	D/C#	95	SB88		7 5	SC61		255	SA35	335	SB8
16		96						256			
	RES#	96	SA88		76 77	SB61			SC34	336	SA8
17	CS#		SC87		77 70	SA61		257	SB34	337	SC7
18	IREF	98	SB87		78 70	SC60		258	SA34	338	SB7
19	BS2	99	SA87		79	SB60		259	SC33	339	SA7
20	BS1	100	SC86		80	SA60		260	SB33	340	SC6
21	VDD	101	SB86		81	SC59		261	SA33	341	SB6
22	NC	102	SA86		82	SB59		262	SC32	342	SA6
23	NC	103	SC85		83	SA59		263	SB32	343	SC5
24	NC	104	SB85		84	SC58		264	SA32	344	SB5
25	VBREF	105	SA85		85	SB58		265	SC31	345	SA5
26	NC	106	SC84		86	SA58		266	SB31	346	SC4
27	FB	107	SB84		87	SC57		267	SA31	347	SB4
28	VDDB	108	SA84		88	SB57		268	SC30	348	SA4
29	GDR	109	SC83		89	SA57		269	SB30	349	SC3
30	VSS	110	SB83		90	SC56		270	SA30	350	SB3
31	NC	111	SA83		91	SB56		271	SC29	351	SA3
32	NC	112	SC82	1	92	SA56		272	SB29	352	SC2
33	NC	113	SB82	1	93	SC55	1	273	SA29	353	SB2
34	NC	114	SA82	1	94	SB55	1	274	SC28	354	SA2
35	COM63	115	SC81	1	95	SA55	1	275	SB28	355	SC1
36	COM61	116	SB81	1	96	SC54	1	276	SA28	356	SB1
37	COM59	117	SA81	1	97	SB54	1	277	SC27	357	SA1
38	COM57	118	SC80	1	98	SA54	1	278	SB27	358	SC0
39	COM55	119	SB80	1	99	SC53	1	279	SA27	359	SB0
40	COM53	120	SA80	2	00	SB53	1	280	SC26	360	SA0
41	COM51	121	SC79	2	01	SA53	1	281	SB26	361	NC
42	COM49	122	SB79	2	02	SC52	1	282	SA26	362	NC
43	COM47	123	SA79	2	03	SB52	1	283	SC25	363	NC
44	COM45	124	SC78	2	04	SA52	1	284	SB25	364	NC
45	COM43	125	SB78	2	05	SC51	1	285	SA25	365	NC
46	COM41	126	SA78		06	SB51		286	SC24	366	NC
47	COM39	127	SC77		07	SA51		287	SB24	367	COM0
48	COM37	128	SB77		08	SC50		288	SA24	368	COM2
49	COM35	129	SA77		09	SB50		289	SC23	369	COM4
50	COM33	130	SC76		10	SA50		290	SB23	370	COM6
51	COM31	131	SB76		11	SC49		291	SA23	371	COM8
52	COM29	132	SA76		12	SB49	1	292	SC22	372	COM10
53	COM27	133	SC75		13	SA49		293	SB22	373	COM12
54	COM25	134	SB75		14	SC48	1	293	SA22	373	COM12 COM14
55	COM23	135	SA75		15	SB48		295	SC21	375	COM14 COM16
							1		SB21		
56 57	COM21 COM19	136 137	SC74 SB74		16 17	SA48 SC47		296 297	SA21	376 377	COM18 COM20
5 <i>1</i>					18			297		377	
	COM17 COM15	138	SA74			SB47			SC20		COM22
59 60		139	SC73		19	SA47		299	SB20	379	COM24
60	COM13	140	SB73		20	SC46		300	SA20	380	COM26
61	COM11	141	SA73		21	SB46		301	SC19	381	COM28
62	COM9	142	SC72		22	SA46		302	SB19	382	COM30
63	COM7	143	SB72		23	SC45		303	SA19	383	COM32
64	COM5	144	SA72		24	SB45		304	SC18	384	COM34
65	COM3	145	SC71		25	SA45		305	SB18	385	COM36
66	COM1	146	SB71		26	SC44		306	SA18	386	COM38
67	NC	147	SA71		27	SB44		307	SC17	387	COM40
68	NC	148	SC70		28	SA44		308	SB17	388	COM42
69	NC	149	SB70		29	SC43		309	SA17	389	COM44
70	NC	150	SA70		30	SB43		310	SC16	390	COM46
71	NC	151	SC69		31	SA43		311	SB16	391	COM48
72	NC	152	SB69		32	SC42		312	SA16	392	COM50
73	SC95	153	SA69		33	SB42		313	SC15	393	COM52
74	SB95	154	SC68	2	34	SA42	1	314	SB15	394	COM54
75	SA95	155	SB68	2	35	SC41	1	315	SA15	395	COM56
76	SC94	156	SA68		36	SB41	1	316	SC14	396	COM58
77	SB94	157	SC67		37	SA41	1	317	SB14	397	COM60
78	SA94	158	SB67		38	SC40	1	318	SA14	398	COM62
79	SC93	159	SA67		39	SB40		319	SC13	399	NC
	SB93	160	SC66		40	SA40	•	320	SB13	400	NC
80				. 4	. •	5, 1.10		020	3513	700	

Pin no. 401

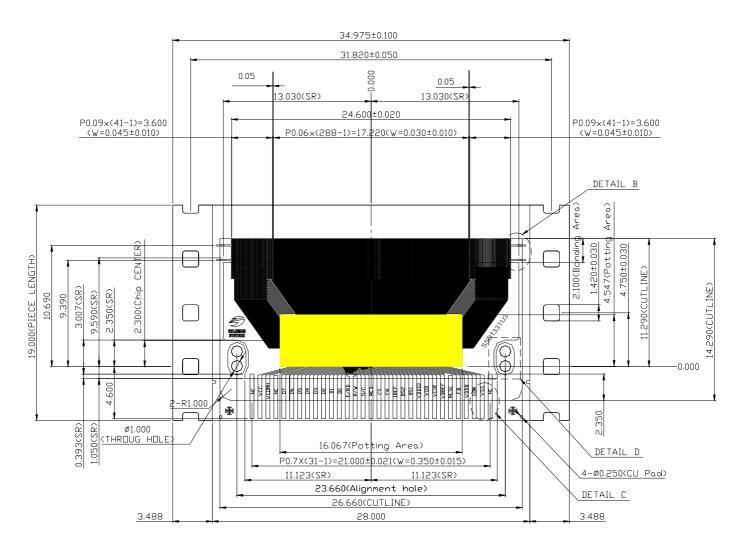
Pin name NC

SSD1331 Rev 1.0 P 63/68 Jul 2006 **Solomon Systech**

14.4 SSD1331U3R1 COF PACKAGE DIMENSIONS

Figure 45 - SSD1331U3R1 outline drawing





NOTE:

1. GENERAL TOLERANCE: ±0.05mm

2. MATERIAL

PI: KAPTON (150EN) 38±4um

CU: 8±2um

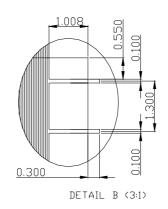
SR: SN9000 15±10um

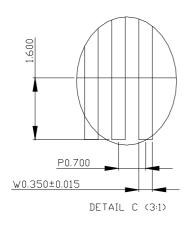
(DTHER TOLERANCE: ±0,200mm)

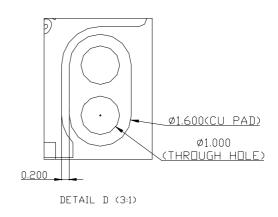
3. SN PLATING: 0.23±0.05um

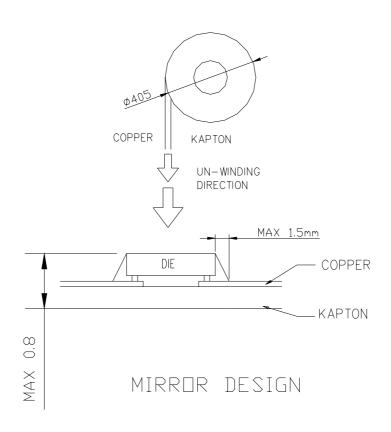
4. TAPSITE: 4 SPH, 19.00mm

Solomon Systech Jul 2006 P 64/68 Rev 1.0 SSD1331





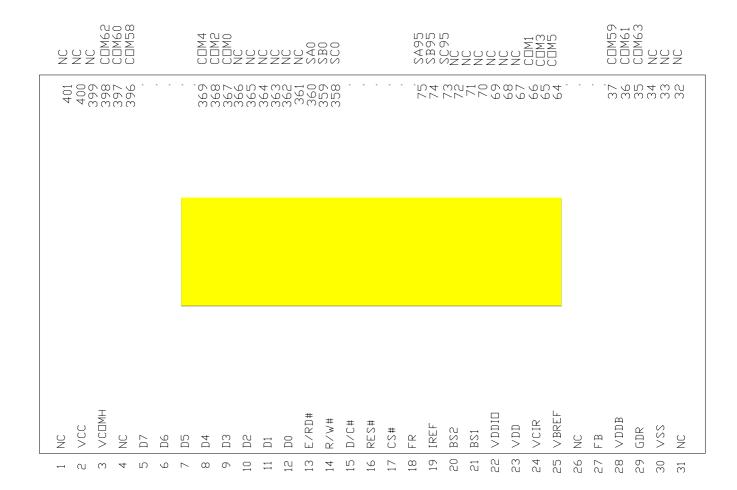




SSD1331 Rev 1.0 P 65/68 Jul 2006 **Solomon Systech**

14.5 SSD1331U3R1 COF PACKAGE PIN ASSIGNMENT

Figure 46 - SSD1331U3R1 pin assignment drawing



Solomon Systech Jul 2006 | P 66/68 | Rev 1.0 | **SSD1331**

Table 23 - SSD1331U3R1 pin assignment

Pin no.	Pin name NC	Pin no. 81	Pin nam	
2	VCC	82	SC92	
3	VCOMH	83	SB92	
4	NC	84	SA92	
5	D7	85	SC91	
6	D6	86	SB91	
7	D5	87	SA91	
8	D4	88	SC90	
9	D3	89	SB90	
10 11	D2 D1	90 91	SA90	
12	DI D0	92	SC89 SB89	
13	E/RD#	93	SA89	
14	R/W#	94	SC88	
15	D/C#	95	SB88	
16	RES#	96	SA88	
17	CS#	97	SC87	
18	FR	98	SB87	
19	IREF	99	SA87	
20	BS2	100	SC86	
21	BS1	101	SB86	
22	VDDIO	102	SA86	
23	VDD	103	SC85	
24	VCIR	104 105	SB85	
25 26	VBREF NC	105	SA85 SC84	
	FB	106	SC84 SB84	
27 28	VDDB	107	SB84 SA84	
29	GDR	108	SC83	
30	VSS	110	SB83	
31	NC	111	SA83	
32	NC	112	SC82	
33	NC	113	SB82	
34	NC	114	SA82	
35	COM63	115	SC81	
36	COM61	116	SB81	
37	COM59	117	SA81	
38	COM57	118	SC80	
39	COM55	119	SB80	
40 41	COM53 COM51	120	SA80	
42	COM49	121 122	SC79 SB79	
43	COM47	123	SA79	
44	COM45	124	SC78	
45	COM43	125	SB78	
46	COM41	126	SA78	
47	COM39	127	SC77	
48	COM37	128	SB77	
49	COM35	129	SA77	
50	COM33	130	SC76	
51	COM31	131	SB76	
52	COM29 COM27	132	SA76	
53	COM27 COM25	133 134	SC75	
54 55		135	SB75 SA75	
56	COM23 COM21	136	SC74	
57	COM19	137	SB74	
58	COM17	138	SA74	
59	COM15	139	SC73	
60	COM13	140	SB73	
61	COM11	141	SA73	
62	COM9	142	SC72	
63	COM7	143	SB72	
64	COM5	144	SA72	
65	COM3	145	SC71	
66	COM1	146	SB71	
67	NC	147	SA71	
68 60	NC NC	148	SC70	
69 70	NC NC	149 150	SB70	
70 71	NC NC	150	SA70 SC69	
71	NC NC	151	SB69	
73	SC95	153	SA69	
74	SB95	154	SC68	
75	SA95	155	SB68	
76	SC94	156	SA68	
77	SB94	157	SC67	
78	SA94	158	SB67	
79	SC93	159	SA67	
80	SB93	160	SC66	

	piii dooigi	
no.	Pin name	Ì
31	SA93	
32	SC92	
33	SB92	
34 35	SA92 SC91	
36 37	SB91 SA91	
38	SC90	
39	SB90	
90	SA90	
91	SC89	
92	SB89	
93	SA89	
94	SC88	
95	SB88	
96	SA88	
97	SC87	
98	SB87	
99	SA87	
00	SC86	
01	SB86	
02	SA86	
03	SC85	
04 05	SB85	
05 06	SA85 SC84	
06 07	SC84 SB84	
08	SA84	
09	SC83	
10	SB83	
11	SA83	
12	SC82	
13	SB82	
14	SA82	
15	SC81	
16	SB81	
17	SA81	
18	SC80	
19	SB80	
20 21	SA80 SC79	
22	SB79	
23	SA79	
24	SC78	
25	SB78	
26	SA78	
27	SC77	
28	SB77	
29	SA77	
30	SC76	
31	SB76	
32	SA76	
33	SC75	
34 35	SB75 SA75	
36	SC74	
37	SB74	
38	SA74	
39	SC73	
40	SB73	
41	SA73	
42	SC72	
43	SB72	
44	SA72	
45	SC71	
46	SB71	
47	SA71	
48	SC70	
49 50	SB70	
50	SA70 SC69	
51 52	SC69 SB69	
52 53	SA69	
54	SC68	
55	SB68	
56	SA68	
57	SC67	
58	SB67	
59	SA67	
60	SC66	

Pin no.	Pin name	Pin no.
161	SB66	241
162	SA66	242
163	SC65	243
164	SB65	244
165	SA65	245
166	SC64	246
167	SB64	247
168	SA64	248
169	SC63	249
170	SB63	250
_		
171	SA63	251
172	SC62	252
173	SB62	253
174	SA62	254
175	SC61	255
176	SB61	256
177	SA61	257
178	SC60	258
179	SB60	259
180	SA60	260
181	SC59	261
182	SB59	262
183	SA59	
		263
184	SC58	264
185	SB58	265
186	SA58	266
187	SC57	267
188	SB57	268
189	SA57	269
190	SC56	270
191	SB56	271
192	SA56	272
193	SC55	273
194	SB55	274
194	SA55	275
	SC54	
196		276
197	SB54	277
198	SA54	278
199	SC53	279
200	SB53	280
201	SA53	281
202	SC52	282
203	SB52	283
204	SA52	284
205	SC51	285
206	SB51	286
207	SA51	287
208	SC50	288
209	SB50	289
210	SA50	290
211	SC49	291
212	SB49	292
213	SA49	293
214	SC48	294
215	SB48	295
216	SA48	296
217	SC47	297
218	SB47	298
219	SA47	299
220	SC46	300
221	SB46	301
221	SA46	302
223		
	SC45	303
224	SB45	304
225	SA45	305
226	SC44	306
227	SB44	307
228	SA44	308
229	SC43	309
230	SB43	310
231	SA43	311
232	SC42	312
233	SB42	313
234	SA42	314
	SC41	314
235		
236	SB41	316
237	SA41	317
238	SC40	318
239	SB40	319
240	SA40	320

Pin no.	Pin name
321	SA13
322	SC12
323	SB12
324	SA12
325	SC11
326	SB11
327	SA11
328	SC10
329	SB10
330	SA10
331	SC9
332	SB9
333	SA9
334	SC8
335	SB8
336	SA8
337	SC7
338	SB7
339	SA7
340	SC6
341	SB6
342	SA6
343	SC5
344	SB5
345	SA5
346	SC4
347	SB4
	_
348	SA4
349	SC3
350	SB3
351	SA3
352	SC2
353	SB2
354	SA2
355	SC1
356	SB1
357	SA1
358	SC0
359	SB0
360	SA0
361	NC
362	NC
363	NC
364	NC
365	NC
366	NC
367	COM0
368	COM2
369	COM4
370	COM6
371	COM8
372	COM10
373	COM12
374	COM14
375	COM16
376	COM18
377	COM20
378	COM22
378	COM24
379	
	COM26
381	COM28
382	COM30
383	COM32
384	COM34
385	COM36
386	COM38
387	COM40
388	COM42
389	COM42 COM44
390	COM46
391	COM48
392	COM50
393	COM52
394	COM54
395	COM56
396	COM58
396	COM58 COM60
398	COM62
222	
399 400	NC NC

SB39

SA38 SC37 SB37 SA37 SC36 SB36 SA36 SC35

SC34 SB34 SA34 SC33

SC32 SB32 SA32

SA31 SC30 SB30 SA30

SA29 SC28 SB28

SB27 SA27 SC26 SB26

SB25 SA25 SC24

SC23 SB23 SA23

SB21 SA21

SA20 SC19 SB19 SA19

SA18 SC17 SB17

SB16 SA16 SC15

SB14 SA14

Pin no.	Pin name
401	NC

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Solomon Systech Jul 2006 | P 68/68 | Rev 1.0 | SSD1331