UG-9664HDDAG01

Application note

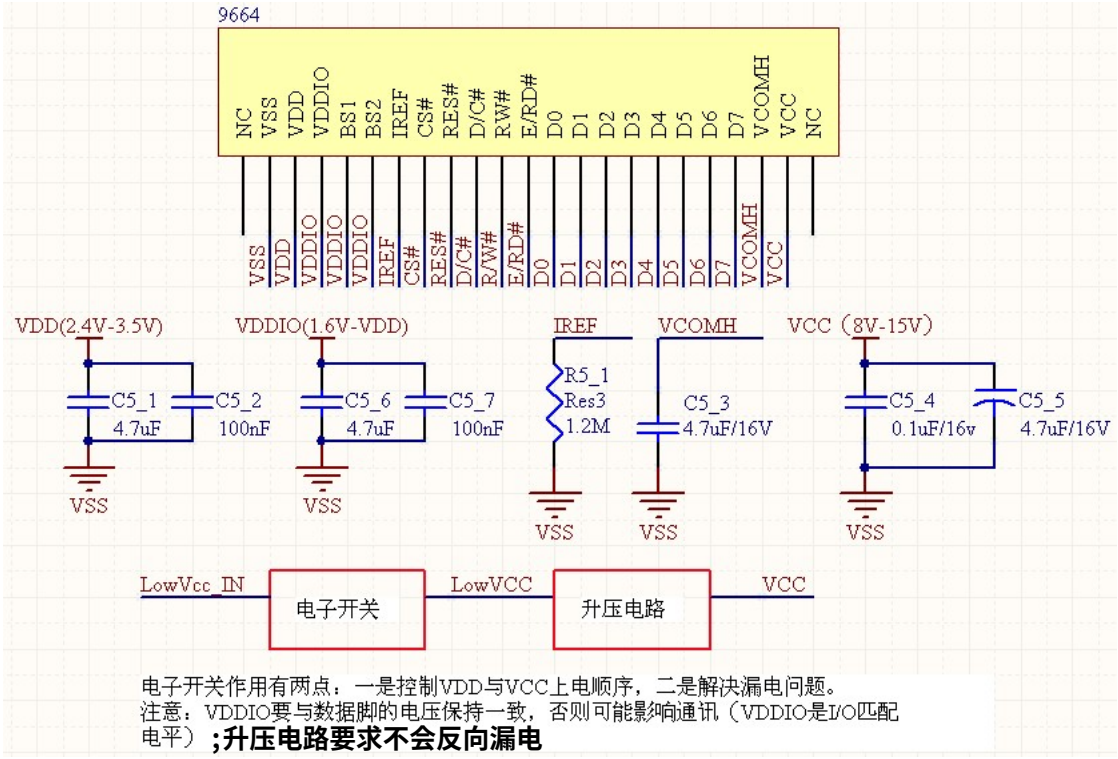
Evaluation Kit User Guide

Futureway Technology Limited
香港辰阳技术有限公司

Tel:0755-88846216 88843896
Fax:0755-61624316

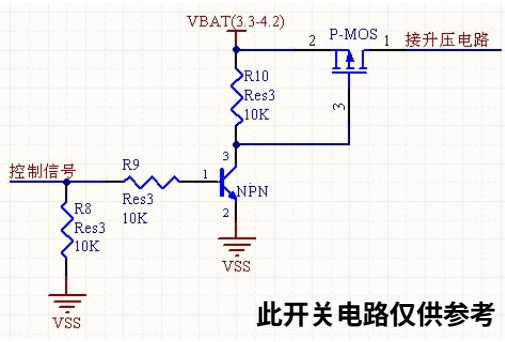
EVK Schematic

8080并口方式连接图



;升压电路要求不会反向漏电

开关电路



此开关电路仅供参考

Symbol define

D0-D7：These pins are 8-bit bi-directional data bus to be connected to the MCU's data bus.

BS1,BS2：These input pins are used to configure MCU interface selection by appropriate logic setting, which is described in the following table.

	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	Serial interface
BS1	**0**	**1**	**0**
BS2	**1**	**1**	**0**

Table 1 – MCU Interface Selection Setting

E_RD：This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected.

When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin E(RD#) must be connected to VSS.

RW_WR：This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W) selection input. Read mode will be carried out when this pin is pulled high and write mode when low.

When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin RW_WR must be connected to VSS.

DC：This pin is Data/Command control pin. When the pin is pulled high, the data at D7-D0 is treated as display data. When the pin is pulled low, the data at D7-D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the timing characteristics diagrams.

RESET：This pin is reset signal input. When the pin is low, initialization of the chip is executed.

CS：This pin is the chip select input. The chip is enabled for MCU communication only when CS is pulled low.

VCC：This is the most positive voltage supply pin of the chip.

VDD：Power Supply pin for logic operation of the driver.

VDDIO：Power supply for interface logic level. It should be match with the MCU interface voltage level. VDDIO must always be equal or lower than VDD .

(VDD - VSS = 2.4V to 3.5V, VDDIO = 2.4V to VDD, TA = -40 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	130	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	100 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 3 8080-Series MPU Parallel Interface Timing Characteristics

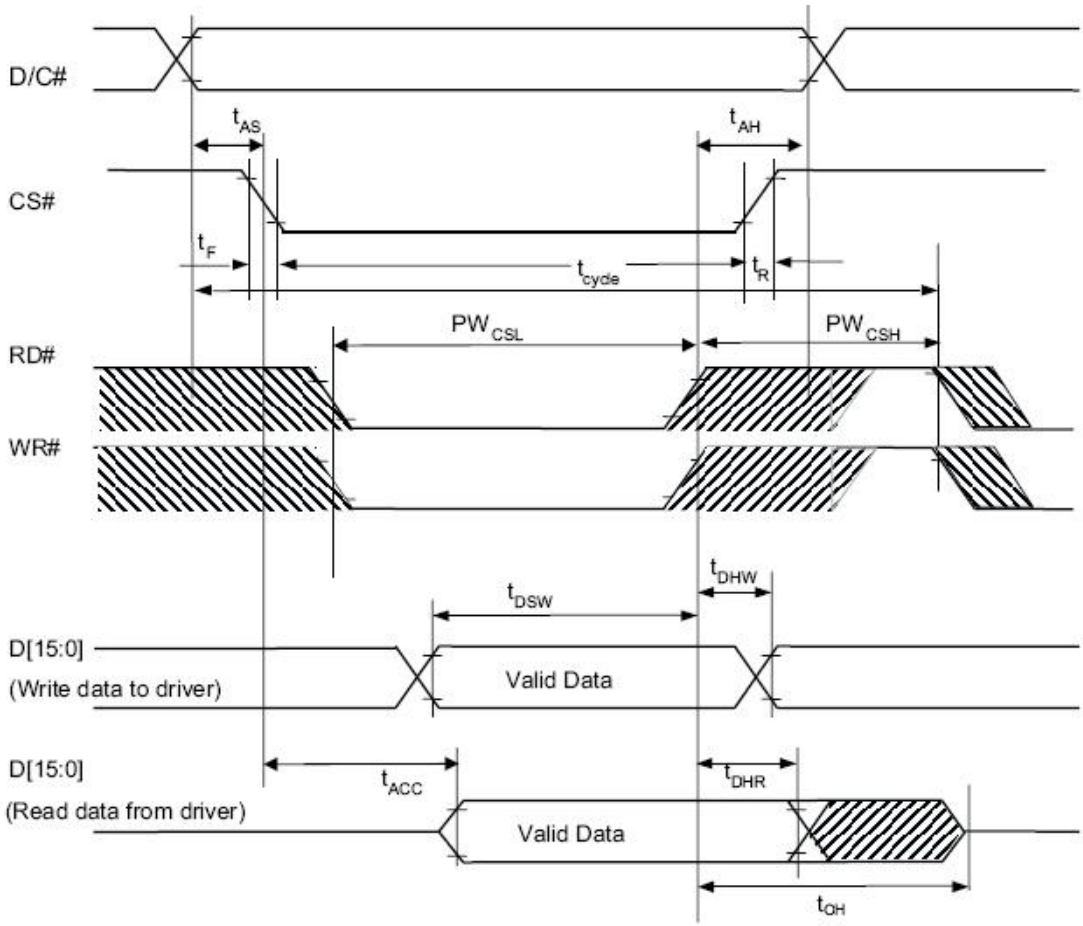
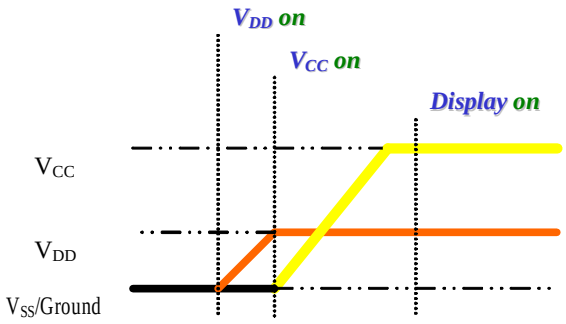
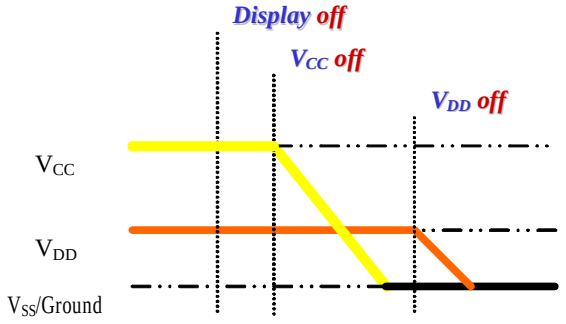


Figure 2 8080-series MPU parallel interface characteristics

Module power on sequence

Power down and Power up Sequence

To protect OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

<table>
<tr>
<td>1.1 Power up Sequence:
1. Power up V_{DD}
2. Send Display off command
3. Driver IC Initial Setting
4. Clear Screen
5. Power up V_{DDH}
6. Delay 100ms
(when V_{DD} is stable)
7. Send Display on command</td>
<td> 
</td>
</tr>
<tr>
<td>1.2 Power down Sequence:
1. Send Display off command
2. Power down V_{DDH}
3. Delay 100ms
(when V_{DDH} is reach 0 and panel is completely discharges)
4. Power down V_{DD}</td>
<td> 
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How to use UG-9664HDDAG01 module