計算機システム設計論　演習問題(4)

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コードを以下に示す。

module chat(input in,clk,rst,output logic out);

logic [3:0] count;

logic val;

always\_ff @(negedge clk) begin

if(rst) val <= 0;

else begin

if(!in) val <= 1;

else val <= val;

end

end

always\_ff @(negedge clk) begin

if(rst) count <= 4'b1111;

else if(val) begin

if(count != 0) count <= count - 1;

else count <= count;

end

end

always\_comb begin

if(count==0 || count ==4'b1111) out = in; //counterが始動する前or終了した後はinをそのまま出力

else out = 0; //counterが動いている間は0を出力

end

endmodule

続いてシミュレーションに使用したtestモジュールを示す。

module test;

logic in,clk,rst;

logic out;

always #5 clk = ~clk;

chat chat(in,clk,rst,out);

initial begin

$dumpfile("chat.vcd");

$dumpvars(0,test);

in = 1;

clk = 0;

rst = 1;

#10

rst = 0;

in = 1;

#10

in = 0;

#10

in = 1;

#10

in = 0;

#10

in = 1;

#10

in = 1;

#10

in = 1;

#10

in = 0;

#10

in = 1;

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in = 1;

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in = 1;

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in = 0;

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in = 0;

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in = 0;

#10

in = 0;

#10

in = 0;

#10

in = 1;

rst = 1;

#10

in = 1;

rst = 0;

#10

in = 1;

#10

in = 1;

#10

in = 0;

#10

in = 0;

#10

in = 1;

#10

in = 0;

#10

in = 0;

$finish;

end

endmodule

シミュレーション結果を以下に示す。

A screenshot of a computer

Description automatically generated with medium confidence