Hiroshi Sasaki

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Research Interests

Computer Architecture, Computer Security, Computer Systems, Workload Characterization

Professional Experience

Tokyo Institute of Technology ..... Apr. 2020 — Present
Associate Professor, Department of Information and Communications Engineering

Tier IV, Inc. ..... Apr. 2019 — Present
Consultant

Columbia University ..... Apr. 2016 — Mar. 2020
Associate Research Scientist, Department of Computer Science (Apr. 2016 — Mar. 2020)
Visiting Research Scientist, Department of Computer Science (Apr. 2014 — Mar. 2016)

IBM T.J. Watson Research Center ..... July 2013 — Mar. 2014
Visiting Research Scientist, Reliability- and Power-Aware Microarchitectures Group

Kyushu University ..... Aug. 2011 — Mar. 2014
Research Associate Professor, Department of Advanced Information Technology

The University of Tokyo ..... Apr. 2008 — July 2011
Research Assistant Professor, Department of Information Physics and Computing (Apr. 2010 — July 2011)
Research Assistant Professor, Research Center for Advanced Science and Technology (Apr. 2008 — Mar. 2010)

Education

The University of Tokyo, PhD in Engineering ..... Mar. 2008

The University of Tokyo, Master of Information Science and Technology ..... Mar. 2005

The University of Tokyo, Bachelor of Engineering ..... Mar. 2003

Publications

Conference papers

[C1] Hiroshi Sasaki, Miguel A. Arroyo, M. Tarek Ibn Ziad, Koustubha Bhat, Kanad Sinha, Simha Sethumadhavan. Practical byte-granular memory blacklisting using Califorms. In *Proceedings of the 52nd IEEE/ACM International Symposium on Microarchitecture (MICRO)*, 2019.
IEEE Micro Top Picks Honorable Mention

[C2] Hiroshi Sasaki, Fang-Hsiang Su, Teruo Tanimoto, Simha Sethumadhavan. Why do programs have heavy tails? In *Proceedings of the 2017 IEEE International Symposium on Workload Characterization (IISWC)*, pp.135–145, 2017.

[C3] Hiroshi Sasaki, Alper Buyuktosunoglu, Augusto Vega, Pradip Bose. Characterization and mitigation of power contention across multiprogrammed workloads. In *Proceedings of the 2016 IEEE International Symposium on Workload Characterization (IISWC)*, pp.55–64, 2016.

[C4] Yuan He, Masaaki Kondo, Takashi Nakada, Hiroshi Sasaki, Shinobu Miwa, Hiroshi Nakamura. Runtime multi-optimizations for energy efficient on-chip interconnections, In *Proceedings of the 33nd IEEE International Conference on Computer Design (ICCD)*, pp.455–458, 2015. (poster presentation)

[C5] Takeshi Soga, Hiroshi Sasaki, Tomoya Hirao, Masaaki Kondo, Koji Inoue. A flexible hardware barrier mechanism for many-core processors, In *Proceedings of the 20th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.61–68, 2015.

[C6] Satoshi Imamura, Hiroshi Sasaki, Koji Inoue. Power-capped DVFS and thread allocation with ANN models on modern NUMA systems. In *Proceedings of the 32nd IEEE International Conference on Computer Design (ICCD)*, pp.324–331, 2014.

[C7] Yuki Abe, Hiroshi Sasaki, Shinpei Kato, Koji Inoue, Masato Edahiro, Martin Peres. Power and performance characterization and modeling of GPU-accelerated systems. In *Proceedings of the 28th IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, pp.113–122, 2014.

[C8] Hiroshi Sasaki, Satoshi Imamura, Koji Inoue. Coordinated power-performance optimization in manycores. In *Proceedings of the 22nd International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pp.51–62, 2013.
IEEE Computer Society Japan Chapter Young Author Award 2013

[C9] Yuan He, Hiroshi Sasaki, Shinobu Miwa, Hiroshi Nakamura. McRouter: multicast within a router for high performance network-on-chips. In *Proceedings of the 22nd International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pp.842–850, 2013.

[C10] Keitarou Oka, Hiroshi Sasaki, Koji Inoue. Line sharing cache: exploring cache capacity with frequent line value locality. In *Proceedings of the 18th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.669–674, 2013.

[C11] Masaaki Kondo, Son-Truong Nguyen, Tomoya Hirao, Takeshi Soga, Hiroshi Sasaki, Koji Inoue. SMYLEref: a reference architecture for manycore-processor SoCs. In *Proceedings of the 18th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.561–564, 2013. (invited paper)

[C12] Hiroshi Sasaki, Teruo Tanimoto, Koji Inoue, Hiroshi Nakamura. Scalability-based manycore partitioning. In *Proceedings of the 21st International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pp.107–116, 2012.

[C13] Takaaki Hanada, Hiroshi Sasaki, Koji Inoue, Kazuaki J. Murakami. Performance evaluation of 3D stacked multi-core processors with temperature consideration. In *Proceedings of the 2011 IEEE International 3D Systems Integration Conference (3DIC)*, pp.1–5, 2012.

[C14] Noriko Takagi, Hiroshi Sasaki, Masaaki Kondo, Hiroshi Nakamura. Cooperative shared resource access control for low-power chip multiprocessors. In *Proceedings of the 14th ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pp.177–182, 2009.

[C15] Hiroshi Sasaki, Masaaki Kondo, Hiroshi Nakamura. An intra-task DVFS technique based on statistical analysis of hardware events. In *Proceedings of the 4th ACM International Conference on Computing Frontiers (CF)*, pp.123–130, 2007.

[C16] Hiroshi Sasaki, Masaaki Kondo, Hiroshi Nakamura. Energy-efficient dynamic instruction scheduling logic through instruction grouping. In *Proceedings of the 2006 ACM International Symposium on Low Power Electronics and Design (ISLPED)*, pp.43–48, 2006.

Journal papers

[J1] Satoshi Imamura, Yuichiro Yasui, Koji Inoue, Takatsugu Ono, Hiroshi Sasaki, Katsuki Fujisawa. Evaluating energy-efficiency of DRAM channel interleaving schemes for multithreaded programs. *IEICE Transactions on Information and Systems*, Vol.E101-D, No.9, pp.2247–2257, Sep. 2018.

[J2] Teruo Tanimoto, Takatsugu Ono, Koji Inoue, Hiroshi Sasaki. Enhanced dependence graph model for critical path analysis on modern out-of-order processors. *IEEE Computer Architecture Letters (CAL)*, Vol.16, Issue 2, pp.111–114, Jul-Dec 2017 (published in Mar 2017).

[J3] Hiroshi Sasaki, Fang-Hsiang Su, Teruo Tanimoto, Simha Sethumadhavan. Heavy tails in program structure. *IEEE Computer Architecture Letters (CAL)*, Vol.16, Issue 1, pp.34–37, Jan-Jun 2017 (published in May 2016).

[J4] Hiroshi Sasaki, Alper Buyuktosunoglu, Augusto Vega, Pradip Bose. Mitigating power contention: a scheduling based approach. *IEEE Computer Architecture Letters (CAL)*, Vol.16, Issue 1, pp.60–63, Jan-Jun 2017 (published in May 2016).

[J5] Yuan He, Masaaki Kondo, Takashi Nakada, Hiroshi Sasaki, Shinobu Miwa, Hiroshi Nakamura. A runtime optimization selection framework to realize energy efficient networks-on-chip. *IEICE Transactions on Information and Systems*, Vol.E99.D, No.12, pp.2881–2890, Dec. 2016

[J6] Yuan He, Hiroki Matsutani, Hiroshi Sasaki, Hiroshi Nakamura. Adaptive data compression on 3D network-on-chips. *IPSJ Transactions on Advanced Computing Systems*, Vol.5, No.1, pp.80–87, Jan. 2012.

[J7] Hiroshi Sasaki, Masaaki Kondo, Hiroshi Nakamura. Energy-efficient dynamic instruction scheduling logic through instruction grouping. *IEEE Transactions on VLSI (TVLSI)*, Vol.17 Issue 6, pp.848–852, June 2009.

Workshop papers

[W1] Satoshi Imamura, Yuichiro Yasui, Koji Inoue, Takatsugu Ono, Hiroshi Sasaki, Katsuki Fujisawa. Power-efficient breadth-first search with DRAM row buffer locality-aware address mapping. In *High Performance Graph Data Management and Processing Workshop 2016 (HPGDMP)*, pp.17–24, 2016. (held in conjunction with SC)

[W2] Jie Yin, Ye Liu, Shinpei Kato, Hiroshi Sasaki, Hiroaki Takada. An empirical study on the NoC architecture based on bidirectional ring and mesh topologies. In *2016 Workshop on Multicore and Rack-scale Systems (MaRS)*, 2016. (held in conjunction with EuroSys)

[W3] Yuan He, Hiroshi Sasaki, Shinobu Miwa, Hiroshi Nakamura. Predict-more router: a low latency NoC router with more route predictions. In *Proceedings of the 2013 IEEE International Parallel and Distributed Processing Workshops and Phd Forum (IPDPSW)*, Communication Architecture for Scalable Systems (CASS), pp.842–850, 2013.

[W4] Yuki Abe, Hiroshi Sasaki, Martin Peres, Koji Inoue, Kazuaki Murakami, Shinpei Kato. Power and performance analysis of GPU-accelerated systems. In *2012 Workshop on Power-Aware Computing and Systems (HotPower)*, 2012. (held in conjunction with OSDI)

[W5] Satoshi Imamura, Hiroshi Sasaki, Naoto Fukumoto, Koji Inoue, Kazuaki Murakami. Optimizing power-performance trade-off for parallel applications through dynamic core-count and frequency scaling. In *2nd Workshop on Runtime Environments/Systems, Layering, Virtualized Environments (RESoLVE)*, 2012. (held in conjunction with ASPLOS)

[W6] Lovic Gauthier, Farhad Mehdipour, Koji Inoue, Shinya Ueno, Hiroshi Sasaki. Efficient barrier synchronization for 2D meshed NoC-based many-core processors. In *17th Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI)*, 2012.

[W7] Hiroshi Sasaki, Takatsugu Oya, Masaaki Kondo, Hiroshi Nakamura. Power-performance modeling of heterogeneous cluster-based web servers. In *Proceedings of the 2009 20th IEEE/ACM International Conference on Grid Computing (Grid)*, pp.225–231, 2009. (presented at Energy Efficient Grids, Clouds and Clusters Workshop (E2GC2))

[W8] Toshiya Komoda, Hiroshi Sasaki, Masaaki Kondo, Hiroshi Nakamura. Compiler directed fine grain power gating for leakage power reduction in microprocessor functional units. In *Workshop on Optimizations for DSP and Embedded Systems (ODES)*, 2009. (held in conjunction with CGO)

[W9] Masaaki Kondo, Hiroshi Sasaki, Hiroshi Nakamura. Improving fairness, throughput and energy-efficiency on a chip multiprocessor through DVFS. In *ACM SIGARCH Computer Architecture News*, Vol.35, Issue 1, pp.31–38, Mar. 2007. Workshop on Design, Architecture and Simulation of Chip Multi-Processors (dasCMP), 2006. (held in conjunction with MICRO)

[W10] Hiroshi Sasaki, Masaaki Kondo, Hiroshi Nakamura. Dynamic instruction cascading on GALS microprocessor. In *International Workshop on Power And Timing Modeling, Optimization and Simulation (PATMOS)*, pp.30–39, 2005.

Book chapters

[B1] Hiroshi Sasaki, Hideharu Amano, Kimiyoshi Usami, Masaaki Kondo, Mitaro Namiki, Hiroshi Nakamura. Geyser: energy-efficient MIPS CPU core with fine-grained run-time power gating. Book Chapter in *Handbook of Energy-Aware and Green Computing* edited by Ishfag Ahmad and Sanjay Ranka, Chapman Hall/CRC Computer Information Science Series, pp.49–65, Jan. 2012.

PROFESSIONAL ACTIVITIES

Organizing committee members

- Organizer, Shonan Meeting No.134 "Advances in Heterogeneous Computing from Hardware to Software," 2018.
- Publication chair, International Conference on Parallel Architectures and Compilation Techniques (**PACT**) 2013.

Program committee members

- International Symposium on Microarchitecture (**MICRO**) 2019 (external review committee)
- International Conference on Computer Design (ICCD) 2014, 2015, 2016, 2017
- International Symposium on Workload Characterization (**IISWC**) 2016
- International Conference on Distributed Computing and Internet Technology (ICDCIT) 2015
- International Conference on Parallel Architectures and Compilation Techniques (**PACT**) 2014 (external PC)
- International Conference on Parallel and Distributed Systems (ICPADS) 2013
- International Conference on Embedded and Ubiquitous Computing (EUC) 2012, 2013
- International Workshop on Cyber-Physical Systems, Networks, and Applications (CPSNA) 2011, 2012

External reviewers

- **Conferences**

  2017 **ASPLOS, ISCA**

  2016 **ASPLOS**

  2015 **ISCA**

  2014 **ISCA, DAC, MICRO**

  2013 **MICRO**

  2012 **SC**

  2010 **ISCA**, ICS, ISLPED

  2009 ISLPED, ICCD

  2008 CF

- **Journals**

  IEEE TVLSI

  IEEE CAL

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