RAM Register Map for buffered DSP values

This table shows the register map of the first page of RAM in the SNES. The values in these registers are used to store important configuration values for the correct function of the DSP. Values that correspond to a specific register in the DSP can be transferred directly, while other values must be collected to a single byte or word and will then be transferred to the DSP. These registers are mirrored on banks $00 to $3F and again on bank $7E (according to SNES memory map). The whole map takes up 144 bytes of memory, while only 54 bytes are being used. Green marks indicate free memory. The grey area is reserved for more audio channels in future updates.

	Description	L CH Vol	R CH Vol	LO 8bit PITCH	HI 8bit PITCH	SOURCE	ADSR1	ADSR2	KEY ON	PITCH MOD	NOISE ENABLE	ECHO ENABLE	tbd	tbd
CH 1	DSP register	00	01	02	03	04	05	06					volume buffer	
	RAM address	1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	100A	100B	100C
	value range	0-7F	0-7F	0-FF	0-3F	0-255			0 / 1					
	default	7F	7F	00	01	0	FF	E0	1	0	0	0		

	Description	L CH Vol	R CH Vol	LO 8bit PITCH	HI 8bit PITCH	SOURCE	ADSR1	ADSR2	KEY ON	PITCH MOD	NOISE ENABLE	ECHO ENABLE	tbd	tbd
CH 2	DSP register	10	11	12	13	14	15	16					volume buffer	
	RAM address	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	101A	101B	101C
	value range	0-7F	0-7F	0-FF	0-3F	0-255			0 / 2					
	default	7F	7F	00	01	0	FF	E0	2	0	0	0		

	Description	L CH Vol	R CH Vol	LO 8bit PITCH	HI 8bit PITCH	SOURCE	ADSR1	ADSR2	KEY ON	PITCH MOD	NOISE ENABLE	ECHO ENABLE	tbd	tbd
CH 3	DSP register	20	21	22	23	24	25	26					volume buffer	
	RAM address	1020	1021	1022	1023	1024	1025	1026	1027	1028	1029	102A	102B	102C
	value range	0-7F	0-7F	0-FF	0-3F	0-255			0 / 4					
	default	7F	7F	00	01	0	FF	E0		0	0	0		

	Description	L CH Vol	R CH Vol	LO 8bit PITCH	HI 8bit PITCH	SOURCE	ADSR1	ADSR2	KEY ON	PITCH MOD	NOISE ENABLE	ECHO ENABLE	tbd	tbd
CH 4	DSP register	30	31	32	33	34	35	36					volume buffer	
	RAM address	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039	103A	103B	103C
	value range	0-7F	0-7F	0-FF	0-3F	0-255			0 / 8					
	default	7F	7F	00	01	0	FF	E0		0	0	0		

	X0	X1	X2	X3	X4	X5	X6	4C/5C	2D	3D	4D		
	L CH Vol	R CH Vol	LO 8bit PITCH	HI 8bit PITCH	SOURCE	ADSR1	ADSR2	KEY ON	PITCH MOD	NOISE ENABLE	ECHO ENABLE		
	00	01	02	03	04	05	06						
CH 5	0	1	2	3	4	5	6	7	8	9	10	11	12
	1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	100A	100B	100C

	X0	X1	X2	X3	X4	X5	X6	4C/5C	2D	3D	4D		
	L CH Vol	R CH Vol	LO 8bit PITCH	HI 8bit PITCH	SOURCE	ADSR1	ADSR2	KEY ON	PITCH MOD	NOISE ENABLE	ECHO ENABLE		
	00	01	02	03	04	05	06						
CH 6	0	1	2	3	4	5	6	7	8	9	10	11	12
	1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	100A	100B	100C

	X0	X1	X2	X3	X4	X5	X6	4C/5C	2D	3D	4D		
	L CH Vol	R CH Vol	LO 8bit PITCH	HI 8bit PITCH	SOURCE	ADSR1	ADSR2	KEY ON	PITCH MOD	NOISE ENABLE	ECHO ENABLE		
	00	01	02	03	04	05	06						
CH 7	0	1	2	3	4	5	6	7	8	9	10	11	12
	1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	100A	100B	100C

	X0	X1	X2	X3	X4	X5	X6	4C/5C	2D	3D	4D		
	L CH Vol	R CH Vol	LO 8bit PITCH	HI 8bit PITCH	SOURCE	ADSR1	ADSR2	KEY ON	PITCH MOD	NOISE ENABLE	ECHO ENABLE		
	00	01	02	03	04	05	06						
CH 8	0	1	2	3	4	5	6	7	8	9	10	11	12
	1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	100A	100B	100C

	Description	DSP Flags	Key ON	Key OFF	Offset	Noise	Echo	Main Volume L	Main Volume R	Echo Vol L	Echo Vol R	Flag Register	tbd	tbd
MASTER	DSP register	6C	4C	5C	5D	3D	4D	0C	1C	2C	3C	6C		
	RAM address	1080	1081	1082	1083	1084	1085	1086	1087	1088	1089	108A	108B	108C
	value range													
	default											33		

tbd	tbd	tbd
100D	100E	100F

tbd	tbd	tbd
101D	101E	101F

tbd	tbd	tbd
102D	102E	102F

tbd	tbd	tbd
103D	103E	103F

13 14 15
100D 100E 100F

13 14 15
100D 100E 100F

13 14 15
100D 100E 100F

13 14 15
100D 100E 100F

tbd	tbd	tbd
108D	108E	108F