RAM Register Map for buffered DSP values

This table shows the register map of the first page of RAM in the SNES. The values in these registers are used to store important configuration values for the correct function of the DSP. Values that correspond to a specific register in the DSP can be transfered directly, while other values must be collected to a single byte or word and will then be transferred to the DSP. These registers are mirrored on banks S00 to SSF and again on bank S7E (according to SNES memory map). The whole map takes up 144 bytes of memory, while only S4 bytes are being used. Green marks indicate free memory. The grey area is reserved for more audio channels in future updates.

	Description	L CH Vol	R CH Vol		HI 8bit PITCH		ADSR1	ADSR2	KEY ON	PITCH MOD	NOISE ENABI	E ECHO ENABL		tbd	tbd	tbd	tbd
CH1	DSP register	00	01	02	03	04	05	06					volume buffer				
	RAM address	1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	100A	100B	100C	100D	100E	100F
	value range	0-7F	0-7F	0-FF	0-3F	0-255			0/1								
	default	7F	7F	00	01	0	FF	E0	1	0	0	0					
	Description	L CH Vol	R CH Vol			SOURCE	ADSR1	ADSR2	KEY ON	PITCH MOD	NOISE ENABI	EECHO ENABL		tbd	tbd	tbd	tbd
	DSP register	10	11	12	13	14	15	16					volume buffer				
CH 2	RAM address	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	101A	101B	101C	101D	101E	101F
	value range	0-7F	0-7F	0-FF	0-3F	0-255			0/2								
	default	7F	7F	00	01	0	FF	E0	2	0	0	0					
	Description	L CILVAL	D CILVAL	LO ON A DITCH	HI 8bit PITCH	COLIDCE	ADSR1	ADSR2	KEY ON	DITCH MOD	NOICE ENABL	EECHO ENABL	- laboral	late at	tbd	tbd	late of
	Description	L CH Vol	R CH Vol		23				KEYON	PITCH MOD	NOISE ENABI	EECHO ENABL		tbd	tDa	τοα	tbd
CH 3	DSP register RAM address	20 1020	21 1021	1022	1023	24 1024	25 1025	26 1026	1027	1028	1029	1024	volume buffer 102B	1000	102D	102E	102F
CH 3	value range	0-7F	0-7F	0-FF	0-3F	0-255	1025	1026	0/4	1028	1029	102A	1026	102C	1020	102E	102F
	default	7F	7F	00	01	0-255	FF	E0	074	0	0	0		+		_	_
	uerauit	/r	11	00	lo1	U	FF	IE0	1	Į0	Į0	lo .		1			
	Description	L CH Vol	R CH Vol	I O Shit PITCH	HI 8bit PITCH	SOURCE	ADSR1	ADSR2	KEY ON	PITCH MOD	NOISE ENABI	E ECHO ENABL	Fithd	tbd	tbd	tbd	tbd
	DSP register	30	31	32	33	34	35	36			INDIOL LIVID	LLCITO LITTE	volume buffer	Lou	LDU	Lou	tou .
CH 4	RAM address	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039	103A	103B	103C	103D	103E	103F
	value range	0-7F	0-7F	0-FF	0-3F	0-255	1000	1000	0/8	2000	1000	200/1	1000	1000	1000	1002	2001
	default	7F	7F	00	01	0	FF	E0		0	0	0					
				100										1			
		X0	X1	X2	Х3	X4	X5	X6	4C/5C			4D					
							ADSR1	ADSR2	KEY ON		NOISE ENABL						
						04		06									
			1			4	5	6		8	9					14	
						1004						100A				100E	100F
		X0	X1	X2	Х3	X4	X5	X6	4C/5C			4D					
		L CH Vol	R CH Vol				ADSR1	ADSR2	KEY ON								
		00				04		06									
			1			4		6		8	9					14	
						1004						100A				100E	100F
		X0	X1	X2	ХЗ	X4	X5	X6	4C/5C		3D 4D						
		L CH Vol	R CH Vol				ADSR1	ADSR2	KEY ON		NOISE ENABLE ECHO ENABLE						
			01			04		06								1.4	
			1			4	5	6		8	9					14	
						1004						100A				100E	100F
			X1		Х3												
									KEY ON								
							05										
			1			4											
	Description	DSP Flags	Key ON	Key OFF	Offset	Noise	Echo	Main Volume L	Main Volume	R Echo Vol L	Echo Vol R	Flag Register	tbd	tbd	tbd	tbd	tbd
	DSP register	6C	4C	5C	5D	3D	4D	0C	1C	2C	3C	6C					
MASTER	RAM address	1080	1081	1082	1083	1084	1085	1086	1087	1088	1089	108A	108B	108C	108D	108E	108F
	value range																
	default											33					
	uciauit																