

## Arithmetic instructions

### Addition / subtraction

#### Addition

Opcode:-

ADD R/M

ADI 8bit data

ADC R/M

ACI 8bit data

INR R/M

INX Rp

DAD Rp

DAA - no operand

#### Substraction

SUB R/M

SUI 8bit data

SBB R/M

SBI 8bit data

DCR R/M

DCX Rp

In arithmetic group instruction, all the flags are modified as per result.

Here one content of operation is stored in Accumulator by default.

ADD R/M

REG : A,B,C,D,E,H,L

MEMORY : [HL] Content of mem loc whose add is stored in HL reg pair

Algo :  $A \leftarrow A + R/M$

Desc : This instruction is used to add content of accumulator with content of reg/mem specified in instruction, and result will be stored in accumulator.

Eg.

ADD B

$A \leftarrow A+B$

Size : 1byte

A =7E , B =9A

ADD B

↓ AC  
FE-01111110

SA-10011010

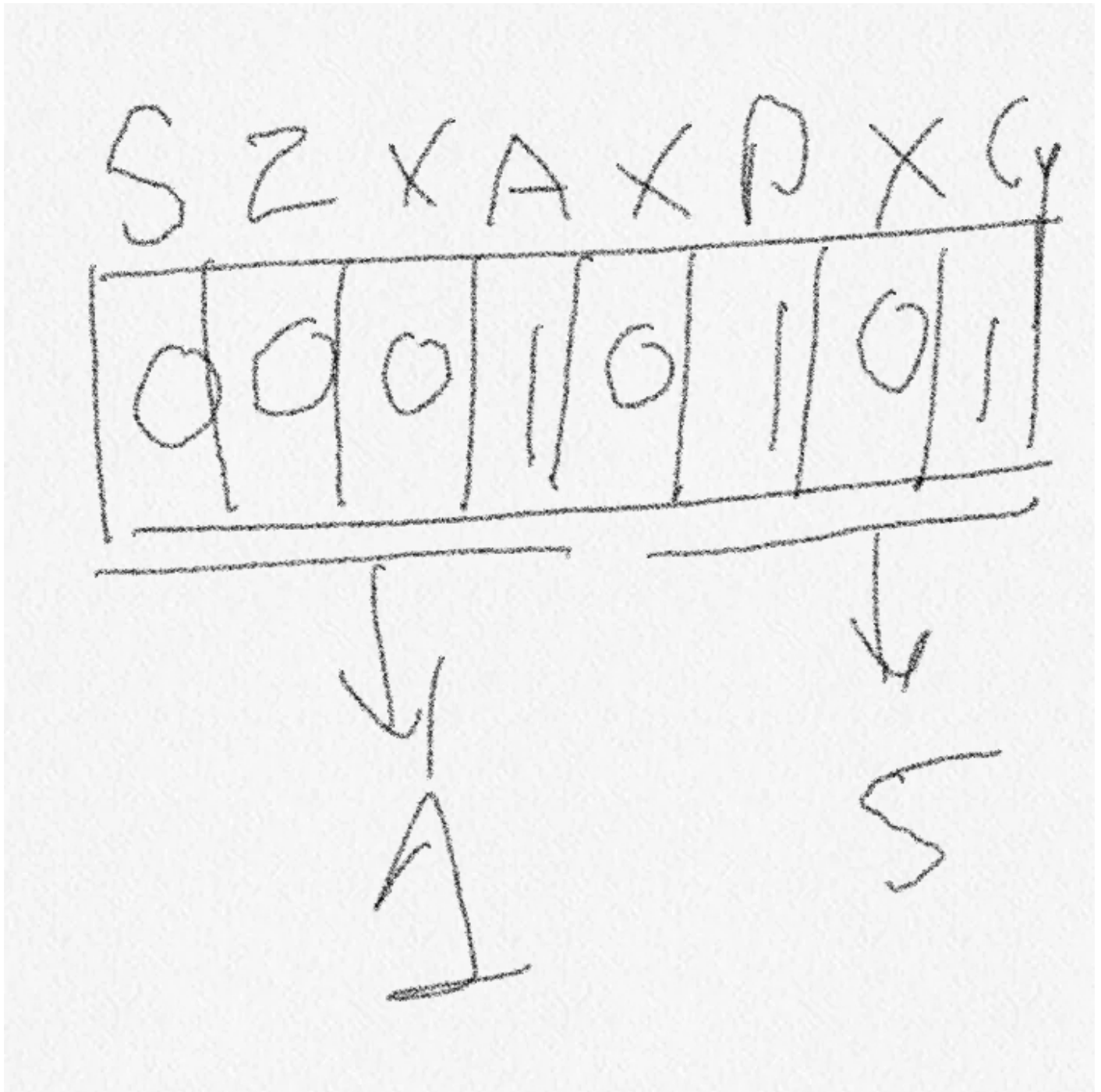
Cy → 100011000

S-0 P-1

Z-0 Cy-1

AC-1 ✓

A = 18



ADI 8bit data

$A \leftarrow A + 8\text{bit data}$

Size : 2bytes

Desc : This instruction is used to add content of accumulator with 8 bit data specified in instruction, and result will be stored into the accumulator.

$$A: \boxed{79}$$

$$+ \boxed{12}$$

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$$A = 8B$$

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67- 0 | 1 | 0 0 | 1 | 1

12 0 0 0 | 0 0 1 0

---

0 | 1 | 1 | 1 | 0 0 1

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S- 0 P- 0

AC- 0 L- 0

G- 0

ADC R/M

add with carry

Algo :  $A \leftarrow A + R/M + CY$

FOR 16 bit addition

Desc : This instruction is used to add content of accumulator with content of reg/mem specified in instruction and also add previous stage carry, and result will be stored in accumulator.

12 34

56 78

1  
2 3 4  
5 6 7 8

---

6 8 1 2

---



34 + 78

12 + 56 + prev carry

BC-579A  
DE-73B2

10011010  
10111000

101016010  
52

$$57 + 73 = 130$$

11026 1014

2

CB52

ACI 8bit data

$A \leftarrow A + 8\text{Bit data} + \text{cy}$

INR R/M

$R/M \leftarrow R/M + 01$

This instruction is used to increment the content of reg /mem specified in instruction and stored result in same reg /mem.

B =34

INR B

B=35

INX Rp

$$\begin{array}{r}
 \text{BC-12FF} \\
 + 1 + 0001 \\
 \hline
 1300
 \end{array}$$

Increment content of reg pair

DAD Rp

16 bit addition

HL  $\leftarrow$  HL + Rp

DAD B

HL  $\leftarrow$  HL + BC

1234  
5678  
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68AC