1 USB Host Controller

1.1 Overview

This chapter describes the Universal Serial Bus host controller (UHC) implemented in the JZ4740 Processor .

The Universal Serial Bus (USB) supports serial data exchanges between a host computer and a variety of simultaneously accessible peripherals. The attached peripherals share USB bandwidth through a host-scheduled, token-based protocol. Peripherals can be attached, configured, used, and detached, while the host and other peripherals continue operation.

Familiarity with the *Universal Serial Bus Specification*, Revision 1.1 and the OHCI specification are necessary to fully understand the material contained in this section

Features :

- USB Rev. 1.1 compatible
- Supports both low-speed and full-speed USB devices
- Open Host Controller Interface (OHCI) Rev 1.0 compatible
- Root hub supports two data ports

1.2 Pin Description

Table 1-1 UHC Pins Description

Name	Type	Description
DPLS0	Inout	Data Positive to Port 0
DPLS1	Inout	Data Positive to Port 1
DMNS0	Inout	Data Minus to Port 0
DMNS1	Inout	Data Minus to Port 1

1.3 Register Description

The Host Controller (HC) contains a set of on-chip operational registers which are mapped into a noncacheable portion of the system addressable space. These registers are used by the Host Controller Driver (HCD). According to the function of these registers, they are divided into four partitions, specifically for Control and Status, Memory Pointer, Frame Counter and Root Hub. All of the registers should be read and written as words.

Register Name	Description	RW	Reset Value	Address	Access Size
HcRevision	Control and Status group	R	0x00000010	0x13030000	32
HcControl		RW	0x00000000	0x13030004	32
HcCommandStatus		RW	0x00000000	0x13030008	32
HcInterruptStatus		RW	0x00000000	0x1303000C	32
HcInterruptEnable		RW	0x00000000	0x13030010	32
HcInterruptDisable		RW	0x00000000	0x13030014	32
HcHCCA	Memory pointer group	RW	0x00000000	0x13030018	32
HcPeriodCurrentED		R	0x00000000	0x1303001C	32
HcControlHeadED		RW	0x00000000	0x13030020	32
HcControlCurrentED		RW	0x00000000	0x13030024	32
HcBulkHeadED		RW	0x00000000	0x13030028	32
HcBulkCurrentED		RW	0x00000000	0x1303002C	32
HcDoneHead		R	0x00000000	0x13030030	32
HcFmInterval	Frame counter group	RW	0x00002EDF	0x13030034	32
HcFmRemaining		R	0x00000000	0x13030038	32
HcFmNumber		R	0x00000000	0x1303003C	32
HcPeriodicStart		RW	0x00000000	0x13030040	32
HcLSThreshold		RW	0x00000628	0x13030044	32
HcRhDescriptorA	Root hub group	R/W	0x02000902	0x13030048	32
HcRhDescriptorB		RW	0x00060000	0x1303004C	32
HcRhStatus		RW	0x00000000	0x13030050	32
HcRhPortStatus 1		RW	0x00000100	0x13030054	32
HcRhPortStatus 2		RW	0x00000100	0x13030058	32

Notes: *Open HCI – Open Host Controller Specification for USB* for details of the each register.

1.4 Introduction

The Host Controller is the device which is located between the USB bus and the Host Controller Driver in the OpenHCI architecture. The Host Controller is charged with processing all of the Data Type lists built by the Host Controller Driver. Additionally, the USB Root Hub is attached to the Host Controller.

The main functions as following:

- **USB States** : the Host Controller Operation with respect to the possible USB Bus states.
- **Frame Management** : all aspects of managing the 1-ms USB Frame.
- **List Processing** : the main function of the Host Controller. the detailed processing of the HCD-built Data Type lists.
- **Interrupt Processing** : the interrupt events tracked by the Host Controller and how the Host Controller provides interrupts for those events.
- **Root Hub** : the Root Hub support.