1 Camera Interface Module

1.1 Overview

The camera interface module (CIM) connects to a CMOS or CCD type image sensor. The CIM sources the digital image stream through a common parallel digital protocol. The CIM can be configured to connect directly to external image sensors and CCIR656 standard video decoders.

The CIM has the following features:

- Input image size up to 2048×2048 pixels
- Integrated DMA support
- Supports generic image data format
- Supports CCIR656 data format
- Configurable CIM_VSYNC and CIM_HSYNC signals: active high/low
- Configurable CIM_PCLK: active edge rising/falling
- 32×32 image data receive FIFO (RXFIFO)

1.2 Pin Description

Table 1-1 Camera Interface Pins Description

Name	I/O	Description
CIM_MCLK	Output	Master clock to Image Sensor
CIM_PCLK	Input	Pixel clock from Image Sensor
CIM_VSYNC	Input	VSYNC from Image Sensor
CIM_HSYNC	Input	HSYNC from Image Sensor
CIM_DATA[7:0]	Input	Data bus from Image Sensor

1.3 Register Description

The CIM has nine registers to configure camera interface and DMA operation for the input data. The table below list these registers.

Table 1-2 CIM Registers

Name	RW	Reset Value	Address	Access Size
CIMCFG	RW	0x00000000	0x13060000	32
CIMCR	RW	0x00000000	0x13060004	32
CIMST	RW	0x00000000	0x13060008	32
CIMIID	R	0x00000000	0x1306000C	32
CIMRXFIFO	R	0x????????	0x13060010	32
CIMDA	RW	0x00000000	0x13060020	32
CIMFA	R	0x00000000	0x13060024	32
CIMFID	R	0x00000000	0x13060028	32
CIMCMD	R	0x00000000	0x1306002C	32

1.3.1 CIM Configuration Register Register (CIMCFG)

CIMCFG **0x13060000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																INV_DAT	VSP	HSP	PCP	Reserved		DUMMY	E_VSYNC	Reserved	PACK			Reserved		DSM	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved		R
15	INV_DAT	Inverse every bit of input data. 0 – not inverse; 1 – inverse	RW
14	VSP	VSYNC polarity selection. When VSYNC signal is input from pin CIM_VSYNC, this bit specifies the VSYNC signal active level and leading edge. When VSYNC is retrieved from SAV&EAV, this bit is ignored. 0 – VSYNC signal active high, VSYNC signal leading edge is rising edge; 1 – VSYNC signal active low, VSYNC signal leading edge is falling edge	RW
13	HSP	Specifies the HSYNC signal active level and leading edge.	RW

<table>
<tr><td></td><td></td><td>0 – HSYNC signal active high, HSYNC signal leading edge is rising edge;
1 – HSYNC signal active low, HSYNC signal leading edge is falling edge</td><td></td></tr>
<tr><td>12</td><td>PCP</td><td>Specifies the PCLK working edge.
0 – Data is sampled by PCLK rising edge;
1 – Data is sampled by PCLK falling edge</td><td>RW</td></tr>
<tr><td>11:10</td><td>Reserved</td><td></td><td>R</td></tr>
<tr><td>9</td><td>DUMMY</td><td>DUMMY zero function. When DUMMY is 1, CIM hardware adds one byte zero to every 3 input data bytes to form 32-bit data.
0 – DUMMY zero function disabled;
1 – DUMMY zero function enabled</td><td>RW</td></tr>
<tr><td>8</td><td>E_VSYNC</td><td>External / internal VSYNC selection. When DSM is CCIR656 Progressive Mode, VSYNC can be external (provided by sensor) or internal (retrieved from SAV&EAV). This bit only valid for CCIR656 Progressive Mode; In other DSM modes, this bit is ignored.
0 – Internal VSYNC mode, pin CIM_VSYNC is ignored;
1 – External VSYNC mode, VSYNC is provided by image sensor via pin CIM_VSYNC</td><td>RW</td></tr>
<tr><td>7</td><td>Reserved</td><td></td><td>R</td></tr>
<tr><td>6:4</td><td>PACK</td><td>Data packing mode, pack 8-bit input data into 32-bit data for FIFO.
<table>
<tr><th>PACK</th><th>Description</th></tr>
<tr><td>3’b000</td><td>0x 11 22 33 44</td></tr>
<tr><td>3’b001</td><td>0x 22 33 44 11</td></tr>
<tr><td>3’b010</td><td>0x 33 44 11 22</td></tr>
<tr><td>3’b011</td><td>0x 44 11 22 33</td></tr>
<tr><td>3’b100</td><td>0x 44 33 22 11</td></tr>
<tr><td>3’b101</td><td>0x 33 22 11 44</td></tr>
<tr><td>3’b110</td><td>0x 22 11 44 33</td></tr>
<tr><td>3’b111</td><td>0x 11 44 33 22</td></tr>
</table>
In this table, 0x11, 0x22, 0x33 and 0x44 means the received data from the sensor, 0x11 is received first and 0x44 is received last.</td><td>RW</td></tr>
<tr><td>3:2</td><td>Reserved</td><td></td><td>R</td></tr>
<tr><td>1:0</td><td>DSM</td><td>Data sample mode. Please refer to the table below.
<table>
<tr><th>DSM</th><th>Description</th></tr>
<tr><td>2’b00</td><td>CCIR656 Progressive Mode</td></tr>
<tr><td>2’b01</td><td>CCIR656 Interlace Mode</td></tr>
<tr><td>2’b10</td><td>Gated Clock Mode</td></tr>
<tr><td>2’b11</td><td>Non-Gated Clock Mode</td></tr>
</table></td><td>RW</td></tr>
</table>

1.3.2 CIM Control Register (CIMCR)

CIMCR **0x13060004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MCLKDIV								Reserved				FRC				Reserved		VDDM	DMA_SOFM	DMA_EOFM	DMA_STOPM	RF_TRIGM	RF_OFM	Reserved	RF_TRIG			Reserved	DMA_EN	RF_RST	ENA
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	MCLKDIV	The parameter for master clock MCLK generation from device clock. MCLK = (Device clock) / (MCLKDIV + 1)	RW
23:20	Reserved		R
19:16	FRC	CIM frame rate control. Specifies the sampling frame data rate. If FRC = N, CIM sampling one frame of every N+1 frames from the sensor. In this way, CIM reduces the frame rate of sensor. Another way to reduce frame rate is to decrease the MCLK frequency output to the image sensor.	RW
15:14	Reserved		R
13	VDDM	The enable control bit for VDD interrupt. 0 – disable; 1 – enable	RW
12	DMA_SOFM	The enable control bit for DMA_SOF interrupt. 0 – disable; 1 – enable	RW
11	DMA_EOFM	The enable control bit for DMA_EOF interrupt. 0 – disable; 1 – enable	
10	DMA_STOPM	The enable control bit for DMA_STOP interrupt. 0 – disable; 1 – enable	RW
9	RF_TRIGM	The enable control bit for RXF_TRIG interrupt. 0 – disable; 1 – enable	RW
8	RF_OFM	The enable control bit for RXF_OF interrupt. 0 – disable; 1 – enable	RW

FRC	Description
4’b0000	Sample every frame from the sensor
4’b0001	Sample 1 frame of every 2 frames from the sensor
……	……
4’b1110	Sample 1 frame of every 15 frames from the sensor
4’b1111	Sample 1 frame of every 16 frames from the sensor

<table>
<tr><td>7</td><td>Reserved</td><td></td><td>R</td></tr>
<tr><td>6:4</td><td>RF_TRIG</td><td>Specifies the trigger value of RXFIFO.
<table>
<tr><th>RXF_TRIG</th><th>Description</th></tr>
<tr><td>0</td><td>Trigger Value is 4</td></tr>
<tr><td>1</td><td>Trigger Value is 8</td></tr>
<tr><td>2</td><td>Trigger Value is 12</td></tr>
<tr><td>3</td><td>Trigger Value is 16</td></tr>
<tr><td>4</td><td>Trigger Value is 20</td></tr>
<tr><td>5</td><td>Trigger Value is 24</td></tr>
<tr><td>6</td><td>Trigger Value is 28</td></tr>
<tr><td>7</td><td>Trigger Value is 32</td></tr>
</table></td><td>RW</td></tr>
<tr><td>3</td><td>Reserved</td><td></td><td>R</td></tr>
<tr><td>2</td><td>DMA_EN</td><td>Enable / disable the DMA function.
0 – disable DMA; 1 – enable DMA</td><td>RW</td></tr>
<tr><td>1</td><td>RF_RST</td><td>RXFIFO software reset. Setting 1 to RXF_RST can reset RXFIFO immediately. Setting 0 to RXF_RST can stop resetting RXFIFO. After reset, RXFIFO is empty.</td><td>RW</td></tr>
<tr><td>0</td><td>ENA</td><td>Enable / disable the CIM module. Setting 1 to ENA can enable CIM. When CIM is working, clear ENA to 0 can stop CIM immediately.
0 – CIM is not enabled, or disable CIM immediately;
1 – CIM is enabled, or enabling CIM</td><td>RW</td></tr>
</table>

1.3.3 CIM Status Register (CIMST)

CIMST 0x13060008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																									DMA_SOF	DMA_EOF	DMA_STOP	RF_OF	RF_TRIG	RF_EMPTY	VDD
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	0	0	0	0	0

Bits	Name	Description	RW
31:7	Reserved		R
6	DMA_SOF	When set to 1, Indicate the DMA start transferring the first data from RXFIFO to frame buffer. Can generate interrupt if CIMCR.DMA_SOFM bit is set. Writing 0 to this bit will clear it, writing 1 will be ignored.	RW
5	DMA_EOF	When set to 1, indicate the DMA complete transferring one frame data from RXFIFO to frame buffer. Can generate interrupt if CIMCR.DMA_EOFM bit is set. Writing 0 to this bit will clear it, writing 1 will be ignored.	RW
4	DMA_STOP	When set to 1, indicate the DMA complete transferring data and stop the operation. Can generate interrupt if CIMCR.DMA_STOPM bit is set. Writing 0 to this bit will clear it, writing 1 will be ignored.	RW
3	RF_OF	RXFIFO over flow. When RXFIFO over flow happens, RXF_OF is set 1. Can generate interrupt if CIMCR.RF_OFM bit is set. Writing 0 to this bit will clear it, writing 1 will be ignored.	RW
2	RF_TRIG	RXFIFO trigger. Indicates whether RXFIFO meet the trigger value or not. When the valid data number in RXFIFO reaches the trig value, RXF_TRIG is set 1; when the valid data number in RXFIFO do not reach the trig value, RXF_TRIG is set 0. Can generate interrupt if CIMCR.RF_TRIGM bit is set. 0 – RXFIFO does not meets the trigger value; 1 – RXFIFO meets the trigger value	R
1	RF_EMPTY	RXFIFO empty. Indicates whether RXFIFO is empty or not. After reset, RXFIFO is empty, and RXF_EMPTY is 1. 0 – RXFIFO is not empty; 1 – RXFIFO is empty	R
0	VDD	CIM disable done. Indicate this module is disabled after clear the CIMCR.ENA bit to disable the CIM module. Can generate interrupt if CIMCR.DMA_VDDM bit is set.	RW

		0 – CIM has not been disabled; 1 – CIM has been disabled Writing 0 to this bit will clear it, writing 1 will be ignored.	

1.3.4 CIM Interrupt ID Register (CIMIID)

CIMIID **0x1306000C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FID																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FID	Frame ID. Contains a copy of the Frame ID register (CIMFID) from the descriptor currently being processed when a DMA_SOF or DMA_EOF interrupt is generated. CIMIID is written to only when CIMCMD.SOFINT or CIMCMD.EOFINT is high. As such, the register is considered to be sticky and will be overwritten only when the associated interrupt is cleared by writing the CIM state register.	R

1.3.5 CIM RXFIFO Register (CIMRXFIFO)

CIMRXFIFO **0x13060010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	Data	This register provides a port for software to read image data directly. When the software start CIM with DMA_EN=1, this register should not be read. Otherwise, the DMA data may be damaged.	R

1.3.6 CIM Descriptor Address (CIMDA)

CIMIDA																															0x13060020
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NDA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	NDA	Hold the physical address of the next descriptor in external memory. The DMAC fetches the descriptor at this location after finishing the current descriptor. The target address Bits [3:0] must be zero to be aligned to 16-byte boundary.	RW

1.3.7 CIM Frame buffer Address Register (CIMFA)

CIMIFA																															0x13060024
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FPA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FPA	Hold the physical address of frame buffer in external memory. When starts CIM, DMA transfers data from RXFIFO to frame buffer. This address is incremented by hardware as the DMAC writes data to memory. The target address Bits [3:0] must be zero to be aligned to 16-byte boundary.	R

1.3.8 CIM Frame ID Register (CIMFID)

CIMFID																														0x13060028
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FID																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FID	Hold the ID field that describes the current frame. The particular use of this field is up to the software. This ID register is copied to the CIM Interrupt ID Register when an interrupt occurs.	R

1.3.9 CIM DMA Command Register (CIMCMD)

CIMFID																														0x1306002C
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SOFINT	EOFINT	Reserved	STOP	Reserved				LEN																							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	SOFINT	DMA start transferring frame data interrupt. When set to 1, the DMA sets the start of frame bit (CIMSTATE.DMA_SOF) when start transferring image data.	R
30	EOFINT	DMA end transferring frame data interrupt. When set to 1, the DMA sets the end of frame bit (CIMSTATE.DMA_EOF) when complete transferring image data.	R
29	Reserved		R
28	STOP	DMA stop. When DMA complete transferring data, STOP bit decides whether DMA should loading next descriptor or not. 0 – DMA start loading next descriptor; 1 – DMA stopped, and CIMSTATE.DMA_STOP bit is set 1 by hardware	R
27:24	Reserved		R
23:0	LEN	Length of transfer in words. Indicate the number of words to be	R

		transferred by DMA. LEN = 0 is not valid. DMA transfers data according to LEN. Each time one or more word(s) been transferred, LEN is decreased automatically.	

1.4 CIM Data Sampling Modes

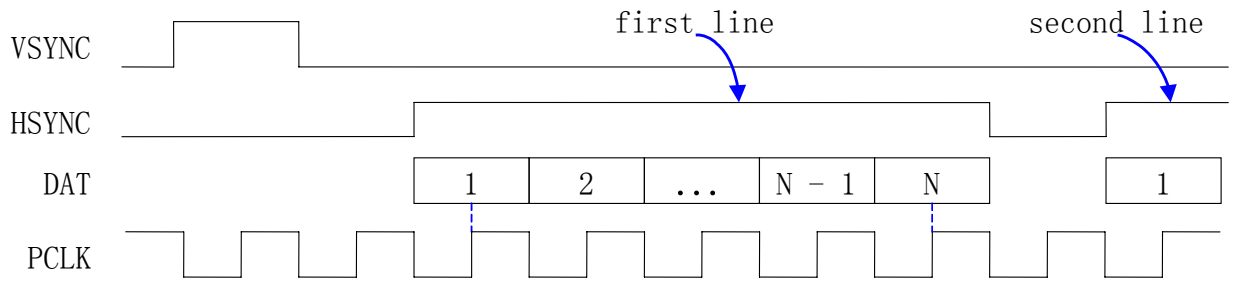
This module support 4 data sampling mode:

1. Gated Clock Mode
2. Non-Gated Clock Mode
3. CCIR656 Interlace Mode
4. CCIR656 Progressive Mode

1.4.1 Gated Clock Mode

CIM_VSYNC, CIM_HSYNC, and CIM_PCLK signals are used in this mode.

A frame start with VSYNC leading edge, then HSYNC goes active and holds the entire line. Data is sampled at the valid edge of PCLK when HSYNC is active; That means, HSYNC functions like “data enable” signal. Please refer to the figure below.



Gated Clock Mode

The VSYNC leading edge, HSYNC active HIGH or LOW, PCLK valid edges are programmable.

1.4.2 Non-Gated Clock Mode

CIM_VSYNC and CIM_PCLK signals are used in this mode. CIM_HSYNC signal is ignored.

A frame starts with VSYNC leading edge, and samples data at every PCLK valid edge. Please refer to the figure below.

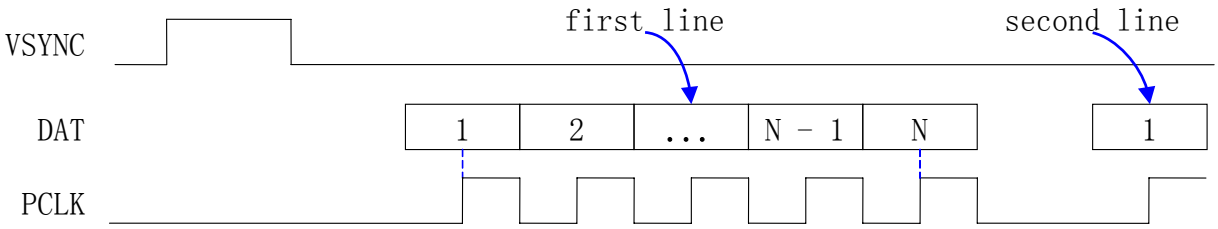


Figure 1-1 Non-Gated Clock Mode

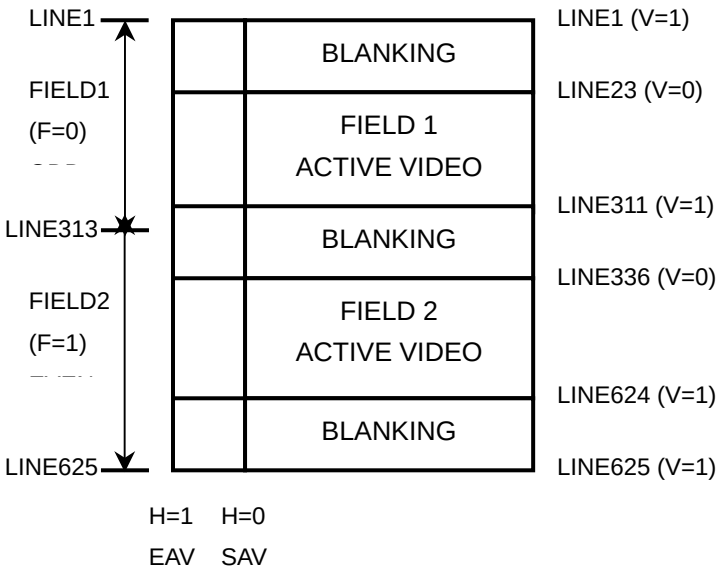
1.4.3 CCIR656 Interlace Mode

CIM_PCLK and CIM_DAT signals are used in this mode, CIM_VSYNC, CIM_HSYNC signals are ignored.

CIM utilizes the SAV & EAV code within CCIR656 data stream to get active video data.

The following diagrams and tables are quoted from CCIR656 standard. Only the PAL format is shown. CIM supports both NTSC and PAL formats. For more information about CCIR656, please refer to CCIR656 standard.

1.4.3.1 PAL Vertical Timing



LINE NUMBER	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

Figure 1-2 Typical BT.656 Vertical Blanking Intervals for 625/50 Video Systems

1.4.3.2 PAL Horizontal Timing

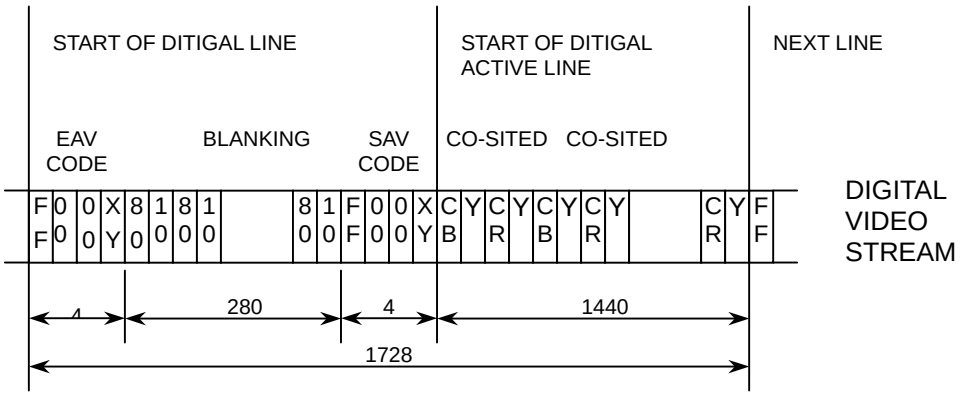


Figure 1-3 BT.656 8-BIT Parallel Interface Data Format for 625/50 Video Systems

1.4.3.3 Coding for SAV and EAV

Data Pin Number	1st Byte 0xFF	2nd Byte 0x00	3rd Byte 0x00	4th Byte 0xXY
7 (MSB)	1	0	0	1
6	1	0	0	F
5	1	0	0	V
4	1	0	0	H
3	1	0	0	P3
2	1	0	0	P2
1	1	0	0	P1
0 (LSB)	1	0	0	P0

1.4.3.4 Coding for Protection Bits

F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

1.4.4 CCIR656 Progressive Mode

CIM_PCLK and CIM_DAT signals are used in this mode. CIM_HSYNC signal is ignored.

CIM_VSYNC is optional in this mode. When the start of frame information is retrieved from SAV and EAV, it is known as internal VSYNC mode. When CIM_VSYNC is provided by sensor directly, it is known as external VSYNC mode. CIM supports both internal and external VSYNC modes.

CCIR656 Progressive Mode is a kind of Non-Interlace Mode. The image data are encoded within only one field. The F-bit of SAV and EAV are ignored. Most sensors support CCIR656 Progressive Mode.

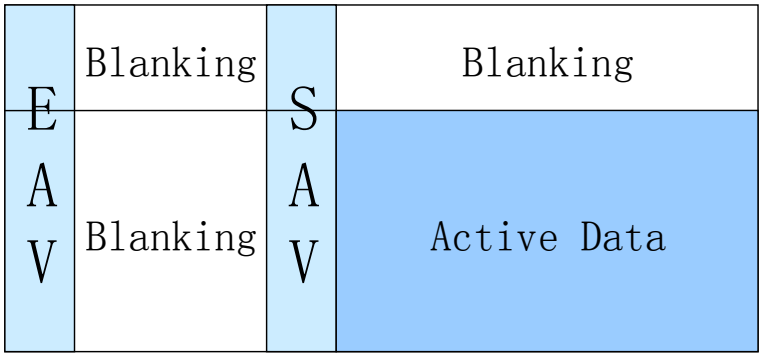


Figure 1-4 CCIR656 Progressive Mode

1.5 DMA Descriptors

A DMA descriptor is a 4-word block corresponding to the four DMA registers – CIMDA, CIMFA, CIMFID, and CIMCMD, aligned on 4-word (16-byte) boundary, in external memory:

word [0] contains the physical address for next CIMDA
word [1] contains the physical address for CIMFA
word [2] contains the value for CIMFID
word [3] contains the value for CIMCMD

Software must write the physical address of the first descriptor to CIMDA before enabling the CIM. Once the CIM is enabled, the first descriptor is read, and all 4 registers are written by the DMAC. The next DMA descriptor pointed to by CIMDA is loaded into the registers after all data for the current descriptor has been transferred.

Note: If only one frame buffer is used in external memory, the CIMDA field (word [0] of the DMA descriptor) must point back to itself. That is to say, the value of CIMDA is the physical address of itself.

1.6 Interrupt Generation

CIM has next interrupt sources:

- RXFIFO FULL Interrupt (RF_TRIG)
  When the valid data number of RXFIFO reaches trigger value, CIMST.RF_TRIG bit is set. At the same time, if RF_TRIGM is 1, RF_TRIG interrupt is generated.

- RXFIFO Over Flow Interrupt (RF_OF)
  When the valid data number of RXFIFO reaches 32 and one more data are written to RXFIFO, CIMST.RF_OF bit is set. At the same time, if RF_OFM is 1, RF_OF interrupt is generated.

- DMA Start Of Frame Data Transferring Interrupt (DMA_SOF)
  When the CIMCMD.SOFINT bit is 1 and DMA start transferring the first data from RXFIFO to frame buffer, CIMST.DMA_SOF bit is set. At the same time, if DMA_SOFM is 1, DMA_SOF interrupt is generated.

- DMA End Of Frame Data Transferring Interrupt (DMA_EOF)
  When the CIMCMD.EOFINT bit is 1 and DMA complete transferring the last data from RXFIFO to frame buffer, CIMST.DMA_EOF bit is set. At the same time, if DMA_EOFM is 1, DMA_EOF interrupt is generated.

- DMA Stop Transferring Interrupt (DMA_STOP)
  When the CIMCMD.STOP bit is 1 and DMA complete transferring the last data from RXFIFO to frame buffer, CIMST.DMA_STOP bit is set. At the same time, if DMA_STOPM is 1, DMA_STOP interrupt is generated.

- CIM Disable Done Interrupt (VDD)
  When disable the module by clearing the CIMCR.ENA, the module should be disabled after transferring current valid data. Then set the CIMST.VDD bit, at the same time, if VDDM is set, VDD interrupt is generated.

1.7 Software Operation

1.7.1 Enable CIM with DMA

1. Configure register CIMCFG;
2. Prepare frame buffer and descriptors;
3. Configure register CIMDA;
4. Write 0 to register CIMSTATE; // clear state register
5. Configure register CIMCTRL with DMA_EN=1, RXF_RST=1, ENA=0;// resetting RXFIFO
6. Configure register CIMCTRL with DMA_EN=1, RXF_RST=0, ENA=0;// stop resetting RXFIFO
7. Configure register CIMCTRL with DMA_EN=1, RXF_RST=0, ENA=1;// enable CIM

1.7.2 Enable CIM without DMA

1. Configure register CIMCFG;
2. Write 0 to register CIMSTATE; // clear state register
3. Configure register CIMCTRL with DMA_EN=0, RXF_RST=1, ENA=0;// resetting RXFIFO
4. Configure register CIMCTRL with DMA_EN=0, RXF_RST=0, ENA=0;// stop resetting RXFIFO
5. Configure register CIMCTRL with DMA_EN=0, RXF_RST=0, ENA=1;// enable CIM

1.7.3 Disable CIM

Method 1:

1. Configure register CIMCTRL with RXF_RST=0, ENA=0; // quick disable
2. Write 0 to register CIMSTATE; // clear state register

Method 2:

When DMA is enabled, the following sequence is recommended:

1. Configure descriptor with STOP = 1;
2. Wait DMA_STOP interrupt, when it occurs, write 0 to CIMCTRL.ENA.
3. Write 0 to register CIMSTATE; // clear state register