1 Smart LCD Controller

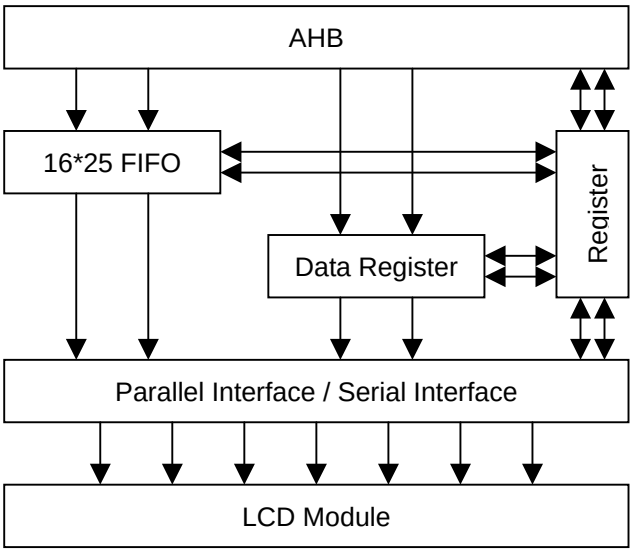
1.1 Overview

The Smart LCD Controller transfers data from the display buffer to the LCD Module. It supports DMA operation and register operation.

Features:

- Supports a large variety of LCD Module from different vendors.
- Supports parallel and serial interfaces.
- Supports different size of display panel.
- Supports different width of pixel data.
- Supports DMA operation and register operation.
- Supports Write Operation. Read Operation is not supported.

1.2 Structure



1.3 Pin Description

Table 1-1 SLCD Pins Description

Name	I/O	Description	Interface
SLCD_RS	O	Command/Data Select Signal. The polarity of the signal can be programmable.	Serial: RS Parallel: RS
SLCD_CS	O	Chip Select Signal. The polarity of the signal can be programmable.	Serial: CS Parallel: Sample Data with the edge of CS
SLCD_CLK	O	The clock of SLCD. The polarity of the clock can be programmable.	Serial or not used
SLCD_DAT*1 [17:0]	O	The data of SLCD.	Serial: SLCD_DAT [15] Parallel: SLCD_DAT [17:0] SLCD_DAT [15:0] SLCD_DAT [7:0]

Note*1: SLCD_DAT [15] is also use as data pin for serial. The SLCD pins are shared with LCDC. You can see the set of register LCDCFG.LCDPIN in LCDC spec.

1.4 Register Description

In this section, we will describe the registers in Smart LCD controller. Following table lists all the registers definition. All register's 32bit address is physical address. And detailed function of each register will be described below.

Name	Description	RW	Reset Value	Address	Access Size
MCFG	SLCD Configure Register	RW	0x0000	0x130500A0	32
MCTRL	SLCD Control Register	RW	0x00	0x130500A4	8
MSTATE	SLCD Status Register	RW	0x00	0x130500A8	8
MDATA	SLCD Data Register	RW	0x00000000	0x130500AC	32
MFIFO	SLCD FIFO	RW	0x00000000	0x130500B0	32

1.4.1 SLCD Configure Register (MCFG)

The register MCFG is used to configure SLCD.

MCFG **0x130500A0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRIGGER		Reserved	DWIDTH			CWIDTH		Reserved			CSPLY	RSPLY	Reserved	CLKPLY	TYPE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:14	TRIGGER	FIFO trigger for DMA Operation. Trigger Length Selection **TRIGGER** / Trigger Length: 00 – 4 word; 01 – 8 word; 10 – Reserved; 11 – Reserved	RW
13	Reserved	These bits always read 0, and written are ignored.	R
12:10	DWIDTH[*1]	Data Width. **DWIDTH** / **Data Width**: 000 – 18-bit once Parallel/Serial; 001 – 16-bit once Parallel/Serial; 010 – 8-bit third time Parallel; 011 – 8-bit twice Parallel; 100 – 8-bit once Parallel/Serial; 111 – 9-bit twice Parallel; 101~110 – Reserved	RW
9:7	CWIDTH[*1]	Command Width. **CWIDTH** / **Command Width**: 00 – 16-bit once; 01 – 8-bit once; 10 – 18-bit once; 11 – Reserved	RW
7:5	Reserved	These bits always read 0, and written are ignored.	R
4	CSPLY	CS Polarity. (CS initial level will be different from CS Polarity) 0: Active Level is Low 1: Active Level is High	RW
3	RSPLY	RS Polarity. 0: Command RS = 0, Data RS = 1	RW

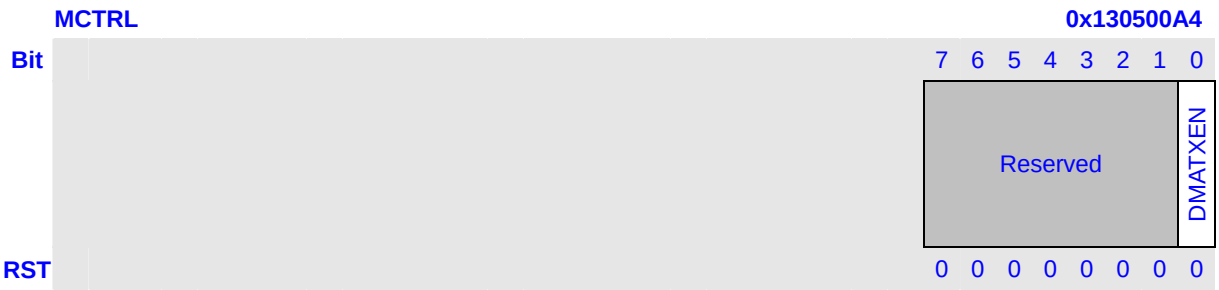
		1: Command RS = 1, Data RS = 0	
2	Reserved	These bits always read 0, and written are ignored.	R
1	CLKPLY	LCD_CLK Polarity. 0: Active edge is Falling 1: Active edge is Rising	RW
0	TTYPE	Transfer Type: 0: Parallel 1: Serial	RW

Note*1: The set of DWIDTH and CWIDTH should keep to the rules as follows:

Interface Mode	Command Width	Data Width	Color
Parallel	18-bit	18-bit once	
	16-bit	16-bit once	
		9-bit twice	
	8-bit	8-bit once	
		8-bit twice	
		8-bit third times	
Serial	18-bit	18-bit once	
	16-bit	16-bit once	
	8-bit	8-bit once	
		8-bit twice	
		8-bit third times	

1.4.2 SLCD Control Register (MCTRL)

MCTRL is SLCD Control Register.



Bits	Name	Description	RW
7:1	Reserved	These bits always read 0, and written are ignored.	R
0	DMATXEN	SLCD DMA Transfer Enable. This bit is only used for DMA automatic transfer.	RW

		(1) This bit starts the automatic transfer of image data from system memory to LCDM. (2) When DMAC finishes transferring the data, and the MSTATE.BUSY bit is 0, you can clear DMATXEN bit to stop DMA mode.	

1.4.3 SLCD Status Register (MSTATE)

The register of MSTATE is SLCD status register.

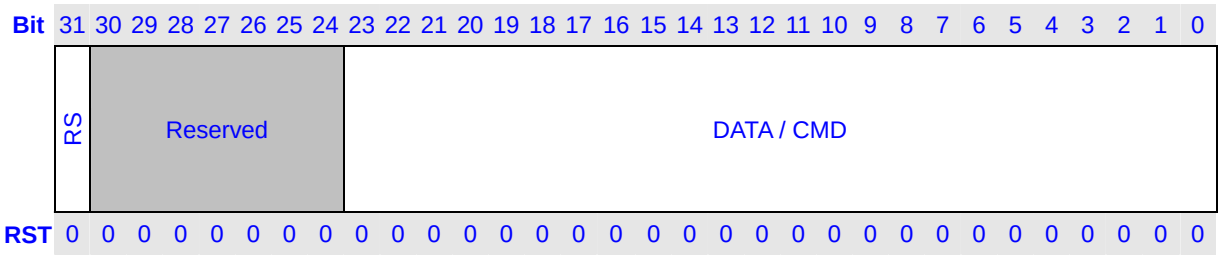
MSTATE **0x130500A8**

Bits	Name	Description	RW
7:1	Reserved	These bits always read 0, and written are ignored.	R
0	BUSY	Transfer is working or not. This bit will be set to 1 when transfer is working. It will be cleared by hardware when transfer is finished. 0: not busy 1: busy	RW

1.4.4 SLCD Data Register (MDATA)

The register MDATA is used to send command or data to LCM. When RS=0, the low 24-bit is used as command. When RS=1, the low 24-bit is used as data.

MDATA **0x130500AC**

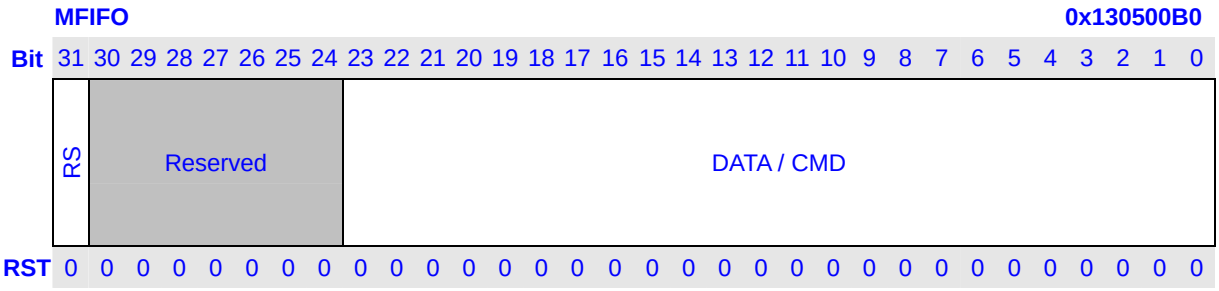


Bits	Name	Description	RW
31	RS	The RS bit of data register is used to decide the meanings of the low 24-bit.	RW

		0: data 1: command	
30:24	Reserved	These bits always read 0, and written are ignored.	R
23:0	DATA/CMD	Data or Command Register.	RW

1.4.5 SLCD FIFO (MFIFO)

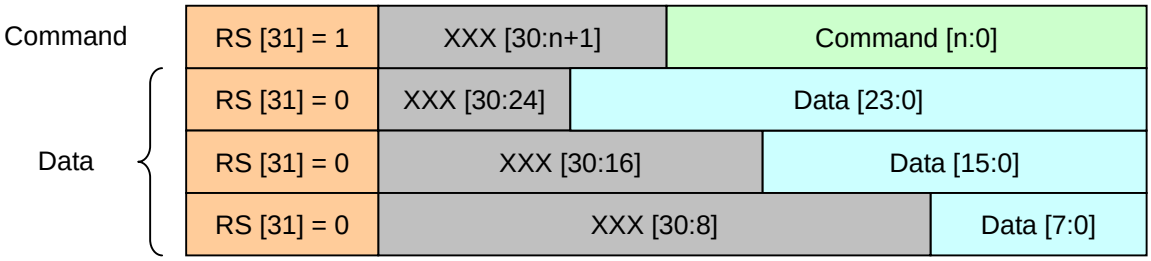
The FIFO is used to send command or data to LCM. When RS=0, the low 24-bit is used as command. When RS=1, the low 24-bit is used as data.



Bits	Name	Description	RW
31	RS	The RS bit of FIFO is used to decide the meanings of the low 24-bit. 0: data 1: command	RW
30:24	Reserved	These bits always read 0, and written are ignored.	R
23:0	DATA/CMD	Data or Command Register.	RW

1.5 System Memory Format

The format of Command and Data in system memory is as follows:



1.5.1 Data format

(1) 24-bit color

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	X	X	X	X	X	X	X	R7	R6	R5	R4	R3	R2	R1	R0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

(2) 18-bit color

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	X	X	X	X	X	X	X	R5	R4	R3	R2	R1	R0	X	X
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
G5	G4	G3	G2	G1	G0	X	X	B5	B4	B3	B2	B1	B0	X	X

(3) 16-bit color

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

(4) 8-bit color

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	C7	C6	C5	C4	C3	C2	C1	C0

1.5.2 Command Format

(1) 18-bit command

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	X	X	X	X	X	X	X	X	X	X	X	X	X	C17	C16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

(2) 16-bit command

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

(3) 8-bit command once

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	C7	C6	C5	C4	C3	C2	C1	C0

(4) 8-bit command twice (Command = command part + data part, twice transfer)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	C7	C6	C5	C4	C3	C2	C1	C0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	D7	D6	D5	D4	D3	D2	D1	D0

Note: The command is made up of command part and data part, but need twice transfer, and the first transfer is command part and the second transfer is data part. You need to divide the command into two parts by software.)

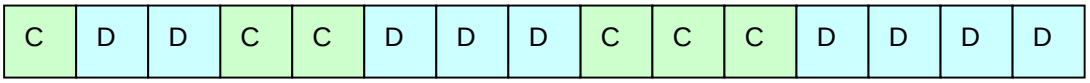
1.6 Transfer Mode

Two transfer modes can be used: DMA Transfer Mode and Data Register Transfer Mode.

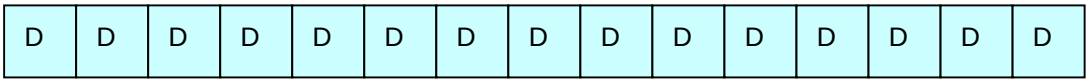
1.6.1 DMA Transfer Mode

Command and data can be recognized by RS bit coming from memory. The format of DMA transfer can be as follows:

(1) Command and Data

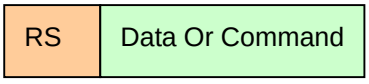


(2) Only Data



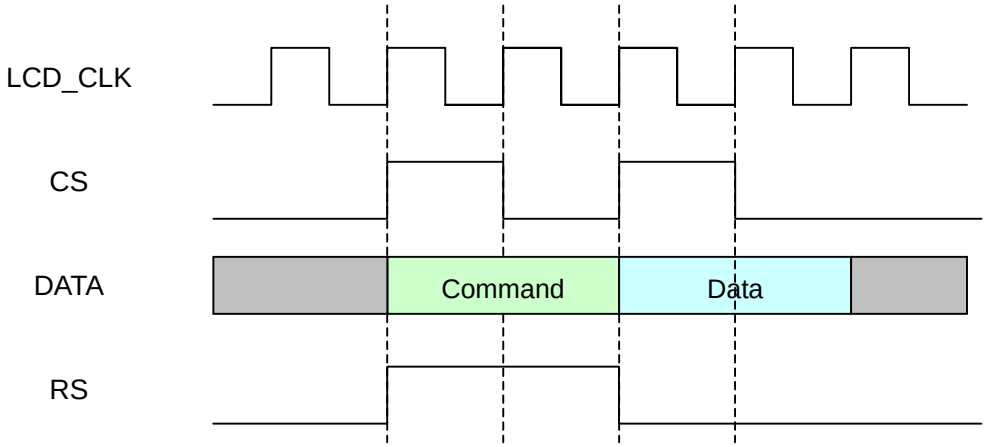
1.6.2 Register Transfer Mode

Each time you can write a command or a data to the register, then it will transfer the RS signal and data or command to LCM. Command and data can be recognized by RS bit coming from data register. The format of data register transfer can be as follows:

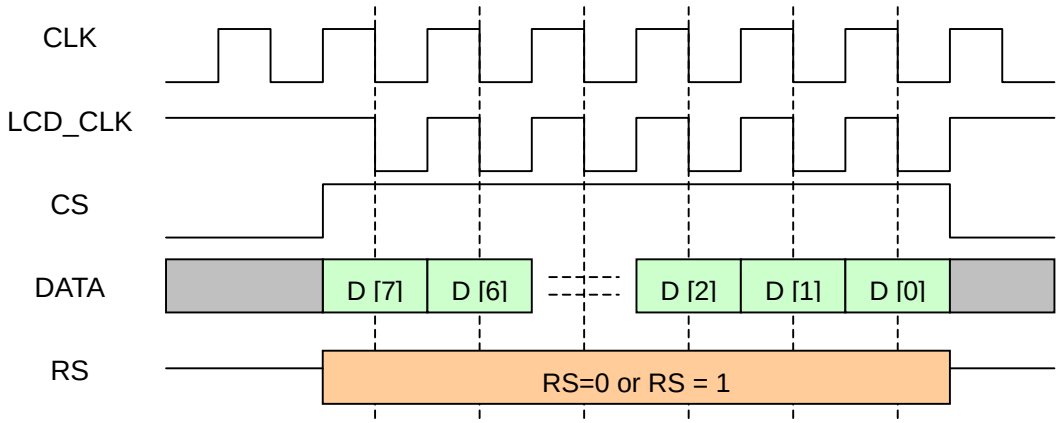


1.7 Timing

1.7.1 Parallel Timing



1.7.2 Serial Timing



1.8 Operation Guide

1.8.1 DMA Operation

(1) Start DMA transfer

(1) Initial DMAC.

(2) Set MCFG to configure SLCD.

(3) Before starting DMA, Wait for MSTATE.BUSY == 0.

(4) Set MCTRL.DMATXEN to 1 to start DMA transfer. (If you don't want to stop DMA transfer, you need not to check MSTATE.BUSY.)

(2) Stop DMA transfer

(1) Check the status of DMAC, and stop DMAC.

(2) Wait MSTATE.BUSY == 0

(3) Set MCTRL.DMATXEN to 0 to stop DMA transfer.

(3) Restart DMA transfer

When MCTRL.DMATXEN is set to 0, and then you want to restart DMA transfer at once, you should ensure that MCTRL.DMATXEN must keep low level at least three cycles of PIXCLK.

1.8.2 Register Operation

(1) Set MCFG to configure SLCD.

(2) Wait for MSTATE.BUSY == 0.

(3) Set MDATA register.

(4) Wait for MSTATE.BUSY == 0.

(5) Set MDATA register.

(6) Wait for MSTATE.BUSY == 0.

(7) … …