Jz4740

32 Bits Microprocessor

Data Sheet

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北京君正集成电路有限公司
Ingenic Semiconductor Co. Ltd

Jz4740 32 Bits Microprocessor

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Release history

Date	Revision	Change
Mar. 2007	0.1	First version, pre-release
Mar. 2007	0.2	Change for RTC: input/output pins PWRON_, WKUP_, PPRST_ and scan chain in/out
Apr. 2007	0.3	Add reset/boot descriptions
Apr. 2007	0.4	Fix BGA193 pin placement bug

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Content

1 Overview 3
1.1 Block Diagram 3
1.2 Features 4
1.2.1 CPU Core 4
1.2.2 Memory Sub-system 4
1.2.3 System Peripherals 4
1.2.4 Human Interface Peripherals 5
1.2.5 Storage Peripherals 6
1.2.6 Connectivity & Communication Peripherals 7
1.3 Characteristic 9
2 Packaging and Pinout Information 10
2.1 Overview 10
2.2 Solder Process 10
2.3 Package 11
2.4 Pin Description 13
3 Electrical Specifications 22
3.1 Absolute Maximum Ratings 22
3.2 Recommended operating conditions 23
3.3 DC Specifications 25
3.4 Characteristics of CODEC 27
3.5 Power Consumption Specifications 28
3.6 AC Specifications 30
3.7 Oscillator Electrical Specifications 30
3.7.1 32.768KHz Oscillator Specifications 30
3.7.2 EXCLK Oscillator Specifications 30
3.8 Power On, Reset and BOOT 31
3.8.1 Power-On Timing 31
3.8.2 Reset procedure 32
3.8.3 BOOT 32
3.9 Memory Bus AC Specifications 33
3.10 Peripheral Module AC Specifications 33
3.10.1 LCD Module Timing 33
3.10.2 CIM Module Timing 33
3.10.3 SPI Module Timing 33
3.10.4 External DMA Request and Grant 33

1 Overview

Jz4740 is a 32 Bits RISC processor targeting for mobile A/V and E-Learning applications. Incorporate the JzRISC core based on leading microarchitecture technology, this processor provides high integration, high performance and low power consumption solution for embedded device.

The JzRISC is the advanced and power-efficient 32-bit RISC core with 16K I-Cache and 16K D-Cache in this processor, operating at speeds up to 400MHz. On-chip modules such as LCD controller, embedded audio CODEC, embedded multi-channel SAR-ADC, AC97/I2S controller and camera interface offer designers a rich suite of peripherals for multimedia application. The memory interface supports a variety of memory types that allow flexible design requirements, include the glueless connection to SLC/MLC NAND Flash for cost sensitive applications. WLAN, Bluetooth and expansion options are provided through the USB 1.1 and MMC/SD host controllers. And the other peripherals such as USB 2.0 device, UART and SPI as well as general-system resources provide enough compute and connectivity capability for many applications. For the processor block diagram, refer to Figure 1-1.

1.1 Block Diagram

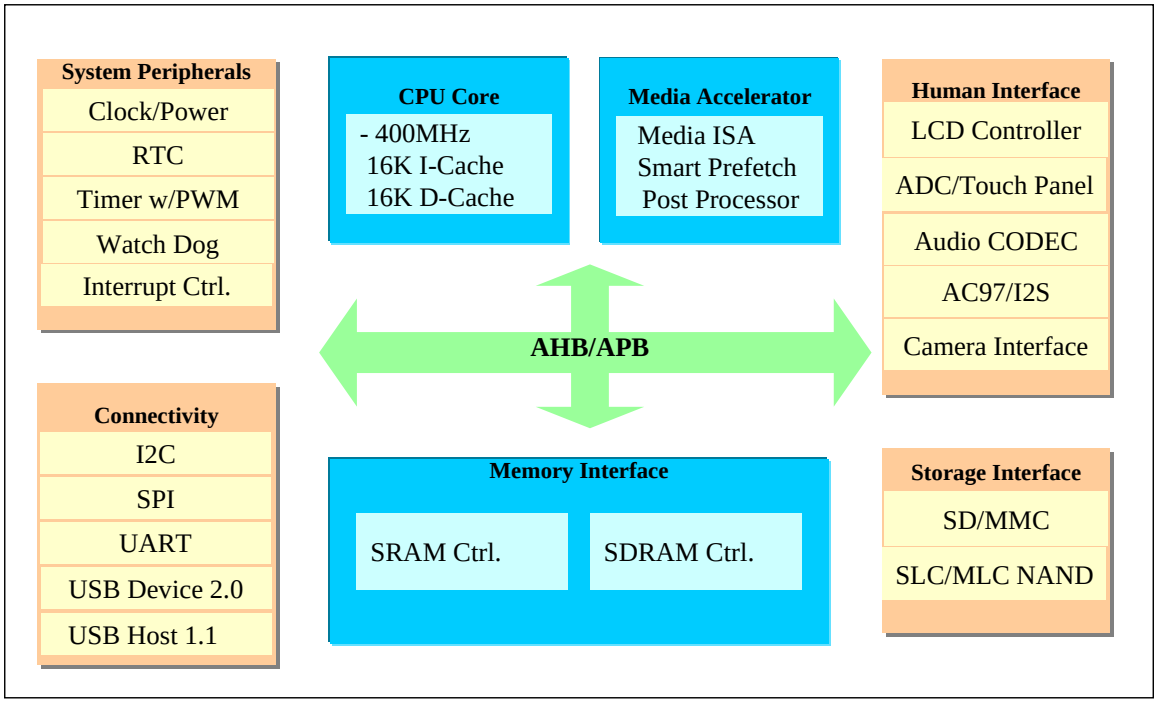


Figure 1-1 Jz4740 Diagram

1.2 Features

1.2.1 CPU Core

- 32-bit RISC CPU, clock up to 400MHz
- Low power consumption: < 0.5mW/MHz
- 16K I-Cache & 16K D-Cache
- MMU support with I-TLB, D-TLB and J-TLB
- Hardware Debug support via JTAG port
- With MXU to support media accelerattion extension instructions
- With smart prefect to accelerate media applications

1.2.2 Memory Sub-system

- Static memory interface
  - Direct interface to SRAM, ROM, Burst ROM, and NOR Flash
  - Six chip-select pin for static memory, each can be configured separately
  - Support 8, 16 or 32 bits data width
  - The size and base address of static memory banks are programmable
- NAND Flash interface
  - Support MLC NAND as well as SLC NAND
  - Support all 8-bit/16-bit NAND Flash devices regardless of density and organization
  - HAMMING and RS Hardware ECC
  - Support automatic boot up from NAND Flash devices
- Synchronous DRAM Interface
  - 1 banks with programmable size and base address
  - 32-bit and 16-bit data bus width is supported
  - Multiplexes row/column addresses according to SDRAM capacity
  - Two-bank or four-bank SDRAM is supported
  - Supports auto-refresh and self-refresh functions
  - Supports power-down mode to minimize the power consumption of SDRAM
  - Supports page mode
- Direct Memory Access Controller
  - Six independent DMA channels
  - Descriptor supported
  - Transfer data units: 8-bit, 16-bit, 32-bit, 16-byte or 32-byte
  - Transfer requests can be: auto-request within DMA; and on-chip peripheral module request
  - Interrupt on transfer completion or transfer error
  - Supports two transfer modes: single mode or block mode
- The Jz4740 processor system supports little endian only

1.2.3 System Peripherals

- General-Purpose I/O ports

  - Total GPIO pin number is 124
  - Each pin can be configured as general-purpose input or output or multiplexed with internal chip functions
  - Each pin can act as a interrupt source and has configurable rising/falling edge or high/low level detect manner, and can be masked independently
  - Each pin can be configured as open-drain when output
  - Each pin can be configured as internal resistor pull-up
- Clock generation and power management
  - On-chip oscillator circuit for an 32768Hz clock and an 12MHz clock
  - One On-chip phase-locked loops (PLL) with programmable multiple-ratio. Internal counter are used to ensure PLL stabilize time
  - PLL on/off is programmable by software
  - ICLK, PCLK, SCLK, MCLK and LCLK frequency can be changed separately for software by setting division ratio
  - Supports six low-power modes and function: NORMAL mode; DOZE mode; IDLE mode; SLEEP mode; HIBERNATE mode; and MODULE-STOP function.
- Interrupt controller
  - Total 28 maskable interrupt sources from on-chip peripherals and external request through GPIO ports
  - Interrupt source and pending registers for software handling
  - Unmasked interrupts can wake up the chip in sleep or standby mode
- Timer and counter unit with PWM output
  - Provide eight separate channels
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - PWM output supported
- Watchdog timer
  - 16-bit counter in RTC clock with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Generate power-on reset
- RTC (Real Time Clock)
  - 32-bit second counter
  - 1Hz from 32768hz
  - Alarm interrupt
  - Independent power
  - A 32-bits scratch register used to indicate whether power down happens for RTC power

1.2.4 Human Interface Peripherals

- LCD controller
  - Single-panel display in active mode, and single- or dual-panel displays in passive mode

- 2, 4, 16 grayscales and up to 4096 colors in STN mode
- 2, 4, 16, 256, 4K, 32K, 64K, 256K and 16M colors in TFT mode
- 18 bit data bus support 1,2,4,8 pins STN panel, 16bit and 18bit TFT and 8bit I/F TFT
- Display size up to 800×600 pixels
- 256×16 bits internal palette RAM
- Support ITU601/656 data format
- Support smart LCD (SRAM-like interface LCD module)

- AC97/I2S controller
  - Supports 8, 16, 18, 20 and 24 bit for sample for AC-link and I2S/MSB-Justified format
  - DMA transfer mode support
  - Support variable sample rate mode for AC-link format
  - Power down mode and two wake-up mode support for AC-link format
  - Programmable Interrupt function support
  - Support the embedded CODEC

- Camera interface
  - Input image size up to 2048×2048 pixels
  - Supports CCIR656 data format
  - 32×32 image data receive FIFO with DMA support

- Embedded Audio CODEC
  - 18-bit DAC, SNR: 88dB
  - 16-bit ADC, SNR: 85dB
  - Sample rate: 8/11.025/12/16/22.05/24/32/44.1/48kHz
  - L/R channels line input
  - MIC input
  - L/R channels headphone output amplifier support up to 32ohm load

- SADC
  - 12-bit, 2Mbps, SNR@500kHz is 61dB, THD@500kHz is -71dB
  - XP/XN, YP/YN inputs for touch screen
  - Battery voltage input
  - 1 generic input Channel

1.2.5 Storage Peripherals

- MultiMedia Card/Secure Digital Controller
  - Compliant with “The MultiMediaCard System Specification version 3.3”
  - Compliant with “SD Memory Card Specification version 1.01” and “SDIO Card Specification version 1.0” with 1 command channel and 4 data channels
  - 20~80 Mbps maximum data rate

- Supports up to 10 cards (including one SD card)
- Maskable hardware interrupt for SD I/O interrupt, internal status, and FIFO status

- NAND Flash Controller
  - Incorporated in memory controller
  - Support SLC/MLC NAND flash
  - Hardware RS and HAMMING ECC engine

1.2.6 Connectivity & Communication Peripherals

- I2C bus interface
  - Only supports single master mode
  - Supports I2C standard-mode and F/S-mode up to 400 kHz
  - Double-buffered for receiver and transmitter
  - Supports general call address and START byte format after START condition

- Synchronous serial interface
  - Supports three formats: TI's SSP, National Microwire, and Motorola's SPI
  - Configurable 2 - 17 (or multiples of them) bits data transfer
  - Full-duplex/transmit-only/receive-only operation
  - Supports normal transfer mode or Interval transfer mode
  - Programmable transfer order: MSB first or LSB first
  - 17-bit width, 128-level deep transmit-FIFO and receive-FIFO
  - Programmable divider/prescaler for SSI clock
  - Back-to-back character transmission/reception mode
  - Up to 60M bps

- UART
  - 5, 6, 7 or 8 data bit operation with 1 or 1.5 or 2 stop bits, programmable parity (even, odd, or none)
  - 16x8bit FIFO for transmit and 16x11bit FIFO for receive data
  - Interrupt support for transmit, receive (data ready or timeout), and line status
  - Supports DMA transfer mode
  - Provide complete serial port signal for modem control functions
  - Support slow infrared asynchronous interface (IrDA)
  - IrDA function up to 115200bps baudrate
  - UART function up to 921.6Kbps baudrate

- USB host interface
  - Open Host Controller Interface (OHCI)-compatible and USB Revision 1.1-compatible

- USB device interface
  - Compliant with USB protocol revision 2.0
  - High speed and full speed supported

- Embedded USB 2.0 PHY

1.3 Characteristic

Item	Characteristic
Process Technology	0.18um CMOS
Power supply voltage	I/O: 3.3 ± 0.3V Core: 1.8 ± 0.2
Package	193 BGA 13mm * 13mm
Operating frequency	336 – 400MHz
Power consumption	250mw @ 400MHz

2 Packaging and Pinout Information

2.1 Overview

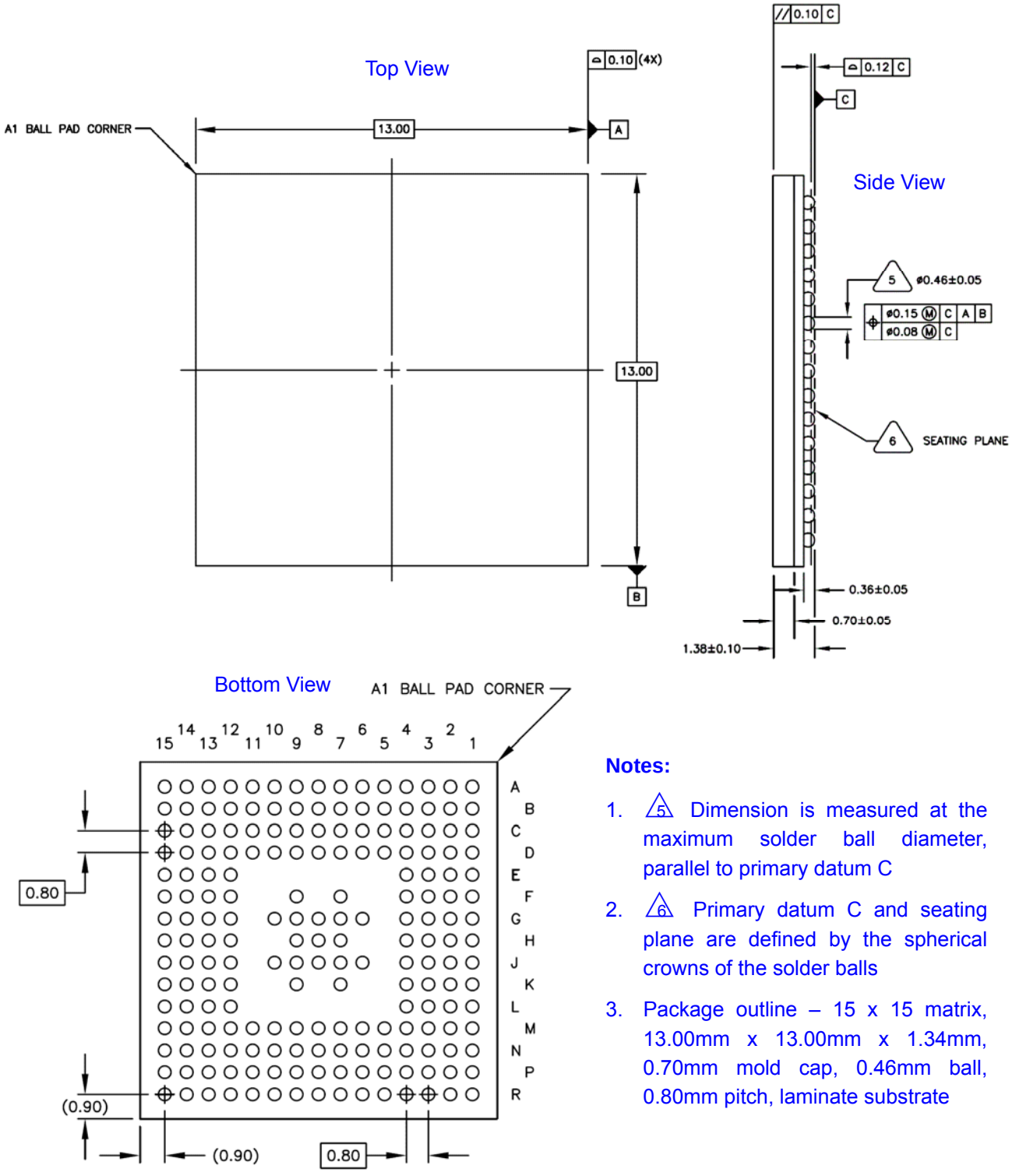
Jz4740 processor is packaged in a 193-pin ball grid array (LFBGA), has a square 13x13 and 4 rows ball assignment. The following figures and tables list all the functional pins.

All of the GPIO pins are multiplexed on the on-chip peripheral modules, and the reset state is general-purpose input with internal pull-up, except for WAIT_ pin, which is initial to WAIT_ function.

2.2 Solder Process

Jz4740 package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.

2.3 Package

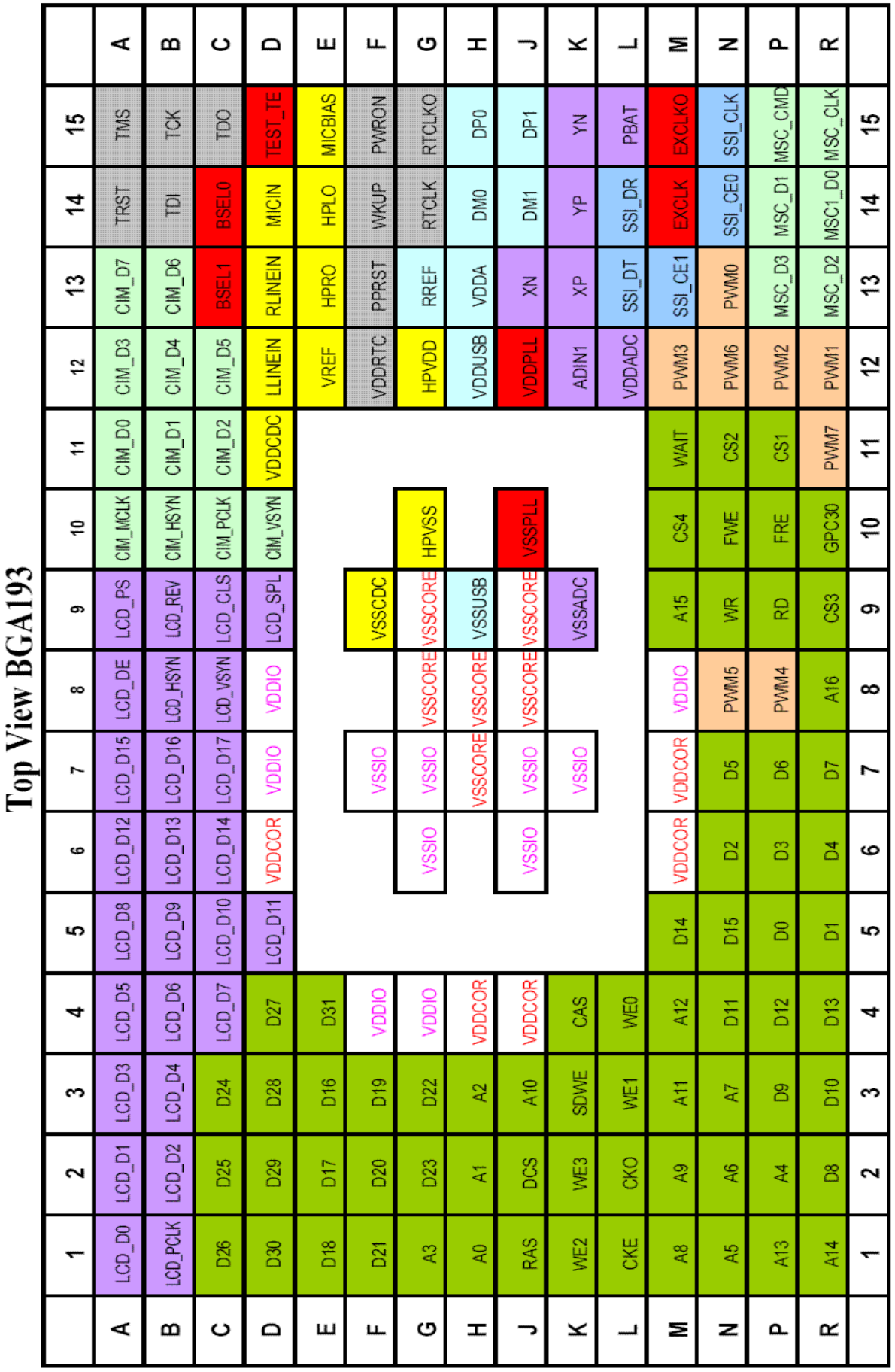


Notes:

1. (5) Dimension is measured at the maximum solder ball diameter, parallel to primary datum C
2. (6) Primary datum C and seating plane are defined by the spherical crowns of the solder balls
3. Package outline – 15 x 15 matrix, 13.00mm x 13.00mm x 1.34mm, 0.70mm mold cap, 0.46mm ball, 0.80mm pitch, laminate substrate

Figure 2-1 Jz4740 package

Top View BGA193



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	LCD_D0	LCD_D1	LCD_D3	LCD_D5	LCD_D8	LCD_D12	LCD_D15	LCD_DE	LCD_PS	CIM_MCLK	CIM_D0	CIM_D3	CIM_D7	TRST	TMS	A
B	LCD_PCLK	LCD_D2	LCD_D4	LCD_D6	LCD_D9	LCD_D13	LCD_D16	LCD_HSYN	LCD_REV	CIM_HSYN	CIM_D1	CIM_D4	CIM_D6	TDI	TCK	B
C	D26	D25	D24	LCD_D7	LCD_D10	LCD_D14	LCD_D17	LCD_VSYN	LCD_CLS	CIM_PCLK	CIM_D2	CIM_D5	BSEL1	BSEL0	TDO	C
D	D30	D29	D28	D27	LCD_D11	VDDCOR	VDDIO	VDDIO	LCD_SPL	CIM_VSYN	VDDCDC	LLINEIN	RLINEIN	MICIN	TEST_TE	D
E	D18	D17	D16	D31			VSSIO		VSSCDC			VREF	HPRO	HPLO	MICBIAS	E
F	D21	D20	D19	VDDIO				VSSCORE		HPVSS		VDDRTC	PPRST	WKUP	PWRON	F
G	A3	D23	D22	VDDIO		VSSIO	VSSIO	VSSCORE	VSSCORE			HPVDD	RREF	RTCLK	RTCLKO	G
H	A0	A1	A2	VDDCOR			VSSCORE	VSSCORE	VSSUSB			VDDUSB	VDDA	DM0	DP0	H
J	RAS	DCS	A10	VDDCOR		VSSIO	VSSIO	VSSCORE	VSSCORE	VSSPLL		VDDPLL	XN	DM1	DP1	J
K	WE2	WE3	SDWE	CAS			VSSIO		VSSADC			ADIN1	XP	YP	YN	K
L	CKE	CKO	WE1	WE0								VDDADC	SSI_DT	SSI_DR	PBAT	L
M	A8	A9	A11	A12	D14	VDDCOR	VDDCOR	VDDIO	A15	CS4	WAIT	PWM3	SSI_CE1	EXCLK	EXCLKO	M
N	A5	A6	A7	D11	D15	D2	D5	PWM5	WR	FWE	CS2	PWM6	PWM0	SSI_CE0	SSI_CLK	N
P	A13	A4	D9	D12	D0	D3	D6	PWM4	RD	FRE	CS1	PWM2	MSC_D3	MSC_D1	MSC_CMD	P
R	A14	D8	D10	D13	D1	D4	D7	A16	CS3	GPC30	PWM7	PWM1	MSC_D2	MSC1_D0	MSC_CLK	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

2.4 Pin Description

Table 2-1 EMC Pins (69 for Jz4740, 51 for Jz4720; all GPIO shared)

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
D0 PA0	IO IO	P5		8mA, pullup-pe	D0: Memory data bus bit 0 PA0: GPIO group A bit 0	VDDIO
D1 PA1	IO IO	R5		8mA, pullup-pe	D1: Memory data bus bit 1 PA1: GPIO group A bit 1	VDDIO
D2 PA2	IO IO	N6		8mA, pullup-pe	D2: Memory data bus bit 2 PA2: GPIO group A bit 2	VDDIO
D3 PA3	IO IO	P6		8mA, pullup-pe	D3: Memory data bus bit 3 PA3: GPIO group A bit 3	VDDIO
D4 PA4	IO IO	R6		8mA, pullup-pe	D4: Memory data bus bit 4 PA4: GPIO group A bit 4	VDDIO
D5 PA5	IO IO	N7		8mA, pullup-pe	D5: Memory data bus bit 5 PA5: GPIO group A bit 5	VDDIO
D6 PA6	IO IO	P7		8mA, pullup-pe	D6: Memory data bus bit 6 PA6: GPIO group A bit 6	VDDIO
D7 PA7	IO IO	R7		8mA, pullup-pe	D7: Memory data bus bit 7 PA7: GPIO group A bit 7	VDDIO
D8 PA8	IO IO	R2		8mA, pullup-pe	D8: Memory data bus bit 8 PA8: GPIO group A bit 8	VDDIO
D9 PA9	IO IO	P3		8mA, pullup-pe	D9: Memory data bus bit 9 PA9: GPIO group A bit 9	VDDIO
D10 PA10	IO IO	R3		8mA, pullup-pe	D10: Memory data bus bit 10 PA10: GPIO group A bit 10	VDDIO
D11 PA11	IO IO	N4		8mA, pullup-pe	D11: Memory data bus bit 11 PA11: GPIO group A bit 11	VDDIO
D12 PA12	IO IO	P4		8mA, pullup-pe	D12: Memory data bus bit 12 PA12: GPIO group A bit 12	VDDIO
D13 PA13	IO IO	R4		8mA, pullup-pe	D13: Memory data bus bit 13 PA13: GPIO group A bit 13	VDDIO
D14 PA14	IO IO	M5		8mA, pullup-pe	D14: Memory data bus bit 14 PA14: GPIO group A bit 14	VDDIO
D15 PA15	IO IO	N5		8mA, pullup-pe	D15: Memory data bus bit 15 PA15: GPIO group A bit 15	VDDIO
D16 PA16	IO IO	E3		8mA, pullup-pe	D16: Memory data bus bit 16 PA16: GPIO group A bit 16	VDDIO
D17 PA17	IO IO	E2		8mA, pullup-pe	D17: Memory data bus bit 17 PA17: GPIO group A bit 17	VDDIO
D18 PA18	IO IO	E1		8mA, pullup-pe	D18: Memory data bus bit 18 PA18: GPIO group A bit 18	VDDIO
D19 PA19	IO IO	F3		8mA, pullup-pe	D19: Memory data bus bit 19 PA19: GPIO group A bit 19	VDDIO
D20 PA20	IO IO	F2		8mA, pullup-pe	D0: Memory data bus bit 20 PA0: GPIO group A bit 20	VDDIO
D21 PA21	IO IO	F1		8mA, pullup-pe	D0: Memory data bus bit 21 PA0: GPIO group A bit 21	VDDIO
D22 PA22	IO IO	G3		8mA, pullup-pe	D0: Memory data bus bit 22 PA0: GPIO group A bit 22	VDDIO
D23 PA23	IO IO	G2		8mA, pullup-pe	D0: Memory data bus bit 23 PA0: GPIO group A bit 23	VDDIO
D24 PA24	IO IO	C3		8mA, pullup-pe	D0: Memory data bus bit 24 PA0: GPIO group A bit 24	VDDIO

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
D25 PA25	IO IO	C2		8mA, pullup-pe	D0: Memory data bus bit 25 PA0: GPIO group A bit 25	VDDIO
D26 PA26	IO IO	C1		8mA, pullup-pe	D0: Memory data bus bit 26 PA0: GPIO group A bit 26	VDDIO
D27 PA27	IO IO	D4		8mA, pullup-pe	D0: Memory data bus bit 27 PA0: GPIO group A bit 27	VDDIO
D28 PA28	IO IO	D3		8mA, pullup-pe	D0: Memory data bus bit 28 PA0: GPIO group A bit 28	VDDIO
D29 PA29	IO IO	D2		8mA, pullup-pe	D0: Memory data bus bit 29 PA0: GPIO group A bit 29	VDDIO
D30 PA30	IO IO	D1		8mA, pullup-pe	D0: Memory data bus bit 30 PA0: GPIO group A bit 30	VDDIO
D31 PA31	IO IO	E4		8mA, pullup-pe	D0: Memory data bus bit 31 PA0: GPIO group A bit 31	VDDIO
A0 PB0	O IO	H1		12mA, pullup-pe	A0: Static/SDRAM memory address bit 0 PB0: GPIO group B bit 0	VDDIO
A1 PB1	O IO	H2		12mA, pullup-pe	A1: Static/SDRAM memory address bit 1 PB1: GPIO group B bit 1	VDDIO
A2 PB2	O IO	H3		12mA, pullup-pe	A2: Static/SDRAM memory address bit 2 PB2: GPIO group B bit 2	VDDIO
A3 PB3	O IO	G1		12mA, pullup-pe	A3: Static/SDRAM memory address bit 3 PB3: GPIO group B bit 3	VDDIO
A4 PB4	O IO	P2		12mA, pullup-pe	A4: Static/SDRAM memory address bit 4 PB4: GPIO group B bit 4	VDDIO
A5 PB5	O IO	N1		12mA, pullup-pe	A5: Static/SDRAM memory address bit 5 PB5: GPIO group B bit 5	VDDIO
A6 PB6	O IO	N2		12mA, pullup-pe	A6: Static/SDRAM memory address bit 6 PB6: GPIO group B bit 6	VDDIO
A7 PB7	O IO	N3		12mA, pullup-pe	A7: Static/SDRAM memory address bit 7 PB7: GPIO group B bit 7	VDDIO
A8 PB8	O IO	M1		12mA, pullup-pe	A8: Static/SDRAM memory address bit 8 PB8: GPIO group B bit 8	VDDIO
A9 PB9	O IO	M2		12mA, pullup-pe	A9: Static/SDRAM memory address bit 9 PB9: GPIO group B bit 9	VDDIO
A10 PB10	O IO	J3		12mA, pullup-pe	A10: Static/SDRAM memory address bit 10 PB10: GPIO group B bit 10	VDDIO
A11 PB11	O IO	M3		12mA, pullup-pe	A11: Static/SDRAM memory address bit 11 PB11: GPIO group B bit 11	VDDIO
A12 PB12	O IO	M4		12mA, pullup-pe	A12: Static/SDRAM memory address bit 12 PB12: GPIO group B bit 12	VDDIO
A13 PB13	O IO	P1		12mA, pullup-pe	A13: Static/SDRAM memory address bit 13 PB13: GPIO group B bit 13	VDDIO
A14 PB14	O IO	R1		12mA, pullup-pe	A14: Static/SDRAM memory address bit 14 PB14: GPIO group B bit 14	VDDIO
A15 CL PB15	O O IO	M9		2mA, pullup-pe	A15: Static memory address bit 15 CL: NAND flash command latch PB15: GPIO group B bit 15	VDDIO
A16 AL PB16	O O IO	R8		2mA, pullup-pe	A16: Static memory address bit 16 AL: NAND flash address latch PB16: GPIO group B bit 16	VDDIO
DCS_ PB19	O IO	J2		8mA, pullup-pe	DCS_: SDRAM chip select PB19: GPIO group B bit 19	VDDIO
RAS_ PB20	O IO	J1		8mA, pullup-pe	RAS_: SDRAM row address strobe PB20: GPIO group B bit 20	VDDIO
CAS_ PB21	O IO	K4		8mA, pullup-pe	CAS_: SDRAM column address strobe PB21: GPIO group B bit 21	VDDIO

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
SDWE_ & BUFD_ PB22	O IO	K3		12mA, pullup-pe	SDWE_: SDRAM write enable BUFD_: Select CPU to SRAM chip direction in data bi-direction buffer PB22: GPIO group B bit 22	VDDIO
CKE PB23	O IO	L1		8mA, pullup-pe	CKE: SDRAM clock enable PB23: GPIO group B bit 23	VDDIO
CKO PB24	O IO	L2		12mA, pullup-pe	CKO: SDRAM clock PB24: GPIO group B bit 24	VDDIO
CS1_ PB25	O IO	P11		2mA, pullup-pe	CS1_: Static memory chip select 1 PB25: GPIO group B bit 25	VDDIO
CS2_ PB26	O IO	N11		2mA, pullup-pe	CS2_: Static memory chip select 2 PB26: GPIO group B bit 26	VDDIO
CS3_ PB27	O IO	R9		2mA, pullup-pe	CS3_: Static memory chip select 3 PB27: GPIO group B bit 27	VDDIO
CS4_ PB28	O IO	M10		2mA, pullup-pe	CS4_: Static memory chip select 4 PB28: GPIO group B bit 28	VDDIO
RD_ PB29	O IO	P9		2mA, pullup-pe	RD_: Static memory read strobe PB29: GPIO group B bit 29	VDDIO
WR_ PB30	O IO	N9		2mA, pullup-pe	WR_: Static memory write strobe PB30: GPIO group B bit 30	VDDIO
WE0_ PB31	O IO	L4		8mA, pullup-pe	WE0_: SDR/Static memory byte 0 write enable PB31: GPIO group B bit 31	VDDIO
WE1_ PC24	O IO	L3		8mA, pullup-pe	WE1_: SDR/Static memory byte 1 write enable PC24: GPIO group C bit 24	VDDIO
WE2_ PC25	O IO	K1		8mA, pullup-pe	WE2_: SDR/Static memory byte 2 write enable PC25: GPIO group C bit 25	VDDIO
WE3_ PC26	O IO	K2		8mA, pullup-pe	WE3_: SDR/Static memory byte 3 write enable PC26: GPIO group C bit 26	VDDIO
WAIT_ PC27	I IO	M11		2mA, Schmitt, pullup-pe	WAIT_: Slow static memory/device wait signal PC27: GPIO group C bit 27	VDDIO
FRE_ PC28	O IO	P10		2mA, pullup-pe	FRE_: NAND flash read enable PC28: GPIO group C bit 28	VDDIO
FWE_ PC29	O IO	N10		2mA, pullup-pe	FWE_: NAND flash write enable PC29: GPIO group C bit 29	VDDIO
PC30 (FRB)	IO	R10		2mA, pullup-pe	PC30: GPIO group C bit 30. If NAND flash is used, it should connect to NAND FRB (NAND flash ready/busy)	VDDIO

Table 2-2 LCDC Pins (26 for Jz4740, 20 for Jz4720; all GPIO shared)

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
LCD_CLS A21 PB17	O O IO	C9		4mA, pullup-pe	LCD_CLS: LCD CLS output A21: Static memory address bit 21 PB17: GPIO group B bit 17	VDDIO
LCD_SPL A22 PB18	O O IO	D9		4mA, pullup-pe	LCD_SPL: LCD SPL output A22: Static memory address bit 22 PB18: GPIO group B bit 18	VDDIO
LCD_D0 PC0	O IO	A1		4mA, pullup-pe	LCD_D0: LCD data bit 0 PC0: GPIO group C bit 0	VDDIO
LCD_D1 PC1	O IO	A2		4mA, pullup-pe	LCD_D1: LCD data bit 1 PC1: GPIO group C bit 1	VDDIO

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
LCD_D2 PC2	O IO	B2		4mA, pullup-pe	LCD_D2: LCD data bit 2 PC2: GPIO group C bit 2	VDDIO
LCD_D3 PC3	O IO	A3		4mA, pullup-pe	LCD_D3: LCD data bit 3 PC3: GPIO group C bit 3	VDDIO
LCD_D4 PC4	O IO	B3		4mA, pullup-pe	LCD_D4: LCD data bit 4 PC4: GPIO group C bit 4	VDDIO
LCD_D5 PC5	O IO	A4		4mA, pullup-pe	LCD_D5: LCD data bit 5 PC5: GPIO group C bit 5	VDDIO
LCD_D6 PC6	O IO	B4		4mA, pullup-pe	LCD_D6: LCD data bit 6 PC6: GPIO group C bit 6	VDDIO
LCD_D7 PC7	O IO	C4		4mA, pullup-pe	LCD_D7: LCD data bit 7 PC7: GPIO group C bit 7	VDDIO
LCD_D8 PC8	O IO	A5		4mA, pullup-pe	LCD_D8: LCD data bit 8 PC8: GPIO group C bit 8	VDDIO
LCD_D9 PC9	O IO	B5		4mA, pullup-pe	LCD_D9: LCD data bit 9 PC9: GPIO group C bit 9	VDDIO
LCD_D10 PC10	O IO	C5		4mA, pullup-pe	LCD_D10: LCD data bit 10 PC10: GPIO group C bit 10	VDDIO
LCD_D11 PC11	O IO	D5		4mA, pullup-pe	LCD_D11: LCD data bit 11 PC11: GPIO group C bit 11	VDDIO
LCD_D12 PC12	O IO	A6		4mA, pullup-pe	LCD_D12: LCD data bit 12 PC12: GPIO group C bit 12	VDDIO
LCD_D13 PC13	O IO	B6		4mA, pullup-pe	LCD_D13: LCD data bit 13 PC13: GPIO group C bit 13	VDDIO
LCD_D14 PC14	O IO	C6		4mA, pullup-pe	LCD_D14: LCD data bit 14 PC14: GPIO group C bit 14	VDDIO
LCD_D15 PC15	O IO	A7		4mA, pullup-pe	LCD_D15: LCD data bit 15 PC15: GPIO group C bit 15	VDDIO
LCD_D16 PC16	O IO	B7		4mA, pullup-pe	LCD_D16: LCD data bit 16 PC20: GPIO group C bit 16	VDDIO
LCD_D17 PC17	O IO	D7		4mA, pullup-pe	LCD_D17: LCD data bit 17 PC17: GPIO group C bit 17	VDDIO
LCD_PCLK PC18	IO IO	B1		4mA, pullup-pe	LCD_PCLK: LCD pixel clock PC18: GPIO group C bit 18	VDDIO
LCD_HSYNC PC19	IO IO	B8		4mA, pullup-pe	LCD_HSYNC: LCD line clock/horizonal sync PC19: GPIO group C bit 19	VDDIO
LCD_VSYNC PC20	IO IO	C8		4mA, pullup-pe	LCD_VSYNC: LCD frame clock/vertical sync PC20: GPIO group C bit 20	VDDIO
LCD_DE PC21	O IO	A8		4mA, pullup-pe	LCD_DE: STN AC bias drive/non-STN data enable PC21: GPIO group C bit 21	VDDIO
LCD_PS A19 PC22	O O IO	A9		4mA, pullup-pe	LCD_PS: LCD PS output for special TFT A19: Static memory address bit 19 PC22: GPIO group C bit 22	VDDIO

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
LCD_REV A20 PC23	O O IO	B9		4mA, pullup-pe	LCD_REV: LCD REV output for special TFT A20: Static memory address bit 20 PC23: GPIO group C bit 23	VDDIO

Table 2-3 USB device 2.0 and host 1.1 Pins (8 for Jz4740, 8 for Jz4720)

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
DP0	AIO	H15			DP0: USB 2.0 device data plus	VDD_{USB}
DM0	AIO	H14			DM0: USB 2.0 device data minus	VDD_{USB}
RREF	AIO	G13			RREF: External Reference for USB 2.0 device. Connect a 10kΩ external reference resistor, with 1% tolerance to analog ground VSSUSB	VDD_{USB}
VDDA	AIO	H13			VDDA: For USB 2.0 device. Connect a 0.1μF capacitor to analog ground VSSUSB	VDD_{USB}
VDDUSB	P	H12			VDDUSB: USB analog power, 3.3V	-
VSSUSB	P	H9			VSSUSB: USB analog ground	-
DP1	AIO	J15			DP1: USB 1.1 host data plus	VDD_{USB}
DM1	AIO	J14			DM1: USB 1.1 host data minus	VDD_{USB}

Table 2-4 SSI/AIC Pins (5 for Jz4740, 5 for Jz4720; all GPIO shared)

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
SSI_CLK SCLK_RSTN PD18	O O IO	N15		2mA, pullup-pe	SSI_CLK: SSI clock output SCLK_RSTN: I2S system clock output or AC97 reset output PD18: GPIO group D bit 18	VDDIO
SSI_CE0_ BCLK PD19	O IO IO	N14		2mA, pullup-pe	SSI_CE0_: SSI chip enable 0 BCLK: AC97/I2S bit clock PD19: GPIO group D bit 19	VDDIO
SSI_DT SDATO PD20	O O IO	L13		2mA, pullup-pe	SSI_DT: SSI data output SDATO: AC97/I2S serial data output PD20: GPIO group D bit 20	VDDIO
SSI_DR SDATI PD21	I I IO	L14		2mA, pullup-pe	SSI_DR: SSI data input SDATI: AC97/I2S serial data input PD21: GPIO group D bit 21	VDDIO
SSI_CE1__GPC SYNC PD22	O IO IO	M13		2mA, pullup-pe	SSI_CE1__GPC: SSI chip enable 1 or general-purpose control signal SYNC: AC97 frame SYNC or I2S Left/Right PD22: GPIO group D bit 22	VDDIO

Table 2-5 TCU/I2C/UART Pins (8 for Jz4740, 6 for Jz4720; all GPIO shared)

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
PWM0 I2C_SDA PD23	O IO IO	N13		4mA, pullup-pe	PWM0: PWM 0 output I2C_SDA: I2C serial data PD23: GPIO group D bit 23	VDDIO
PWM1 I2C_SCK	O IO	R12		4mA, pullup-pe	PWM1: PWM 1 output I2C_SCK: I2C serial clock	VDDIO

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
PD24	IO				PD24: GPIO group D bit 24	
PWM2 UART_TxD PD25	O O IO	P12		2mA, pullup-pe	PWM2: PWM 2 output UART_TxD: UART transmitting data PD25: GPIO group D bit 25	VDDIO
PWM3 UART_RxD PD26	O I IO	M12		2mA, pullup-pe	PWM3: PWM 3 output UART_RxD: UART Receiving data PD26: GPIO group D bit 26	VDDIO
PWM4 A17 PD27	O O IO	P8		2mA, pullup-pe	PWM4: PWM 4 output A17: Static memory address bit 17 PD27: GPIO group D bit 27	VDDIO
PWM5 A18 PD28	O O IO	N8		2mA, pullup-pe	PWM5: PWM 5 output A18: Static memory address bit 18 PD28: GPIO group D bit 28	VDDIO
PWM6 UART_CTS_ PD30	O I IO	N12		2mA, pullup-pe	PWM6: PWM 6 output UART_CTS_: UART CTS_ input PD30: GPIO group D bit 30	VDDIO
PWM7 UART_RTS_ PD31	O O IO	R11		2mA, pullup-pe	PWM7: PWM 7 output UART_RTS_: UART RTS_ output PD31: GPIO group D bit 31	VDDIO

Table 2-6 SAR ADC Pins (8 for Jz4740, 7 for Jz4720)

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
XP	AI	K13			XP: Touch screen X+ input	VDD_{ADC}
XN	AI	J13			XN: Touch screen X- input	VDD_{ADC}
YP	AI	K14			YP: Touch screen Y+ input	VDD_{ADC}
YN	AI	K15			YN: Touch screen Y- input	VDD_{ADC}
PBAT/ADIN0	AI	L15			ADIN0: Battery voltage input or ADC general purpose input 0	VDD_{ADC}
ADIN1	AI	K12			ADIN1: ADC general purpose input 1	VDD_{ADC}
VDDADC	P	L12			VDDADC: ADC analog power, 3.3 V	-
VSSADC	P	K9			VDDADC: ADC analog ground	-

Table 2-7 Audio CODEC Pins (11 for Jz4740, 9 for Jz4720)

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
LHPO	AO	E14			LHPO: Left headphone out	VDD_{CDC}
RHPO	AO	E13			RHPO: Right headphone out	VDD_{CDC}
MICIN	AI	D14			MICIN: Microphone input	VDD_{CDC}
MICBIAS	AO	E15			MICBIAS: Microphone bias	VDD_{CDC}
LLINEIN	AI	D12			LLINEIN: Left line input	VDD_{CDC}
RLINEIN	AI	D13			RLINEIN: Right line input	VDD_{CDC}
VREF	AO	E12			VREF: Voltage Reference Output. An electrolytic capacitor more than 10μF in parallel with a 0.1μF ceramic capacitor attached from this pin to VSSCDC eliminates the effects of high frequency noise	VDD_{CDC}
VDDHP	P	G12			VDDHP: Headphone amplifier power, 3.3V	-

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
VSSHP	P	G10			VSSHP: Headphone amplifier ground	-
VDDCDC	P	D11			VDDCDC: CODEC analog power, 3.3V	-
VSSCDC	P	F9			VSSCDC: CODEC analog ground	-

Table 2-8 CIM Pins (12 for Jz4740, 0 for Jz4720; all GPIO shared)

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
CIM_D0 PD00	I IO	A11		4mA, pullup-pe	CIM_D0: CIM data input bit 0 PD00: GPIO group D bit 0	VDDIO
CIM_D1 PD01	I IO	B11		4mA, pullup-pe	CIM_D1: CIM data input bit 1 PD01: GPIO group D bit 1	VDDIO
CIM_D2 PD02	I IO	C11		4mA, pullup-pe	CIM_D2: CIM data input bit 2 PD02: GPIO group D bit 2	VDDIO
CIM_D3 PD03	I IO	A12		4mA, pullup-pe	CIM_D3: CIM data input bit 3 PD03: GPIO group D bit 3	VDDIO
CIM_D4 PD04	I IO	B12		4mA, pullup-pe	CIM_D4: CIM data input bit 4 PD04: GPIO group D bit 4	VDDIO
CIM_D5 PD05	I IO	C12		4mA, pullup-pe	CIM_D5: CIM data input bit 5 PD05: GPIO group D bit 5	VDDIO
CIM_D6 PD06	I IO	B13		4mA, pullup-pe	CIM_D6: CIM data input bit 6 PD06: GPIO group D bit 6	VDDIO
CIM_D7 PD07	I IO	A13		4mA, pullup-pe	CIM_D7: CIM data input bit 7 PD07: GPIO group D bit 7	VDDIO
CIM_MCLK PD14	O IO	A10		4mA, pullup-pe	CIM_MCLK: CIM master clock output PD14: GPIO group D bit 14	VDDIO
CIM_PCLK PD15	I IO	C10		4mA, pullup-pe	CIM_PCLK: CIM pixel clock input PD15: GPIO group D bit 15	VDDIO
CIM_VSYNC PD16	I IO	D10		4mA, pullup-pe	CIM_VSYNC: CIM VSYNC input PD16: GPIO group D bit 16	VDDIO
CIM_HSYNC PD17	I IO	B10		4mA, pullup-pe	CIM_HSYNC: CIM HSYNC input PD17: GPIO group D bit 17	VDDIO

Table 2-9 MSC (MMC/SD) Pins (6 for Jz4740, 6 for Jz4720; all GPIO shared)

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
MSC_D0 PD10	IO IO	R14		4mA, pullup-pe	MSC_D0: MSC data bit 0 PD10: GPIO group D bit 10	VDDIO
MSC_D1 PD11	IO IO	P14		4mA, pullup-pe	MSC_D0: MSC data bit 1 PD11: GPIO group D bit 11	VDDIO
MSC_D2 PD12	IO IO	R13		4mA, pullup-pe	MSC_D0: MSC data bit 2 PD12: GPIO group D bit 12	VDDIO
MSC_D3 PD13	IO IO	P13		4mA, pullup-pe	MSC_D0: MSC data bit 3 PD13: GPIO group D bit 13	VDDIO

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
MSC_CMD PD08	IO IO	P15		4mA, pullup-pe	MSC_CMD: MSC command PD08: GPIO group D bit 8	VDDIO
MSC_CLK PD09	O IO	R15		4mA, pullup-pe	MSC_CLK: MSC clock output PD09: GPIO group D bit 9	VDDIO

Table 2-10 CPM Pins (4 for Jz4740, 4 for Jz4720)

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
EXCLK	AI	M14		10~20 MHz Oscillator, OSC on/off	EXCLK: OSC input or 12MHz clock input	VDDIO
EXCLKO	AO	M15			EXCLKO: OSC output	VDDIO
VDDPLL	P	J12			VDDPLL: PLL analog power, 1.8V	-
VSSPLL	P	J10			VSSPLL: PLL analog ground	-

Table 2-11 RTC Pins (6 for Jz4740, 7 for Jz4720; all GPIO shared)

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
RTCLK	AI	G14		32768Hz Oscillator	RTCLK: OSC input	VDD_{RTC}
RTCLKO	AO	G15			RTCLKO: OSC output or 32768Hz clock input	VDD_{RTC}
PWRON_	AO	F15		~2mA, Open-Draw	PWRON_: Power on/off control of main power	VDD_{RTC}
WKUP_ PD29	AI AI	F14		Schmitt	WKUP_: Wake signal after main power down PD29: GPIO group D bit 29, input/interrupt only	VDD_{RTC}
PPRST_	AI	F13		Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDD_{RTC}
VDDRTC	P	F12			VDDRTC: 3.3V power for RTC and hibernating mode controlling that never power down	-
VSSRTC	P				VSSRTC: RTC ground	-

Table 2-12 JTAG/UART Pins (5 for Jz4740, 5 for Jz4720)

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
TRST_	I	A14		Schmitt, pull-down	TRST_: JTAG reset	VDDIO
TCK	I	B15		Schmitt, pull-down	TCK: JTAG clock	VDDIO
TMS	I	A15		Schmitt, pull-up	TMS: JTAG mode select	VDDIO
TDI UART_RxD	I I	B14		Schmitt, pull-up	TDI: JTAG serial data input UART_RxD: UART Receiving data, PC31 is used to select between JTAG and UART	VDDIO
TDO UART_TxD	O O	C15		4mA	TDO: JTAG serial data output UART_TxD: UART transmitting data, PC31 is used to select between JTAG and UART	VDDIO

Table 2-13 System Pins (3 for Jz4740, 3 for Jz4720)

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
BOOT_SEL0	I	C14		Schmitt	BOOT_SEL0: Boot select bit 0	VDDIO
BOOT_SEL1	I	C13		Schmitt	BOOT_SEL1: Boot select bit 1	VDDIO
TEST_TE	I	D15		Schmitt, pull-down	TEST_TE: Manufacture test enable, program readable	VDDIO
CHIP_MD	I			Schmitt	CHIP_MD: 0 – BGA193 package, 1 – COB package	VDDIO

Table 2-14 IO/Core power supplies (22 for Jz4740, ? for Jz4720)

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
VDDIO	P	D7 D8 F4 G4 M8			VDDIO: 5 IO digital power, 3.3V	-
VSSIO	P	F7 G6 G7 J6 J7 K7			VSSIO: 6 IO digital ground	-
VDDCORE	P	D6 H4 J4 M6 M7			VDDCORE: 5 CORE digital power, 1.8V	-
VSSCORE	P	G8 G9 H7 H8 J8 J9			VSSCORE: 6 CORE digital ground	-

Notes:

1. The meaning of phases in IO cell characteristics are
   a) 2/4/8/12mA out: The IO cell's output driving strength is about 2/4/8/12mA
   b) Pull-up: The IO cell contains a pull-up resistor
   c) Pull-down: The IO cell contains a pull-down resistor
   d) Pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register.
   e) Schmitt: The IO cell is Schmitt trig input

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDIO power supplies voltage	-0.5	4.6	V
VDDUSB power supplies voltage	-0.3	3.9	V
VDDCDC power supplies voltage	-0.3	4.0	V
VDDHP power supplies voltage	-0.3	4.0	V
VDDADC power supplies voltage	-0.3	4.0	V
VDDRTC power supplies voltage	-0.3	4.0	V
VDDcore power supplies voltage	-0.2	2.2	V
VDDPLL power supplies voltage	-0.5	2.5	V
Input voltage to VDDIO supplied non-supply pins	-0.5	4.6	V
Input voltage to VDDUSB supplied non-supply pins	-0.5	5.0	V
Input voltage to VDDADC supplied non-supply pins	-0.5	4.0	V
Input voltage to VDDCDC supplied non-supply pins	-0.5	4.0	V
Input voltage to VDDRTC supplied non-supply pins	-0.5	4.0	V
Output voltage from VDDIO supplied non-supply pins	-0.5	4.6	V
Output voltage from VDDUSB supplied non-supply pins	-0.5	5.0	V
Output voltage from VDDADC supplied non-supply pins	-0.5	4.0	V
Output voltage from VDDCDC supplied non-supply pins	-0.5	4.0	V
Output voltage from VDDRTC supplied non-supply pins	-0.5	4.0	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
V_{IO}	VDDIO voltage	2.97	3.3	3.63	V
V_{USB}	VDDUSB voltage	3.0	3.3	3.6	V
V_{CDC}	VDDCDC voltage	3.0	3.3	3.6	V
V_{HP}	VDDHP voltage	3.0	3.3	3.6	V
V_{ADC}	VDDADC voltage	3.0	3.3	3.6	V
V_{RTC}	VDDRTC voltage	3.0	3.3	3.6	V
V_{CORE}	VDDcore voltage	1.62	1.8	1.98	V
V_{PLL}	VDDPLL analog voltage	1.62	1.8	1.98	V

Table 3-3 Recommended operating conditions for VDDIO supplied digital pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH}	Input high voltage	2.0		3.6	V
V_{IL}	Input low voltage	-0.3		0.8	V

Table 3-4 Recommended operating conditions for USB 2.0 Device DP/DM pins

Symbol	Description	Min	Typical	Max	Unit
V_{ILH}	Input voltage range for full speed applications	0		V_{USB}	V
V_{ILH}	Input voltage range for high speed applications	120		400	mV

Table 3-5 Recommended operating conditions for USB 1.1 Host pins

Symbol	Description	Min	Typical	Max	Unit
V_{ILH}	Input voltage range	0		V_{USB}	V

Table 3-6 Recommended operating conditions for ADC pins

Symbol	Description	Min	Typical	Max	Unit
$V_{ILH-PBAT1}$	PBAT input voltage range when measuring low voltage battery	0		2.5	V
$V_{ILH-PBAT2}$	PBAT input voltage range when measuring high voltage battery	0		6	V
$V_{ILH-ADIN1}$	ADIN1 input low voltage range	0		V_{ADC}	V
$V_{ILH-TSC}$	XN/XP/YN/YP input voltage range	0		V_{ADC}	

Table 3-7 Recommended operating conditions for VDDRTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH}	Input high voltage	2.0		3.6	V
V_{IL}	Input low voltage	-0.3		0.8	V

Table 3-8 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	0		85	°C

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-9 DC characteristics for VDDIO pins

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	1.46	1.59	1.75	V
V_{T+}	Schmitt trig low to high threshold point	1.44	1.50	1.56	V
V_{T-}	Schmitt trig high to low threshold point	0.88	0.94	0.99	V
I_L	Input Leakage Current			±10	μA
I_{OZ}	Tri-State output leakage current			±10	μA
R_{PU}	Pull-up Resistor	50	65	100	kΩ
R_{PD}	Pull-down Resistor	40	56	107	kΩ
V_{OL}	Output low voltage @I_{OL}=2, 4, 8, 12mA			0.4	V
V_{OH}	Output high voltage @I_{OH}=2, 4, 8, 12mA	2.4			V
I_{OL}	Low level output current @V_{OL}=0.4V for cells of				mA
	2mA	2.2	3.7	4.6	
	4mA	4.4	7.4	9.2	
	8mA	8.9	14.7	18.4	
	12mA	13.3	22.1	27.5	
I_{OH}	High level output current @V_{OH}=2.4V for cells of				mA
	2mA	2.5	5.1	7.9	
	4mA	5.0	10.2	15.9	
	8mA	10.0	20.4	31.7	
	12mA	15.0	30.6	47.6	

Table 3-10 DC characteristics for USB 2.0 Device DP/DM pins

Symbol	Description	Min	Typical	Max	Unit
V_{OL}	Output low voltage	0		V_{USB}	V
V_{OH}	Output high voltage	0		400	mV

Table 3-11 DC characteristics for USB 1.1 Host pins

Symbol	Description	Min	Typical	Max	Unit
V_{OLH}	Output voltage range	0		V_{USB}	V
V_{DI}	Differential input sensitivity	0.2			V
V_{CM}	Differential common mode range	0.8		2.5	V
V_{SE}	Single ended receiver threshold	0.8		2.0	V

I_{OZ}	Tri-State leakage current			±10	μA
Z_{DRV}	Driver output resistance, including damping resistor	24		44	Ω
V_{OL}	Static output low voltage			0.3	V
V_{OH}	Static output high voltage	2.8			V

Table 3-12 DC characteristics for ADC pins

Symbol	Description	Min	Typical	Max	Unit
V_{OH}	XN/XP/YN/YP output high voltage	0.9 * V_{ADC}		V_{ADC}	V
V_{OL}	XN/XP/YN/YP output low voltage	0		0.1 * V_{ADC}	V

Table 3-13 DC characteristics for VDDRTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{OH}	Output high voltage	2.0		3.6	V
V_{OL}	Output low voltage	-0.3		0.8	V

3.4 Characteristics of CODEC

Table 3-14 CODEC characteristics

Parameter	Conditions	Min	Typical	Max	Unit
S/N (A-weighted)-DAC	Note 1		90		dB
S/N (A-weighted)-ADC	Note 1		85		dB
Dynamic range (A-weighted) @-60dB	Fin@1kHz		90		dB
THD+N (A-weighted) @-6dB-DAC	Note 2				dB
THD+N (A-weighted) @-6dB-ADC	Note 3	70			dB
Inter-channel isolation	Fin@1kHz		60		dB
Inter-channel gain mismatch			0.1	0.2	dB
Closed loop gain			0		dB
Load resistance for HPOUTL & HPOUTR		32			Ω
Power supply rejection @ 200Hz			60		dB
Passband		0		0.42	fs
Passband ripple				±0.1	dB
Stopband		0.58			fs
Stopband attenuation		76			dB
LLINEIN/MIC resistance			40		KΩ
LLINEIN/MIC input range			1.6		Vp-p
MICBIAS voltage			2/3Avd		V
MICBIAS drive current			2		mA
HPOUT output peak value			1.8		Vp-p
Analog supply voltage		3.0	3.3	3.6	V
Digital supply voltage		1.62	1.8	1.98	V
Standby current			3		uA
Power Consumption (no tone)	DAC enable		28		mW
	ADC enable		34		mW
	ADC/DAC enable		62		mW

Note:

1. The ratio of the rms output level with 1KHz full-scale input to the rms output noise level. Measured “A-weighted” over a 20Hz to 0.44Fs bandwidth.
2. The ratio of the rms value of the signal to the rms sum of all the spectral components less than 0.44Fs bandwidth, including distortion components, tested at -6dB input. The headphone output THD+N>= 70dB under 32Ohm/16Ohm loading.

3.5 Power Consumption Specifications

Power consumption depends on the operating voltage, peripherals enabled, external switching activity, and external loading.

The maximum power consumption specification is determined by all units running at their maximum: processor speed, voltage, and loading conditions. This method generates a conservative power consumption value; however, power supply and thermal management design requires the highest possible power consumption for robust design. The Jz4740 processor's maximum power consumption is calculated using the following conditions:

- All peripheral units operating at maximum frequency and size configuration
- All I/O loads maximum (50pF for Memory interface, 100pF for peripherals)
- Core operating at worst case power scenario (hit rates adjusted for worst power)
- All voltages at maximum of range

Do not exceed the maximum package power rating or T_{case} temperature.

But for most of applications, a more optimal system design requires more typical power-consumption figures. These figures are important when considering battery size and optimizing regulator efficiency. Typical systems operate with fewer modules active and at nominal voltage and load. The typical power consumption for the Jz4730 processor is calculated using these conditions:

- All voltage at nominal value
- Nominal case temperature

Table 3-15 Power Consumption Specifications

Symbol	Description	Typical	Max	Unit
400MHz normal mode; Maximum: V(core)= 2.2V, V(IO1)=V, V(IO2)=3.6V, Temp=100°C Typical: V(core)=1.8V, V(IO1)=1.8V, V(IO2)=3.3V, Temp=Room				
				mW
				mW
				mW
				mW
				mW
				mW

				mW
				mW
				mW

3.6 AC Specifications

A pin's AC Characteristics include input and output capacitance. These determine loading for external drivers or other load analysis. The AC Characteristics also include a de-rating factor, which indicates how much faster or slower the AC timings get with different loads. The AC Operating Conditions for all input, output, and I/O pins are shown in Table 3-16. All AC specification values are valid for entire temperature range of the device.

Table 3-16 Standard Input, Output, and I/O Pin AC Operating Conditions

Symbol	Description	Min	Typical	Max	Units
C_{IN}	Input Capacitance, all input and IO pins	3	5	10	pF
C_{OUT_G12}	Output Capacitance, 12mA output and IO pins				pF
C_{OUT_G8}	Output Capacitance, 8mA SDRAM output and IO pins				pF

NOTE: AC Specifications guaranteed for loads in this range. All testing is done at 50pF

3.7 Oscillator Electrical Specifications

The processor contains two oscillators, each for a specific crystal: a 32.768KHz oscillator and a EXCLK oscillator. When choosing a crystal, match the crystal parameters as closely as possible.

3.7.1 32.768KHz Oscillator Specifications

3.7.2 EXCLK Oscillator Specifications

3.8 Power On, Reset and BOOT

3.8.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the Jz4740 processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1 shows this sequence and is detailed in Table 3-17.

On the processor, it is important that the power supplies be powered up in a certain order to avoid high current situations. The required order is:

1. VDDRTC
2. All other 3.3V VDDs (VDD33): VDDIO, VDDCDC, VDDHP, VDDADC, VDDUSB
3. All 1.8V VDDs (VDD18): VDDCORE, VDDPLL

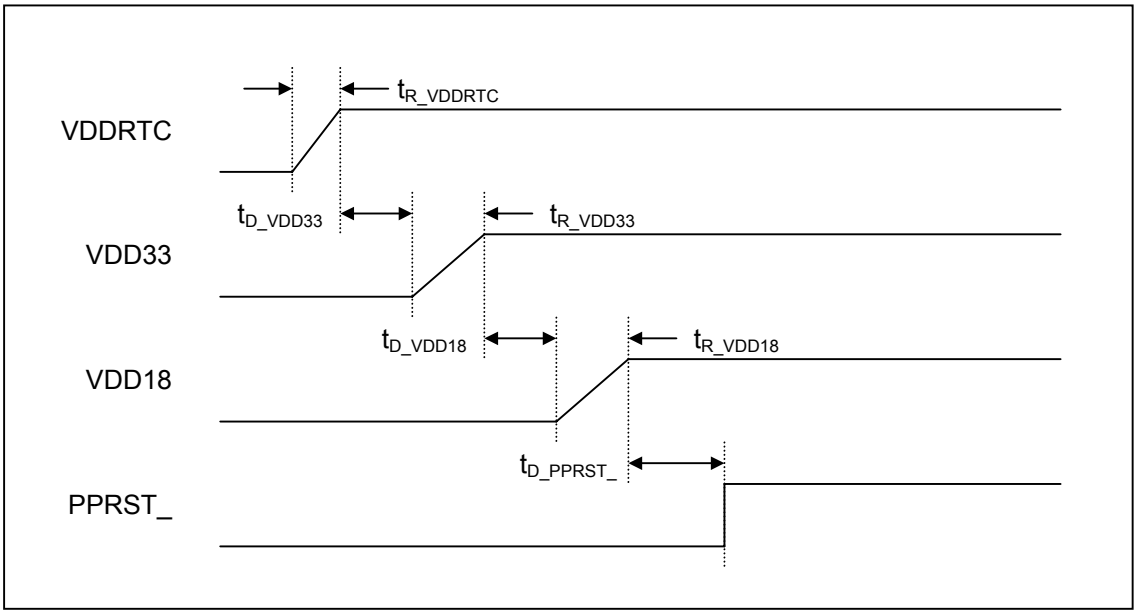


Figure 3-1 Power-On Timing Diagram

Table 3-17 Power-On Timing Parameters

Symbol	Parameter	Min	Typical	Max	Unit
t_{R_VDDRTC}	VDDRTC rise/stabilization time	0.01	–	100	ms
t_{D_VDD33}	Delay between VDDRTC stable and VDD33 applies	$-t_{R\_VDDRTC}$	–	10	ms[1]
t_{R_VDD33}	VDD33 rise/stabilization time	0.01	–	100	ms
t_{D_VDD18}	Delay between VDD33 stable and VDD18 applies	-0.5 * t_{R_VDD33}	–	10	ms[2]
t_{R_VDD18}	VDD18 rise/stabilization time	0.01	–	100	ms
$t_{D\_PPRST\_}$	Delay between VDD18 stable and PPRST_ deasserted	10	–	–	ms

Note:

1. VDD33 can be applied before VDDRTC stable. But the time of VDD33 arriving 50%, 90% voltage level should later than that of VDDRTC arriving the same level.
2. VDD18 can be applied before VDD33 stable. But the time of VDD18 arriving 50%, 90% voltage level should later than that of VDD33 arriving the same level.

3.8.2 Reset procedure

There 3 reset sources: (1) PPRST_ pin reset; (2) WDT timeout reset; and (3) hibernating reset when exiting hibernating mode. After reset, program start from boot.

(1) PPRST_ pin reset

This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is a few RTCLK cycles after rising edge of PPRST_.

(2) WDT reset

This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.

(3) Hibernating reset

This reset happens in case of wakeup the main power from power down. The reset keeps for about 0ms ~ 125ms programable, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins, except WAIT_ pin, are put to GPIO input function with the internal pull-up set to on. The WAIT_ pin is set to wait function with the internal pull-up set to on. The PWRON_ is output 0. The 32768Hz/12MHz oscillators are on. The JATG/UART is put to JTAG function and the TDO is output high-Z (suppose TRST_ is 0). The analog devices, the USB 2.0 PHY, USB 1.1 PHY, the CODEC DAC/ADC and the SAR-ADCs, are put in suspend mode.

3.8.3 BOOT

Jz4740/Jz4720 support 3 different boot sources depending on BOOT_SEL0 and BOOT_SEL1 pin values. Table 3-18 lists them.

Table 3-18 Boot from 3 boot sources

BOOT_SEL1	BOOT_SEL0	Boot Source
0	0	Boot from external ROM at CS4
0	1	Boot from USB device
1	0	Boot from 512 page NAND flash at CS1
1	1	Boot from 2k page NAND flash at CS1

3.9 Memory Bus AC Specifications

This section provides the timing information for these types of memory:

- SRAM / ROM / Flash
- SDRAM

3.10 Peripheral Module AC Specifications

3.10.1 LCD Module Timing

3.10.2 CIM Module Timing

3.10.3 SPI Module Timing

3.10.4 External DMA Request and Grant