1 Clock Reset and Power Controller

1.1 Overview

The Clock & Power management block consists of three parts: Clock control, PLL control, and Power control, Reset control.

The Clock control logic in JZ4740 can generate the required clock signals including CCLK for CPU, HCLK for the AHB bus peripherals, and PCLK for the APB bus peripherals. The JZ4740 has one Phase Locked Loops (PLL): for CCLK, HCLK, and PCLK, USB block (12Mhz) ,LDCLK, LPCLK. The clock control logic can make slow clocks without PLL and connect/disconnect the clock to each peripheral block by software, which will reduce the power consumption.

For the power control logic, the JZ4740 has various power management schemes to keep optimal power consumption for a given task. The power management block in the JZ4740 can activate four modes: NORMAL mode , DOZE mode, IDLE mode, SLEEP mode, and HIBERNATE mode.

For reset control logic, the reset module controls or distributes all of the system reset signals used by the JZ47xx

1.2 Clock Generation Module

The JZ4740 processor contains one PLL driven by the 12-MHz oscillator and a clock generator from which the following are derived:

- CPU clock
- System bus clock
- Peripheral bus clock
- SDRAM bus clock
- Programmable clocks needed by certain peripherals

The output clocks are:

Signal	Description
CCLK	Fast clock used by JZ47xx for internal operations such as executing instructions from the cache. It can be gated during doze and idle mode when all the criteria to enter a low power are met.
HCLK	System clock—This signal appears as the HCLK input to the CPU and the HCLK to the system. This is a continuous clock (when the system is not in sleep mode) It can be gated during Sleep mode when all the criteria to enter a low power are met
PCLK	peripheral clock – APB BUS device clock
MCLK	Flash and Sram external memory clock
CKO	SDRAM Clock
LDCLK	Divided device clock output for the LCDC module
LPCLK	Divided pixel clock output for the LCDC module
I2SCLK	Divided clock output for AIC module
MSCCLK	Divided clock output about 19M to MSC module (MMC card)
12M	Divided clock output for UART I2C SSI TCU USB-PHY

Feature:

- On-chip12MHz oscillator circuit
- One On-chip phase-locked loops (PLL) with programmable multiplier
- CCLK, PCLK, HCLK, MCLK , CKO and LDCLK LPCLK I2SCLK MSCCLK frequency can be changed separately for software by setting registers.

1.2.1 CGM Block Diagram

Following figure illustrates a block diagram of CGM.

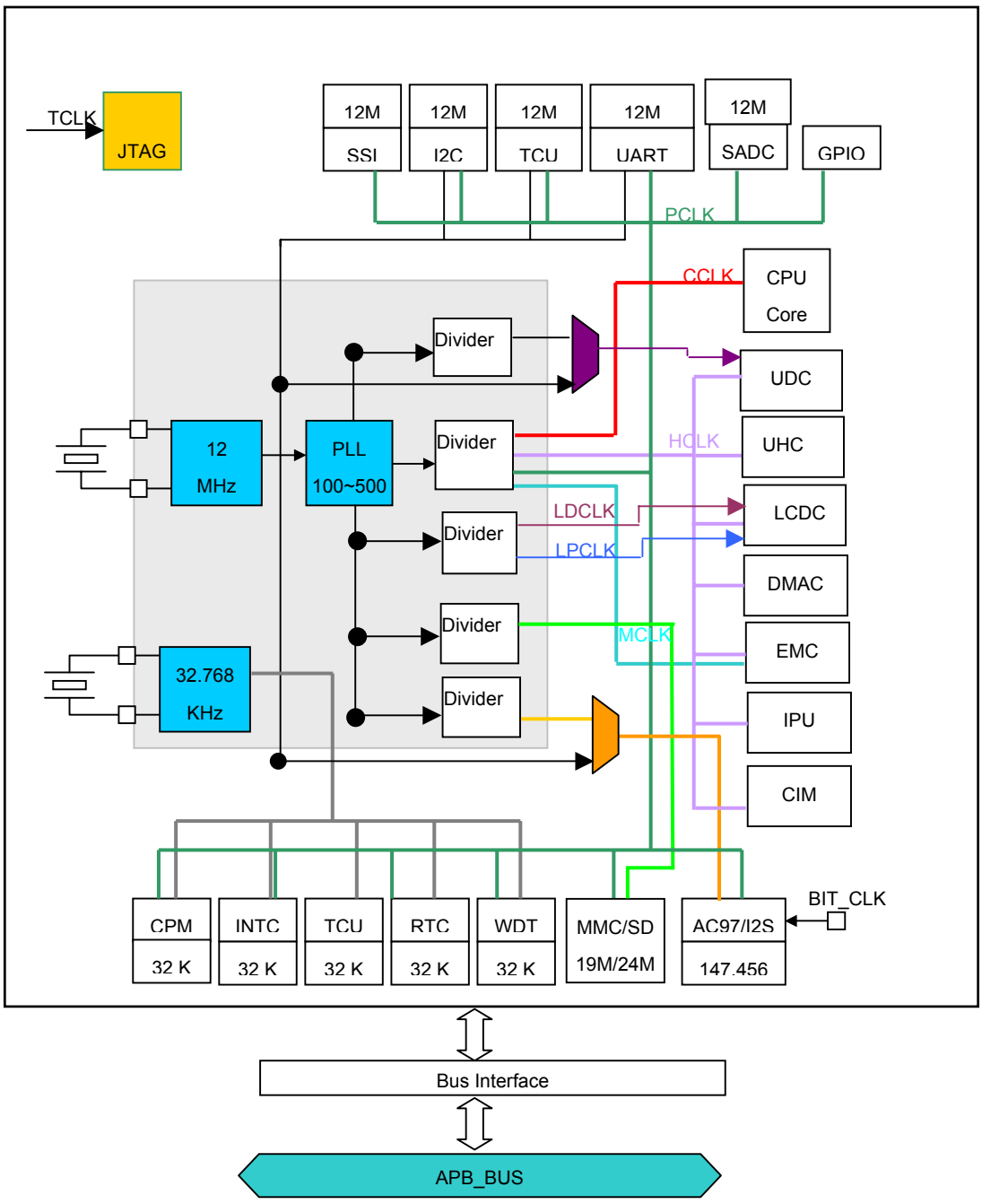


Figure 1-1 CGM Block Diagram

1.2.2 CGM Registers

All CGM register 32bit access address is physical address.

Table 1-1 CGM Registers Configuration

Name	description	RW	Reset Value	Address	Access Size
CPCCR	Clock Control Register	RW	0x42040000	0x10000000	32
CPPCR	PLL Control Register	RW	0x28080011	0x10000010	32
I2SCDR	I2S device clock divider Register	RW	0x00000004	0x10000060	32
LPCDR	LCD pix clock divider Register	RW	0x00000004	0x10000064	32
MSCCDR	MSC device clock divider Register	RW	0x00000004	0x10000068	32
UHCCDR	UHC 48M clock divider Register	RW	0x00000004	0x1000006C	32
UHCTST	UHC PHY test point register	RW	0x00000000	0x10000070	32
SSICDR	SSI clock divider Register	RW	0x00000004	0x10000074	32

1.2.2.1 Clock Control Register

The Clock Control Register (CPCCR) is a 32-bit read/write register, which controls CCLK, HCLK, PCLK, MCLK and LDCLK division ratios. It is initialized to 0x42040000 by any reset. Only word access can be used on CPCCR.

CPCCR **0x10000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	I2CS	CKOEN	UCS	UDIV						CE	PCS	LDIV					MDIV				PDIV				HDIV				CDIV			
RST	0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	I2CS	I2S Clock Source Selection. Selects the I2S clock source between PLL output and pin EXCLK. 0: I2S clock source is EXCLK 1: I2S clock source is PLL output divided by I2SDIV	RW
30	CLKOEN	SCLKO Output Enable. Controls the output of SCLKO 0: Disable SCLKO output. SCLKO is Hi-Z 1: Enable SCLKO output	RW
29	UCS	USB Clock Source Selection. Selects the USB clock source between PLL output and pin EXCLK. 0: USB clock source is pin EXCLK 1: USB clock source is PLL output	RW

<table>
<tr><td>28:23</td><td>UDIV</td><td>Divider for USB Clock Frequency. When USB clock source is PLL (UCS bit is 1), this field specified the USB clock division ratio, which varies from 1 to 64 (division ratio = UDIV + 1).</td><td>RW</td></tr>
<tr><td>22</td><td>CE</td><td>change enable. If CE is 1, writes on CDIV, HDIV, PDIV, MDIV, UDIV, PXDIV or LDIV will start a frequency changing sequence immediately. When CE is 0, writes on CDIV, HDIV, PDIV, MDIV, UDIV, PXDIV and LDIV will not start a frequency changing sequence immediately. The division ratio is actually updated in PLL multiple ratio changing sequence or PLL Disable Sequence.
0: Division ratios are updated in PLL multiple ratio changing sequence or PLL Disable Sequence
1: Division ratios are updated immediately</td><td>RW</td></tr>
<tr><td>21</td><td>PCS</td><td>PLL out clock source clock selection. It supplies source clock for MSC I2S LCD USB
0: divider clock source is PLL output divided by 2
1: divider clock source is PLL output</td><td>RW</td></tr>
<tr><td>20:16</td><td>LDIV</td><td>Divider for LCD device Clock Frequency. Specified the LCLK division ratio, which varies from 1 to 32 (division ratio = LDIV + 1). The frequency of LCLK must be equal to or less than 150 MHz.</td><td>RW</td></tr>
<tr><td>15:12</td><td>MDIV</td><td>Divider for Memory Clock Frequency. Specified the MCLK division ratio.
<table>
<tr><th colspan="4">Bit 15~12: MDIV</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>X1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>X1/2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>X1/3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>X1/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>X1/6</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>X1/8</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>X1/12</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>X1/16</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>X1/24</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>X1/32</td></tr>
<tr><td colspan="4">Other Value</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>11:8</td><td>PDIV</td><td>Divider for Peripheral Clock Frequency. Specified the PCLK division ratio.
<table>
<tr><th colspan="4">Bit 11~8: PDIV</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>X1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>X1/2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>X1/3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>X1/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>X1/6</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>X1/8</td></tr>
</table></td><td>RW</td></tr>
</table>

		0	1	1	0	X1/12	
		0	1	1	1	X1/16	
		1	0	0	0	X1/24	
		1	0	0	1	X1/32	
		Other Value				Reserved	

7:4	HDIV	Divider for System Clock Frequency. Specified the HCLK division ratio.	RW

Bit 7~4: HDIV				Description
0	0	0	0	X1
0	0	0	1	X1/2
0	0	1	0	X1/3
0	0	1	1	X1/4
0	1	0	0	X1/6
0	1	0	1	X1/8
0	1	1	0	X1/12
0	1	1	1	X1/16
1	0	0	0	X1/24
1	0	0	1	X1/32
Other Value				Reserved

3:0	CDIV	Divider for CPU Clock Frequency. Specifies the CCLK division ratio.	RW

BIT 3~0	Description	BIT 3~0	description
0 0 0 0 :	X1	0 0 0 1 :	X1/2
0 0 1 0 :	X1/3	0 0 1 1 :	X1/4
0 1 0 0 :	X1/6	0 1 0 1 :	X1/8
0 1 1 0 :	X1/12	0 1 1 1 :	X1/16
1 0 0 0 :	X1/24	1 0 0 1 :	X1/32
Other Value			Reserved

1.2.2.2 I2S device clock divider Register

I2S device clock divider Register (I2SCDR) is a 32-bit read/write register that specifies the divider of I2S device clock . This register is initialized to 0x00000004 only by any reset. Only word access can be used on I2SCDR

I2SCDR **0x10000060**

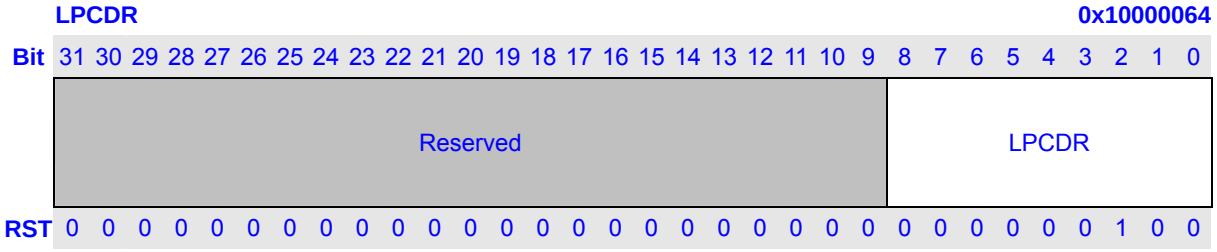
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								I2SCDR							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Description	RW

31:9	Reserved	Writes to these bits have no effect and always read as 0.	R
8:0	I2SCDR	Divider for I2S Frequency. Specified the I2S device clock division ratio, which varies from 1 to 512 (division ratio = I2SCDR + 1).	RW

1.2.2.3 LCD pix clock divider Register

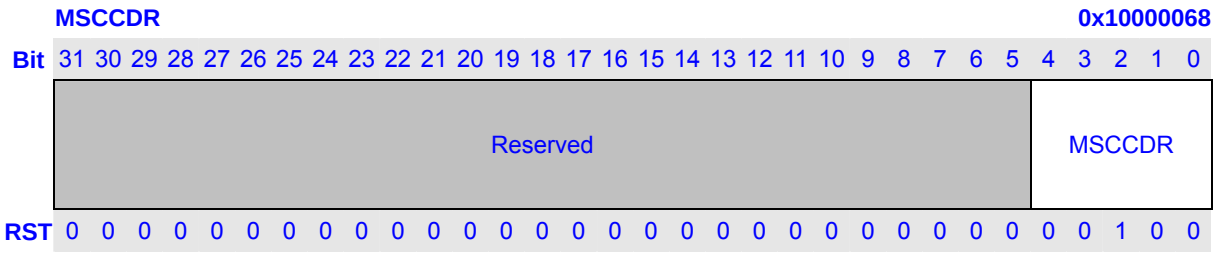
LCD pix clock divider Register (LPCDR) is a 32-bit read/write register that specifies the divider of LCD pixel clock (LPCLK). This register is initialized to 0x00000004 only by any reset. Only word access can be used on LPCDR



Bits	Name	Description	RW
31:9	Reserved	Writes to these bits have no effect and always read as 0.	R
8:0	LPCDR	Divider for Pixel Frequency. Specified the LCD pixel clock (LPCLK) division ratio, which varies from 1 to 512 (division ratio = LPCDR + 1).	RW

1.2.2.4 MSC device clock divider Register

MSC device clock divider Register (MSCCDR) is a 32-bit read/write register that specifies the divider of MSC device clock . This register is initialized to 0x00000004 only by any reset. Only word access can be used on MSCCDR



Bits	Name	Description	RW
31:5	Reserved	Writes to these bits have no effect and always read as 0.	R
4:0	MSCCDR	Divider for MSC Frequency. Specified the MSC device clock division ratio, which varies from 1 to 32 (division ratio = MSCCDR + 1).	RW

1.2.2.5 UHC device clock divider Register

UHC device clock divider Register (UHCCDR) is a 32-bit read/write register that specifies the divider of UHC 48M device clock . This register is initialized to 0x00000004 only by any reset. Only word access can be used on UHCCDR

UHCCDR **0x1000006C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												UHCCDR			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Description	RW
31:4	Reserved	Writes to these bits have no effect and always read as 0.	R
3:0	UHCCDR	Divider for UHC Frequency. Specified the UHC 48M device clock division ratio, which varies from 1 to 16 (division ratio = UHCCDR + 1).	RW

1.2.2.6 UHC PHY test point Register

UHC PHY test point Register (UHCTST) is a 32-bit read/write register. This register is initialized to 0x00000000. only by any reset. Only word access can be used on UHCTST

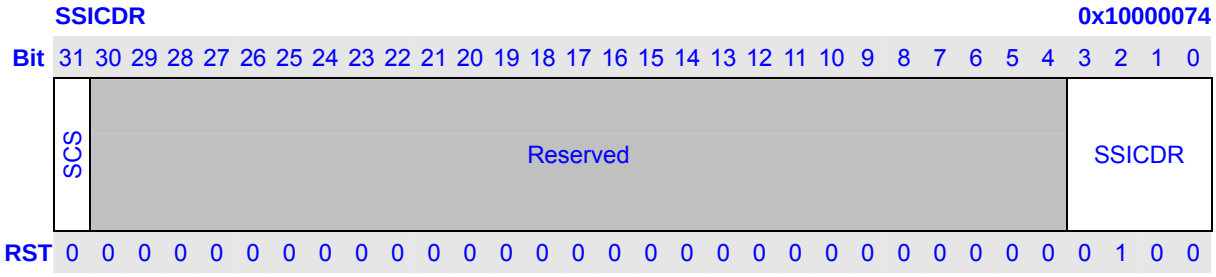
UHCTST **0x10000070**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								UHTST							
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	0	0	0	1	0	0

Bits	Name	Description	RW
31:9	Reserved	Writes to these bits have no effect and always read as 0.	R
8	rcvdata	UHC PHY rcvdata input	R
7	dm	UHC PHY dm input	R
6	dp	UHC PHY dp input	R
5	Testmod	UHC test mode	RW
4	txenl		RW
3	speed		RW
2	Txse0		RW
1	txdm		RW
0	txdp		RW

1.2.2.7 SSI device clock divider Register

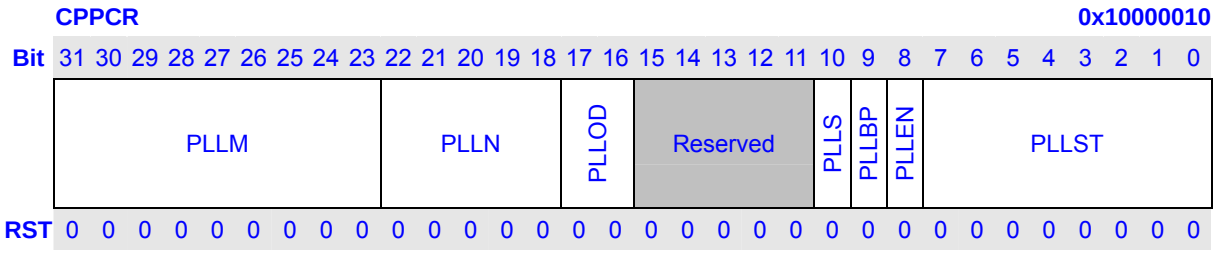
SSI device clock divider Register (SSICDR) is a 32-bit read/write register that specifies the divider of SSI device clock . This register is initialized to 0x00000004 only by any reset. Only word access can be used on SSICDR



Bits	Name	Description	RW
31	SCS	SSI Clock Source Selection. Selects the SSI clock source between PLL output and pin EXCLK. 0: SSI clock source is pin EXCLK 1: SSI clock source is PLL output	RW
30:4	Reserved	Writes to these bits have no effect and always read as 0.	R
3:0	SSICDR	Divider for SSI Frequency. Specified the SSI device clock division ratio, which varies from 1 to 16 (division ratio = SSICDR + 1).	RW

1.2.2.8 PLL Control Register

The PLL Control Register (CPPCR) is a 32-bit read/write register, which controls PLL multiplier, on/off state and stabilize time. It is initialized to 0x28080011 only by any reset. Only word access can be used on CPPCR.



Bits	Name	Description	RW
31:23	PLLM	the PLL feedback 9-bit divider	RW
22:18	PLLN	the PLL input 5-bit divider	RW
17:16	PLLOD	00: divide by 1 01: divide by 2	RW

		10: divide by 2 11: divide by 4	
15:11	Reserved	Writes to these bits have no effect and always read as 0	R
10	PLLS	PLL Stabilize Flag 0: PLL is off or not stable 1: PLL is on and stable	R
9	PLLBP	PLL Bypass. If PLLEN is 1, set this bit to1 will bypass PLL. The PLL is still running background but the source of associated dividers is switched to 12-M. If PLLEN is 0, set this bit to 1 has no effect. If PLLEN is 1, clear this bit to 0 will switch the source of associated dividers to PLL output.	RW
8	PLLEN	PLL Enable. When PLLEN is set to 1, PLL starts to lock phase. After PLL stabilizes, PLLS bit is set. If PLLBP is 0, the source of associated dividers, is switched to PLL output. When PLLEN is clear to 0, PLL is shut off and the source of associated dividers is switched to 12-MHz in spite of PLLBP bit	RW
7:0	PLLST	PLL Stabilize Time. Specifies the PLL stabilize time by unit of RTCCLK (approximate 32kHz) cycles. It is used when change PLL multiplier or change PLL from off to on. It is initialized to H'11	RW

1.2.3 PLL Operation

The PLL developed as a macro cell for clock generator. It can generate a stable high-speed clock from a slower clock signal. The output frequency is adjustable and can be up to 500MHz. The PLL integrates a phase frequency detector (PFD), a low pass filter (LPF), a voltage controlled oscillator (VCO) and other associated support circuitry. All fundamental building blocks as well as fully programmable dividers are integrated on the core. It is useful for clock multiplication of stable crystal oscillator sources and for de-skew clock signals.

The PLL block diagram is shown in following figure

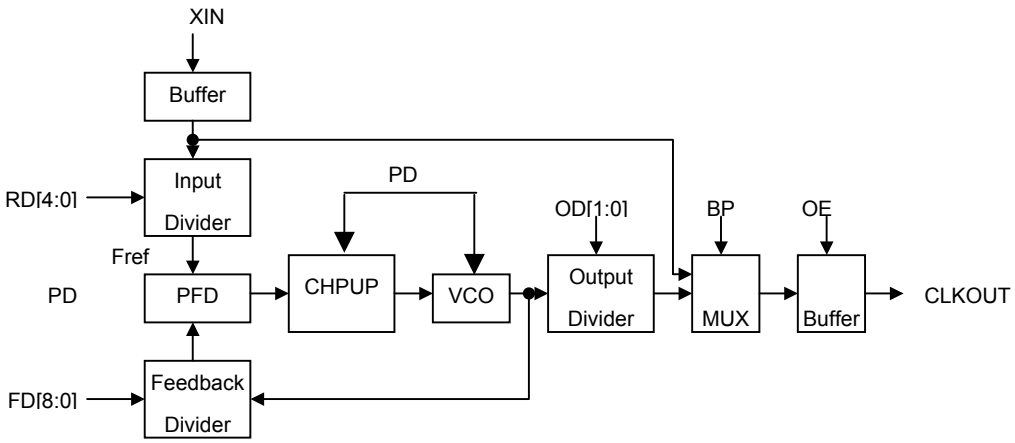


Figure 1-2 Block Diagram of PLL

1.2.3.1 PLL Configuration

– PLL Divider Value Setting

There are 3 divider values (N, M and NO) to set the PLL output clock frequency CLKOUT:

– Input Divider Value N

N = PLLN of CPPCR + 2

– Feedback Divider Value M

M = PLLM of CPPCR + 2

– Output Divider Value NO

Output Divider Setting (OD)	Output Divider Value (NO)
0	1

1	2
2	2
3	4

– The PLL output frequency, CLK_OUT, is determined by the ratio set between the value set in the input divider and the feedback divider. PLL output frequency CLK_OUT is calculated from the following equations:

CLKOUT = XIN x (M / N) x (1/ NO)

M = F0 *1 + F1*2 + F2*4 + F3*8 + F4*16 + F5*32 + F6*64 + F7*128 + F8*256 + 2
N = R0*1 + R1*2 + R2*4 + R3*8 + R4*16 + 2
NO = $2^{od0+od1}$

Where:

CLK_OUT represents the output frequency
XIN represents PLL input frequency
N represents input divider value
M represents feedback divider value
NO represents output divider value

< Attention >
1. 1MHZ ≤ XIN/N ≤ 15MHZ
2. 100MHZ ≤ CLK_OUT x NO ≤ 500MHZ

1.2.4 Main Clock Division Change Sequence

Main clock (CCLK, HCLK, PCLK and MCLK) frequencies can be changed separately or simultaneously by changing division ratio. Following conditions must be obeyed:

– CCLK must be integral multiple of HCLK
– The frequency ratio of CCLK and HCLK can not be 24 and 32
– HCLK must be equal to MCLK or twice of MCLK
– HCLK and MCLK must be integral multiple of PCLK.

Don't violate this limitation, otherwise unpredictable error may occurs.

In normal mode, if CE bit of CPCCR is 1, changing CDIV, HDIV, PDIV or MDIV will start a Division Change Sequence immediately. If CE bit of CPCCR is 0, changing CDIV, HDIV, PDIV or MDIV will not start Division Change Sequence.

1.2.5 Change Other Clock Frequencies

The divider of LCD device clock (LDCLK), LCD pixel clock (LPCLK), I2S device clock, MSC device clock and USB clock can be changed by programming LDIV, LPCDR ,I2SCDR, MSCCDR and UDIV, respectively.

Change LDIV LPCDR I2SCDR MSCCDR and UDIV as following steps:

1. Stop related devices with clock-gate function. Clock supplies to the devices are stopped.
2. Change LDIV, LPCDR, I2SCDR, MSCCDR or UDIV. If CE is 1, clock frequencies are changed immediately. If CE is 0, clock frequencies are not changed until PLL Multiplier Change Sequence is started.
3. Cancel above clock-gate function.

1.2.6 Change Clock Source Selection

USB, I2S device clocks can be selected from two sources. Before change clock source, corresponding devices should be stopped using clock-gate function.

- When USB clock source is changed (UCS bit of CPCCR), USB clock should be stopped.
- When I2S clock source is changed (I2CS bit of CPCCR), AIC should be stopped.

When UCS, I2CS bit is changed, clock source is changed immediately.

1.3 Power Manager

In the Low-Power mode, part or whole processor is halted. This will reduce power consumption. The Power Management Controller contains low-power mode control and reset sequence control

1.3.1 Low-Power Modes and Function

The processor supports six low-power modes and function:

- NORMAL mode

  In Normal mode, all peripherals and the basic blocks including power management block, the CPU core, the bus controller, the memory controller, the interrupt controller, DMA, and the external master may operate completely. But, the clock to each peripheral, except the basic blocks, can be stopped selectively by software to reduce the power consumption.

- DOZE mode

  DOZE mode is entered by setting DOZE bit of LCR to 1. In DOZE mode, clock is burst to CPU core and the clock duty is set by DUTY field of LCR. DOZE mode is canceled by reset, interrupt or clearing DOZE bit to 0. Continuous clock is supplied immediately after DOZE mode is canceled. The other Clocks except CCLK run continuously in DOZE mode.

- IDLE mode

  In IDLE mode, the clock to the CPU core is stopped except the bus controller, the memory controller, the interrupt controller, and the power management block. To exit the IDLE mode, the any interrupts should be activated.

- SLEEP mode

  In SLEEP mode, all clocks except RTC clock are disabled. PLL is disabled also. SLEEP mode is canceled by reset or interrupt. When SLEEP mode is canceled, PLL is restarted , the PLL needs clock stabilization time (PLL lock time). This PLL stabilization time is automatically inserted by the internal logic with lock time count register. and all clocks start operating after PLL stability time.

- HIBERNATE mode

  In HIBERNATE mode, the CORE power and IO power shut down. So, there occurs no power Consumption to CHIP except the RTC and wake-up logic. HIBERNATE mode is cancelled by programmable wakeup event. When HIBERNATE mode is cancelled, wakeup reset occurs except RTC. The hibernating mode is controlled by RTC module. Please reference to RTC spec the details.

- CLOCK GATE function

  CLOCK GATE function is used to gate specified on-chip module when it is not used. Set specified CLKG0~15 bits in CLKGR will enter specified CLK gate function. CLOCK gate function is canceled by reset or clearing specified CLKGR0~15 to 0.

1.3.2 Register Description

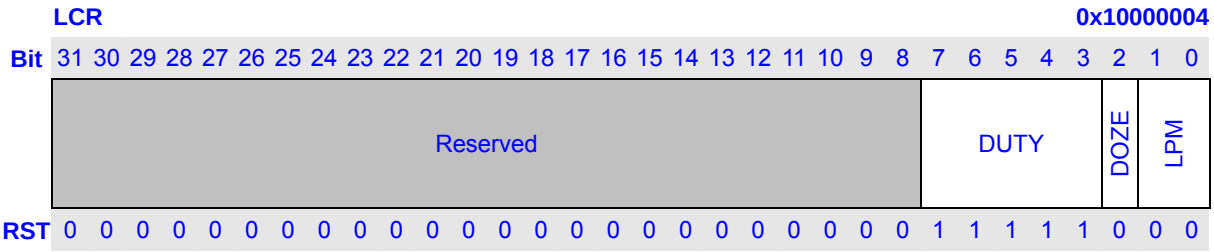
All PMC register 32bit access address is physical address.

Table 1-2 Power/Reset Management Controller Registers Configuration

Name	description	RW	Initial Value	Address	Access Size
LCR	Low Power Control Register	RW	0x000000F8	0x10000004	32
CLKGR	Clock Gate Register	RW	0x00000000	0x10000020	32
SCR	Sleep Control Register	RW	0x00001500	0x10000024	32

1.3.2.1 Low Power Control Register

The Low Power Control Register (LCR) is a 32-bit read/write register that controls low-power mode status. It is initialized to 0x000000F8 by any reset.



Bits	Name	Description	RW
31:8	Reserved	Writes to these bits have no effect and always read as 0	R
7:3	DUTY	CPU Clock Duty. Control the CPU clock duty in doze mode. When the DUTY field is 0x1F, the clock is always on and when it is zero, the clock is always off. Set the DUTY field to 0 when the CPU will be disabled for an extended amount of time. 00000 = 0/31 duty-cycle 00001 = 1/31 duty-cycle 00010 = 2/31 duty-cycle … 11111 = 31/31 duty-cycle	RW
2	DOZE	Doze Mode. Control the doze mode. When doze mode is canceled, this	RW

		bit is cleared to 0 automatically 0: Doze mode is off 1: Doze mode is on	
1:0	LPM	Low Power Mode. Specifies which low-power mode will be entered when SLEEP instruction is executed Bit 1~0: **00**: IDLE mode will be entered when SLEEP instruction is executed **01**: SLEEP mode will be entered when SLEEP instruction is executed **10**: Reserved **11**: Reserved	RW

1.3.2.2 Clock Gate Register

The Clock Gate Register (CLKGR) is a 32-bit read/write register that controls the CLOCK GATE function of peripherals. It is initialized to 0x00000000 by any reset.

CLKGR **0x10000020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																CLKGR															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:15	Reserved	Writes to these bits have no effect and always read as 0	R
14:0	CLKGR	Clock gate Bits. Controls the clock supplies to some peripherals. If set, clock supplies to associated devices are stopped, and registers of the device cannot be accessed also	RW

Bit	Module	Description
15	UART1	
14	UHC	
13	IPU	
12	DMAC	
11	UDC	0: udc_hclk always running, don't stop
10	LCD	
9	CIM	
8	SADC	
7	MSC	
6	AIC	Affects both AC97 bitclk and I2S clock

		6	AIC	Affects both AC97 bitclk and I2S clock	
		5	AIC	Affects PCLK supply of AIC	
		4	SSI		
		3	I2C		
		2	RTC	The second counter is still counting	
		1	TCU		
		0	UART0		

1.3.2.3 Sleep Control Register (SCR)

The Sleep Control Register is a 32-bit read/write register that specifies some special controls of SLEEP mode. It is initialized to 0x00001500 by reset.

SCR **0x10000024**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TPE_ADC	TPE_CDC	Reserved														O1ST								SPENDH	SPENDD	Reserved	O1SE	Reserved			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	TPE_ADC	Test SADC point .	RW
30	TPE_CDC	Test Codec point	RW
31:16	Reserved	Writes to these bits have no effect and always read as 0	R
15:8	O1ST	12MHz Oscillator Stabilize Time. This filed specifies the 12Mhz oscillator stabilize time by unit of 16 RTCCLK periods (oscillator stable time O1ST × 16 / 32768) cycles. It is initialized to H'15.	RW
7	SPENDH	Force UHC phy to enter suspend mode 0: UHC phy hasn't forced to entered SUSPEND mode 1: UHC phy has forced to entered SUSPEND mode	RW
6	SPENDN	force UDC phy to enter suspend mode 0: UDC phy has forced to entered SUSPEND mode 1: UDC phy hasn't forced to entered SUSPEND mode	RW
5	Reserved	Writes to these bits have no effect and always read as 0	R
4	O1SE	12MHz Oscillator Sleep Mode Enable. This filed controls the state of the 12Mhz oscillator in Sleep mode. 0: 12M oscillator is disabled in Sleep mode 1: 12M oscillator is enabled in Sleep mode	RW
3:0	Reserved	Writes to these bits have no effect and always read as 0	R

1.3.3 Doze Mode

Firstly, software should set the DUTY bits of LCR. Then set DOZE bit of LCR to 1 to enter doze mode. When slot controller of PMC indicates that the CPU clock's time-slot has expired, CPU is halted but its register contents are retained. During doze mode, program can modify clock duty-cycle according to core resource requirement. Clock control is in increments of approximately 3% (1/31).

Doze is exited by software, interrupt, reset or SLEEP instruction.

1.3.4 IDLE Mode

In normal or mode, when LPM bits in LCR are 0 and SLEEP instruction is executed, the processor enters idle mode. CPU is halted but its register contents are retained All critical application must be finished and peripherals must be configured to generate interrupts when they need CPU attention.

The procedure of entering sleep mode is shown blow:

1. Set LPM bits in LCR to 0.
2. Executes SLEEP instruction.
3. When current operation of CPU core has finished and CPU core is idle, CCLK supply to CPU core is stopped.

IDLE mode is exited by an interrupt (IRQ or on-chip devices) or a reset.

1.3.5 SLEEP Mode

In normal mode, when LPM bits in LCR is 1 and SLEEP instruction is executed, the processor enter SLEEP mode. CPU and on-chip devices are halted, except some wakeup-logic. PLL is shut off. Clock output from SCLKO pin is also stopped. SDRAM content is preserved by driving into self-refresh state. CPU registers and on-chip devices registers contents are retained

Before enter SLEEP mode, software should ensure that all peripherals are not running. The procedure of entering SLEEP mode is shown blow:

1. Set LPM bit in LCR to 1.
2. Execute a SLEEP instruction.
3. When current access on system bus complete, the arbiter will not grant any following request. EMC will drive SDRAM from auto-refresh mode to self-refresh mode.
4. When system bus is idle state and SDRAM is self-refresh mode, internal clock supplies are stopped.

SLEEP mode can be exited by an interrupt (IRQ or on-chip devices), WDT reset or a poweron reset via the RESETP pin.

1.4 Reset Control Module

1.4.1 Register Description

All RCM register 32bit access address is physical address.

Name	description	RW	Initial Value	Address	Access Size
RSR	Reset Status Register	RW	0x????????	0x10000008	32

1.4.1.1 Reset Status Register (RSR)

The Reset Status Register (RSR) is a 32-bit read/write register which records last cause of reset. Each RSR bit is set by a different source of reset. Please refer to Reset Sequence Control for reset sources description.

RSR 0x10000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														WR	PR
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?

Bits	Name	Description	RW
31:2	Reserved	Writes to these bits have no effect and always read as 0	R
1	WR	WDT Reset. When a WDT reset is detected, WR is set and remains set until software clears it or another reset occurs. This bit can only be written with 0. Write with 1 will be ignored 0: WDT reset has not occurred since the last time the software clears this bit 1: WDT reset has occurred since the last time the software clears this bit	RW
0	PR	Power On Reset. When a poweron reset via PRESET pin is detected, PR is set and remains set until software clears it or another reset occurs. This bit can only be written with 0. Write with 1 is ignored 0: Power on reset has not occurred since the last time the software clears this bit 1: Power on reset has occurred since the last time the software clears this bit	RW

1.4.2 Reset Sources and Pins

Any qualified global reset signal resets the JZ47xx and all related peripherals to their default state. After the internal reset is deasserted, the JZ47xx processor begins fetching code from the internal bootstrap ROM or CS0 space. The memory location of the fetch depends on the configuration of the BOOT pins.

Signal	Direction	Description
PRESET	IN	**Power On Reset**—An active low signal that resets the JZ47xx..
WRESET	internal	**Watchdog Timer Reset**—An active low signal generated by the watchdog timer when a time-out period has expired. Resets the same modules as PRSET.

1.4.3 Power On Reset

Power on reset is generated when PRESET pin is driven to low. Internal reset is asserted immediately. All pins return to their reset states.

PRESET pin must be held low until power stabilizes and the 12MHz oscillator stabilize. CPU and peripherals are clocked by 12MHz oscillator output directly. PLL is reset to off state. All internal modules are initialized to their predefined reset states.

1.4.4 WDT Reset

WDT reset is generated when WDT overflow. Internal reset is asserted within two RTCCLK cycles.

All pins return to their reset states.

Then WDT reset source is cleared because of internal reset. The internal reset is asserted for about 10 milliseconds. CPU and peripherals are clocked by 12MHz oscillator output directly. PLL is reset to off state.