1 DMA Controller

DMA controller (DMAC) is dedicated to transfer data between on-chip peripherals (MSC, AIC, UART, etc.), external memories, and memory-mapped external devices.

1.1 Features

- Support up to 6 independent DMA channels
- Descriptor or No-Descriptor Transfer
- Transfer data units: byte, 2-byte (half word), 4-byte (word), 16-byte or 32-byte
- Transfer number of data unit: 1 ~ 2^{24}
- Independent source and target port width: 8-bit, 16-bit, 32-bit
- Two channel priority modes: fixed, round robin.

1.2 Register Descriptions

Table 1-1 DMAC Registers

Name	Description	RW	Reset Value	Address	Access Size (bit)
DSA0	DMA Source Address 0	RW	0x0	0x13020000	32
DTA0	DMA Target Address 0	RW	0x0	0x13020004	32
DTC0	DMA Transfer Count 0	RW	0x0	0x13020008	32
DRT0	DMA Request Source 0	RW	0x0	0x1302000C	32
DCS0	DMA Channel Control/Status 0	RW	0x0	0x13020010	32
DCM0	DMA Command 0	RW	0x0	0x13020014	32
DDA0	DMA Descriptor Address 0	RW	0x0	0x13020018	32
DSA1	DMA Source Address 1	RW	0x0	0x13020020	32
DTA1	DMA Target Address 1	RW	0x0	0x13020024	32
DTC1	DMA Transfer Count 1	RW	0x0	0x13020028	32
DRT1	DMA Request Source 1	RW	0x0	0x1302002C	32
DCS1	DMA Channel Control/Status 1	RW	0x0	0x13020030	32
DCM1	DMA Command 1	RW	0x0	0x13020034	32
DDA1	DMA Descriptor Address 1	RW	0x0	0x13020038	32
DSA2	DMA Source Address 2	RW	0x0	0x13020040	32
DTA2	DMA Target Address 2	RW	0x0	0x13020044	32
DTC2	DMA Transfer Count 2	RW	0x0	0x13020048	32
DRT2	DMA Request Source 2	RW	0x0	0x1302004C	32
DCS2	DMA Channel Control/Status 2	RW	0x0	0x13020050	32
DCM2	DMA Command 2	RW	0x0	0x13020054	32
DDA2	DMA Descriptor Address 2	RW	0x0	0x13020058	32
DSA3	DMA Source Address 3	RW	0x0	0x13020060	32
DTA3	DMA Target Address 3	RW	0x0	0x13020064	32
DTC3	DMA Transfer Count 3	RW	0x0	0x13020068	32
DRT3	DMA Request Source 3	RW	0x0	0x1302006C	32
DCS3	DMA Channel Control/Status 3	RW	0x0	0x13020070	32
DCM3	DMA Command 3	RW	0x0	0x13020074	32
DDA3	DMA Descriptor Address 3	RW	0x0	0x13020078	32
DSA4	DMA Source Address 4	RW	0x0	0x13020080	32
DTA4	DMA Target Address 4	RW	0x0	0x13020084	32
DTC4	DMA Transfer Count 4	RW	0x0	0x13020088	32
DRT4	DMA Request Source 4	RW	0x0	0x1302008C	32
DCS4	DMA Channel Control/Status 4	RW	0x0	0x13020090	32
DCM4	DMA Command 4	RW	0x0	0x13020094	32
DDA4	DMA Descriptor Address 4	RW	0x0	0x13020098	32

DSA5	DMA Source Address 5	RW	0x0	0x130200A0	32
DDA5	DMA Target Address 5	RW	0x0	0x130200A4	32
DTC5	DMA Transfer Count 5	RW	0x0	0x130200A8	32
DRT5	DMA Request Source 5	RW	0x0	0x130200AC	32
DCS5	DMA Channel Control/Status 5	R/W	0x0	0x130200B0	32
DCM5	DMA Command 5	RW	0x0	0x130200B4	32
DDA5	DMA Descriptor Address 5	RW	0x0	0x130200B8	32
DMAC	DMA Control	R/W	0x0	0x13020300	32
DIRQP	DMA Interrupt Pending	R	0x0	0x13020304	32
DDR	DMA Doorbell	RW	0x0	0x13020308	32
DDRS	DMA Doorbell Set	W	0x0	0x1302030C	32

1.2.1 DMA Source Address (DSAn, n = 0 ~ 5)

DSA0, DSA1, DSA2, DSA3, DSA4, DSA5 — **0x13020000, 0x13020020, 0x13020040, 0x13020060, 0x13020080, 0x130200a0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	SA	Source address	RW

1.2.2 DMA Target Address (DTAn, n = 0 ~ 5)

DTA0, DTA1, DTA2, DTA3, DTA4, DTA5 — **0x13020004, 0x13020024, 0x13020044, 0x13020064, 0x13020084, 0x130200a4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TA																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	TA	Target address	RW

1.2.3 DMA Transfer Count (DTCn, n = 0 ~ 5)

DTC0, DTC1, DTC2, DTC3, DTC4, DTC5 — **0x13020008, 0x13020028, 0x13020048, 0x13020068, 0x13020088, 0x130200a8**

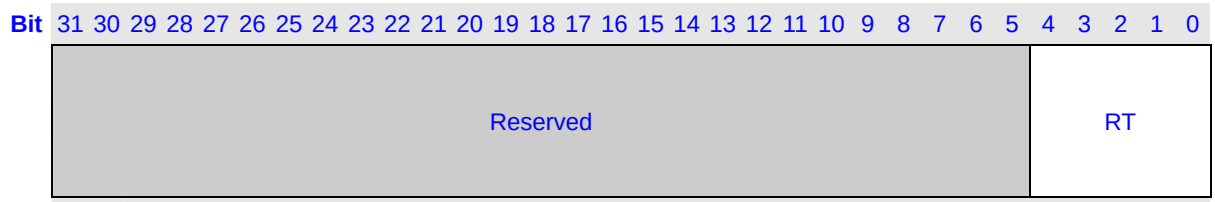
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Name	Description	RW
31:24	Reserved	Write has no effect, read as zero	R
23:0	TC	Hold the number of data unit to transfer and it counts down to 0 at the end	RW

1.2.4 DMA Request Types (DRTn, n = 0 ~ 5)

DRT0, DRT1, DRT2, **0x1302000c, 0x1302002c, 0x1302004c,**

DRT3, DRT4, DRT5 **0x1302006c, 0x1302008c, 0x130200ac**



Bits	Name	Description	RW
31:5	Reserved	Write has no effect, read as zero	R
4:0	RT	Transfer request type	RW

Table 1-2 Transfer Request Types

RT4-0	Description
0~7	Reserved
8	Auto-request (ignore RDIL3-0, external address → external address)
9~19	Reserved
20	UART transmit-fifo-empty transfer request (external address → UTHR)
21	UART receive-fifo-full transfer request (URBR → external address)
22	SSI transmit-fifo-empty transfer request
23	SSI receive-fifo-full transfer request
24	AIC transmit-fifo-empty transfer request
25	AIC receive-fifo-full transfer request
26	MSC transmit-fifo-empty transfer request
27	MSC receive-fifo-full transfer request
28	TCU channel n (overflow interrupt, external address→external address space)
29	SADC transfer request (SADC → external address)
30	SLCD transfer request (external address → SLCD)
31	Reserved

NOTES:

1. Only auto request can be concurrently selected in all channels with different source and target address.

2. For on-chip device DMA request except TCU, the corresponding source or target address that map to on-chip device must be set as fixed.

1.2.5 DMA Channel Control/Status (DCSn, n = 0 ~ 5)

DCS0, DCS1, DCS2, 0x13020010, 0x13020030, 0x13020050,
DCS3, DCS4, DCS5 0x13020070, 0x13020090, 0x130200b0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NDES	Reserved							CDOA								Reserved									INV	Reserved	AR	TT	HLT	CT	CTE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	NDES	Descriptor or No-Descriptor Transfer Select: 0, Descriptor Transfer; 1, No-descriptor Transfer	RW
30:24	Reserved	Write has no effect, read as zero	R
23:16	CDOA	Copy of offset address of last completed descriptor from that in DMA command register. Software could know which descriptor is just completed combining with count terminate interrupt resulted by DCSn.CT (Ignored in No-Descriptor Transfer)	RW
15:7	Reserved	Write has no effect, read as zero	R
6	INV	Descriptor Invalid error: 0, no invalid error; 1, descriptor invalid, DCMn.V bit is loaded as 0 (Ignored in No-Descriptor Transfer)	RW
5	Reserved	Write has no effect, read as zero	R
4	AR	Address Error: 0, no address error; 1, address error	RW
3	TT	Transfer Terminate: 0, No-Link Descriptor or No-Descriptor DMA transfer does not end; 1, No-Link Descriptor or No-Descriptor DMA transfer end	RW
2	HLT	DMA halt: 0, DMA transfer is in progress; 1, DMA halt	RW
1	CT	Count Terminate: 0, Link DMA transfer does not end; 1, Link DMA transfer end (Ignored in No-Descriptor Transfer)	RW
0	CTE	Channel transfer enable: 0, disable; 1, enable	RW

1.2.6 DMA Channel Command (DCMn, n = 0 ~ 5)

DCM0, DCM1, DCM2, 0x13020014, 0x13020034, 0x13020054,
DCM3, DCM4, DCM5 0x13020074, 0x13020094, 0x130200b4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

	Reserved	SAI	DAI	Reserved	RDIL	SP	DP	Reserved	TSZ	TM	Reserved	V	VM	VIE	TIE	LINK
RST	0 0 0 0 0 0 0 0	0	0	0 0 0 0	0 0 0 0 0 0 0 0	0 0	0 0	0 0	0 0 0 0	0	0 0 0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	Write has no effect, read as zero	R
23	SAI	Source Address Increment: 0, no increment; 1, increment	RW
22	DAI	Target Address Increment: 0, no increment; 1, increment	RW
19:16	RDIL	Request Detection Interval Length: Set the number of transfer unit between two requests detection in single mode. Please refer to following Table 1-3	RW
15:14	SP	Source port width: 00, 32-bit; 01, 8-bit; 10, 16-bit; 11, reserved	RW
13:12	DP	Target port width: 00, 32-bit; 01, 8-bit; 10, 16-bit; 11, reserved	RW
11	Reserved	Write has no effect, read as zero	R
10:8	TSZ	Transfer Data Size of a data unit: 000, 32-bit; 001, 8-bit; 010, 16-bit; 011, 16-byte; 100, 32-byte; others, reserved	RW
7	TM	Transfer Mode: 0, single mode; 1, block mode	RW
6:5	Reserved	Write has no effect, read as zero	R
4	V	Descriptor Valid flag: 0, Descriptor Invalid; 1, Descriptor Valid for transfer (Ignored in No-Descriptor Transfer and in Descriptor Transfer with VM=0)	R
3	VM	Descriptor Valid Mode: 0, V bit is ignored; 1, Support V bit (Ignored in No-Descriptor Transfer)	RW
2	VIE	DMA Valid Error Interrupt Enable: 0, disable; 1, enable (Ignored in No-Descriptor Transfer)	RW
1	TIE	Transfer Interrupt Enable (TIE): 0, disable interrupt; 1, enable interrupt	RW
0	LINK	Descriptor Link Enable: 0, disable; 1, enable (Ignored in No-Descriptor Transfer)	RW

Table 1-3 Detection Interval Length

RDIL	Description

0	Interval length is 0
1	Interval length is 2 transfer unit
2	Interval length is 4 transfer unit
3	Interval length is 8 transfer unit
4	Interval length is 12 transfer unit
5	Interval length is 16 transfer unit
6	Interval length is 20 transfer unit
7	Interval length is 24 transfer unit
8	Interval length is 28 transfer unit
9	Interval length is 32 transfer unit
10	Interval length is 48 transfer unit
11	Interval length is 60 transfer unit
12	Interval length is 64 transfer unit
13	Interval length is 124 transfer unit
14	Interval length is 128 transfer unit
15	Interval length is 200 transfer unit

1.2.7 DMA Descriptor Address (DDAn, n = 0 ~ 5)

This register is ignored in No-Descriptor Transfer.

DDA0, DDA1, DDA2, DDA3, DDA4, DDA5 — **0x13020018, 0x13020038, 0x13020058, 0x13020078, 0x13020098, 0x130200b8**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBA																				DOA								Reserved			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:12	DBA	Descriptor Base Address	RW
11:4	DOA	Descriptor Offset Address	RW
3:0	Reserved	Write has no effect, read as zero	R

1.2.8 DMA Control

DMAC — **0x13020300**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																						PM		Reserved				HLT	AR	Reserved	DMAE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:10	Reserved	Write has no effect, read as zero.	R
9:8	PM	Channel priority mode: 00, CH0 > CH1 > CH2 > CH3 > CH4 > CH5 01, CH0 > CH2 > CH3 > CH1 > CH4 > > CH5 10, CH2 > CH0 > CH1 > CH3 > CH4 > CH5 11, round robin	RW
7:4	Reserve	Write has no effect, read as zero.	R
3	HLT	Global halt status, halt occurs in any channel, the bit should set to 1. 0, no halt 1, halt occurred	RW
2	AR	Global address error status, address error occurs in any channel, the bit should be set to 1. 0, no address error 1, address error occurred	RW
1	Reserved	Write has no effect, read as zero.	R
0	DMAE	Global DMA transfer enable. 0, disable DMA channel transfer 1, enable DMA channel transfer	RW

1.2.9 DMA Doorbell (DDR)

DDR **0x13020308**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										DB5	DB4	DB3	DB2	DB1	DB0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:8	Reserved	Write has no effect, read as zero	R
7:0	DBn	DMA Doorbell for each channel, n=0~5, for example DB0 is for DMA channel 0. Software set it to 1 and hardware clears it to 0. 0, disable DMA controller to fetch the first descriptor or DMA controller clears it to 0 as soon as it starts to fetch the descriptor 1, Write 1 to DDS will set the corresponding DBn bit to 1 and enable DMA controller to fetch the first descriptor For example, write 0x00000001 to DDS, DB0 bit is set to 1 and enable DMA channel 0 to fetch the first descriptor. Write 0 to DDS, no meaning.	RW

1.2.10 DMA Interrupt Pending (DIRQP)

DIRQP **0x13020304**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																										CIRQ5	CIRQ4	CIRQ3	CIRQ2	CIRQ1	CIRQ0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:6	Reserved	Write has no effect, read as zero.	R
5:0	CIRQn	CIRQn (n=0~5) denotes pending status for corresponding channel 0, no abnormal situation or normal DMA transfer is in progress 1, abnormal situation occurred or normal DMA transfer done	RW

1.3 DMA manipulation

1.3.1 Descriptor Transfer

To do proper Descriptor DMA transfer, do as following steps:

1. First of all, check whether the status of DMA controller are available, that is, for global control (DMAC), ensure that DMAC.AR=0 and DMAC.HLT=0; while for expected channels, ensure that DCSn.AR=0, DCSn.HLT=0, DCSn.TT=0, DTCn=0 and DCSn.INV=0.
2. Set DMAC.DMAE=1 and expected DCSn.CTE=1 to launch DAM transfer
3. For Descriptor transfer, guarantee DCSn.NDES=0
4. Build descriptor in memory. Write the first descriptor address in DDAn and the address must be 16Bytes aligned. The descriptor address includes two parts: Base and Offset address. If the descriptor is linked, the 32-bit address of next descriptor is composed of 20-bit Base address in DDAn and 8-bit Offset address in DES3.DOA and the four LSB is 0x0. See Table 1-4 for the detailed 4-word descriptor structure.
5. Set 1 to the corresponding bit in DDR to initiate descriptor fetch
6. Hardware clears the corresponding bit in DDR as soon as it starts to fetch the descriptor.
7. If DES0.V =0 and DES0.VM=1, DMAC stops and set DCSn.INV=1. Otherwise, it waits for dma request from peripherals to start dma transfer
8. After DMAC completes the current descriptor dma transfer, if DES0.VM=1, it clears DES0.V to 0 and writes back to memory. If DES0.Link=1, it sets DCSn.CT to 1, otherwise it sets DCSn.TT to 1. If the interrupt enabled, it will generates the corresponding interrupts.
9. If DES0.LINK=1, after DMAC completes the current descriptor dma transfer and return to fetch the next descriptor and continues dma transfer until completes the descriptor dma transfer which DES0.LINK=0.

Table 1-4 Descriptor Structure

Word	Bit	Name	Function
1st (DES0)	31	EACKS	External DMA DACKn output polarity select
	30	EACKM	External DMA DACKn output Mode select
	29-28	ERDM	External DMA request detection Mode
	27	EOPM	External DMA End of process mode
	26-24	Reserved	
	23	SAI	Source Address Increment
	22	DAI	Target Address Increment
	21-20	Reserved	
	19-16	RDIL	Request Detection Interval Length
	15-14	SP	Source port width
	13-12	DP	Target port width
	11	Reserved	
	10-8	TSZ	Transfer Data Size
	7	TM	Transfer Mode
	6-5	Reserved	
	4	V	Descriptor Valid
	3	VM	Descriptor Valid Mode
	2	VIE	Descriptor Invalid Interrupt Enable
	1	TIE	Transfer Interrupt Enable
	0	LINK	Descriptor Link Enable
2st (DES1)	31-0	DSA	Source Address
3st (DES2)	31-0	DTA	Target Address
4st (DES3)	31-24	DOA	Descriptor Offset address
	23-0	DTC	Transfer Counter

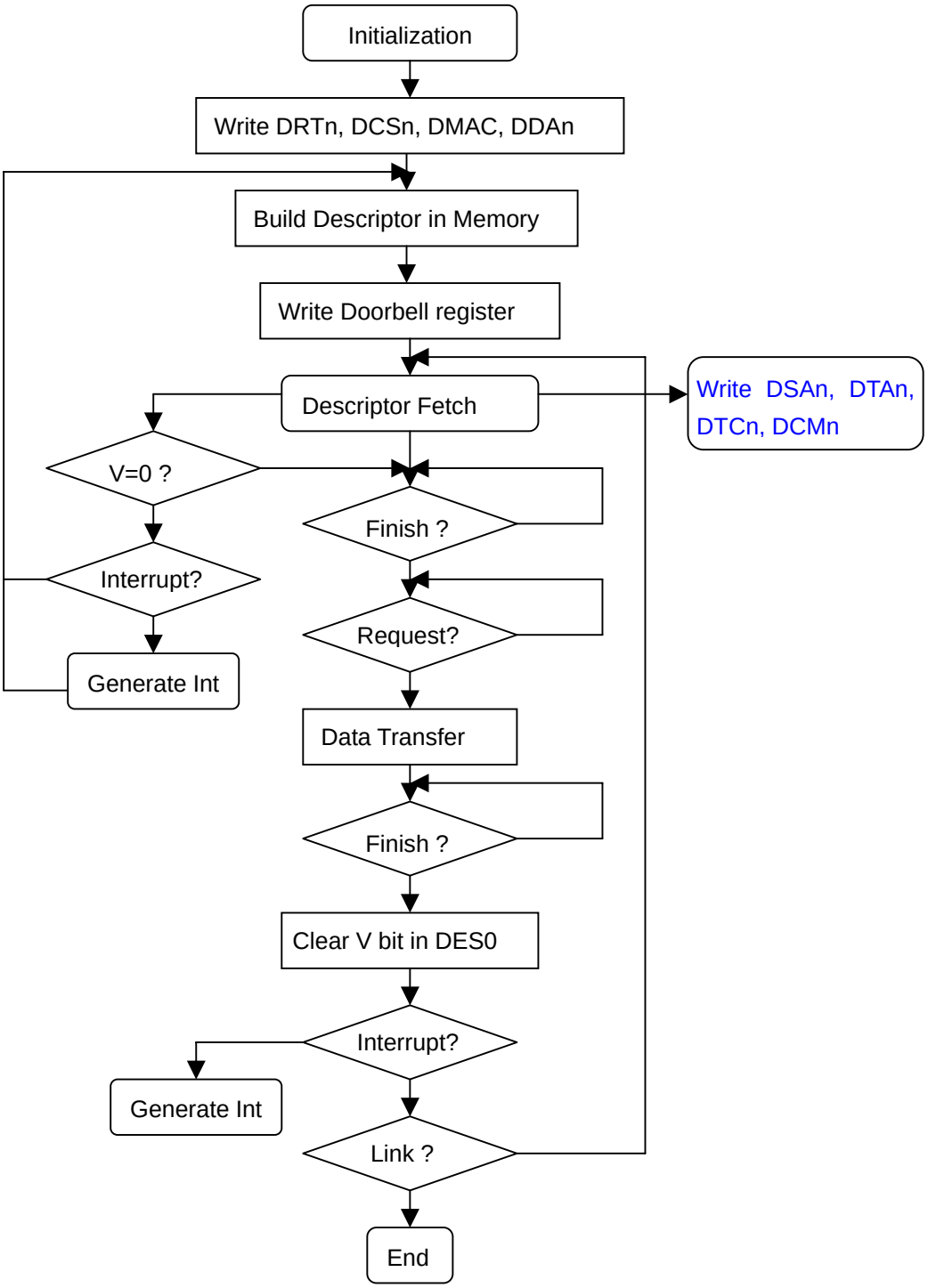


Figure 1-1 Descriptor Transfer Flow

1.3.2 No-Descriptor Transfer

To do proper DMA transfer, do as following steps:

1. First of all, check whether the status of DMA controller are available, that is, for global control (DMAC), ensure that DMAC.AR=0 and DMAC.HLT=0; while for expected channels, ensure that DCSn.AR=0, DCSn.HLT=0 and DCSn.TT=0 and DTCn=0.
2. For each channel n, initialize DSAn, DTAn, DTCn, DRTn, DCSn, DCMn properly
3. Set DMAC.DMAE=1 and expected DCSn.CTE=1 and DCSn.NDES=1 to launch DAM transfer

For a channel with auto-request (DRTn.RT=0x8), the transfer begins automatically when the DCSn.CTE bit and DMAC.DMAE bit are set to 1. While for a channel with other request types, the transfer does not start until a transfer request is issued and detected.

For any channel n, The DTCn value is decremented by 1 for each successful transaction of a data unit. When the specified number of transfer data unit has been completed (DTCn = 0), the transfer ends normally. Meanwhile corresponding bit of DIRQP is set to 1. If DCMn.TIE bit is set to 1, an interrupt request is sent to the CPU. However, during the transfer, if a DMA address error occurs, the transfer is suspended, both DCSn.AR and DMAC.AR are set to 1 as well as corresponding bit of DIRQP. Then an interrupt request is sent to the CPU despite of DCMn.TIE.

Sometimes, for example, an UART parity error occurs for a channel that is transferring data between such UART and another terminal. In the case, both DCSn.HLT and DMAC.HLT are set to 1 and the transfer is suspended. Software should identify halt status by checking such two bits and re-configure DMA to let DMA rerun properly later.

1.4 DMA Requests

DMA transfer requests are normally generated from either the data transfer source or target, but also they can be issued by on-chip peripherals that are neither the source nor the target. There are two DMA transfer request types: auto-request, and on-chip peripheral request. For any channel n, its transfer request type is determined through DRTn.

1.4.1 Auto Request

When there is no explicit transfer request signal available, for example, memory-to-memory transfer or memory to some on-chip peripherals like GPIO, the auto-request mode allows the DMA to automatically generate a transfer request signal internally. Therefore, when DMA initialization done, once the DMAC.DMAE and DCSn.CTE are set to 1, the transfer begins immediately in channel n which DRTn=0x8.

1.4.2 On-Chip Peripheral Request

In the mode, transfer request signals come from on-chip peripherals. All request types except 0x8 (value of DRT) belong to the mode. Both single and block transfer mode are available. Note that in single mode, the transfer byte number for one request detection according to DCMn.RDIL must be equal or less than the byte number according to receive or transmit trigger value of source or target devices.

1.5 DMA Transfer Modes

Each channel can toggles between two transfer modes: single and block

1.5.1 Single Mode

A channel with single mode will periodically detect the request signal according to presetting detection interval length (DCMn.RDIL). Moreover, during the transfer, after a transaction of a data unit (8-bit, 16-bit, 32-bit, 16-byte, or 32-byte), an internal arbitrator in the DMA will arbitrate all active channels again to select one to represent DMA's bus request to participate the AHB bus arbitration. Above process will repeat when the channel captures the bus again until corresponding DCSn.TT bit equals to 1 or abnormal situation (address error, halt) occurs.

1.5.2 Block Mode

Once a channel with block mode captures the bus, it will do data transfer continuously until all data units are transferred or abnormal situation occurs. During the process, it does not release the bus so that neither other channels nor other bus masters can take up the bus. In the mode, the channel just detects the request signal once and corresponding DCMn.RDIL is ignored.

1.6 Channel Priorities

There are two priority modes: fixed, round robin

1.6.1 Fixed Mode

The relative channel priorities are unvaried in the mode.

- CH0 > CH1 > CH2 > CH3 > CH4 > CH5 > CH6 > CH7
- CH0 > CH2 > CH3 > CH1 > CH4 > CH6 > CH7 > CH5
- CH2 > CH0 > CH1 > CH3 > CH6 > CH4 > CH5 > CH7

1.6.2 Round Robin Mode

In the mode, there are two priority groups: CH0~CH3 and CH4~CH7. Round robin is performed in each group, and CH0~CH3 always has higher priority than CH4~CH7.

Table 1-5 Relationship among DMA Transfer connection, Request Mode and Transfer Mode

Transfer Connection	Request Mode	Transfer Mode	Data Size (bits)	Channel
External memory or memory-mapped external device and on-chip peripheral module	Auto on-chip	Block/Single	8/16/32 16-byte/32-byte	0~5

1.7 Examples

1.7.1 Memory-to-memory auto request No-Descriptor Transfer

Suppose you want to do memory move between two different memory regions through channel 3, for example, moving 1KB data from address 0x20001000 to 0x20011000, do as following steps:

a) Check if (DMAC.AR==0 && DMAC.HLT==0 && DCS3.AR==0 && DCS3.HLT==0 && DCS3.CT==0 && DCS3.NDES=1 && DTC3==0)

b) If above condition is true, set value 0 to DCS3.CTE to disable the channel 3 temporarily

c) Set source address 0x20001000 to DSA3 and target address 0x20011000 to DTA3

d) Suppose the data unit is word, set transfer count number 256 (1024/4) to DTC3

e) Set auto-request (0x8) to DRT3

f) Up to now, only the most important channel control register DCM3 is left, set it carefully:

- Set value 1 to SAI and DAI[*1]
- Ignore RDIL because in the case there is no explicit request signal can be detected
- Set word size (0) to SP and DP[*2]
- Set single mode (0) to TM[*3]
- Set value 1 to TIE to let CPU do some post process after the transfer done

g) Set value 1 to DCS3.CTE and DMAC.DMAE to launch the transfer in channels 3

h) When the transfer terminates normally (DTC3==0 && DCS3.TT==1), DIRQP.CIRQ3 will automatically be set value 1 and an interrupt request will be sent to CPU

i) When CPU grants the interrupt request, in the corresponding IRQ handler, software must clear the DCS3.CT to value 0, and the behavior will automatically clear DIRQP.CIRQ3.

NOTES:

1. Either source or target is a FIFO, must not enable corresponding address increment
2. When either source or target need be accessed through EMC (external memory controller), the real port with of the device is encapsulated by EMC, so you can set any favorite port with for it despite of the real one
3. Block mode may block bus for a long time, do not use the mode unless the data are emergency