1 Watchdog Timer

1.1 Overview

The JZ47xx watchdog timer is used to resume the controller operation whenever it is disturbed by malfunctions such as noise and system errors. The watchdog timer can generate the reset signal.

Features:

- Generates WDT reset.
- A 16-bit Data register and a 16-bit counter.
- Counter clock uses the input clock selected by software.
    — PCLK, EXTAL and RTCCLK can be used as the clock for counter
    — The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
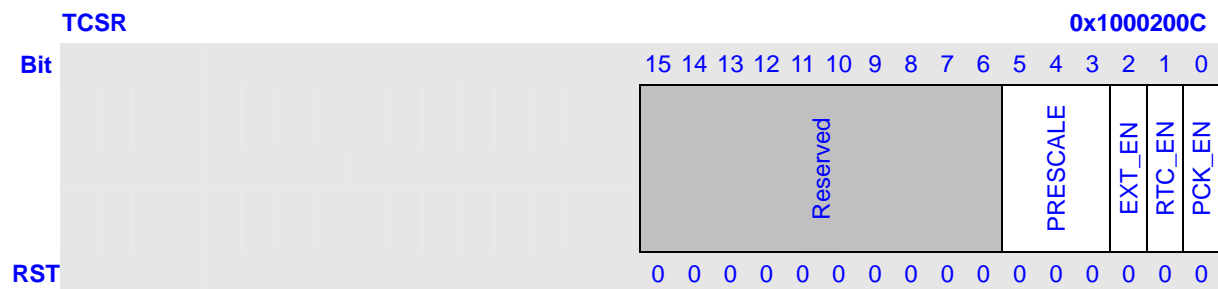
1.2 Register Description

In this section, we will describe the registers in WDT. Following table lists all the registers definition. All WDT register's 32bit address is physical address. And detailed function of each register will be described below.

Name	Description	RW	Reset Value	Address	Access Size
TDR	Watchdog Timer Data Register	RW	0x????	0x10002000	16
TCER	Watchdog Counter Enable Register	RW	0x00	0x10002004	8
TCNT	Watchdog Timer Counter	RW	0x????	0x10002008	16
TCSR	Watchdog Timer Control Register	RW	0x0000	0x1000200C	16

1.2.1 Watchdog Control Register (TCSR)

The TCSR is a 16-bit read/write register. It contains the control bits for WDT. It is initialized to 0x00 by any reset.

TCSR   **0x1000200C**

Bit	15 14 13 12 11 10 9 8 7 6	5 4 3	2	1	0
	Reserved	PRESCALE	EXT_EN	RTC_EN	PCK_EN
RST	0 0 0 0 0 0 0 0 0 0	0 0 0	0	0	0

Bits	Name	Description	RW
15:6	Reserved	These bits always read 0, and written are ignored.	R
5:3	PRESCALE	These bits select the TCNT count clock frequency. | Bit 2	Bit1	Bit 0	Description | |---|---|---|---|
0	0	0	Internal clock: CLK/1
0	0	1	Internal clock: CLK/4
0	1	0	Internal clock: CLK/16
0	1	1	Internal clock: CLK/64
1	0	0	Internal clock: CLK/256
1	0	1	Internal clock: CLK/1024
110~111			Reserved		RW
2	EXT_EN	Select EXTAL as the timer clock input. 1: Enable 0: Disable	RW
1	RTC_EN	Select RTCCLK as the timer clock input.	RW

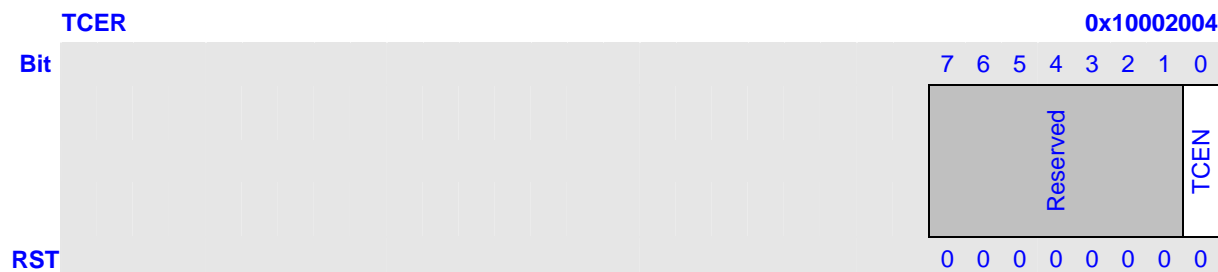|		1: Enable	
		0: Disable	
0	PCK_EN	Select PCLK as the timer clock input.	RW
		1: Enable	
		0: Disable	

Note:

The input clock of timer and the PCLK should keep to the rules as follows:

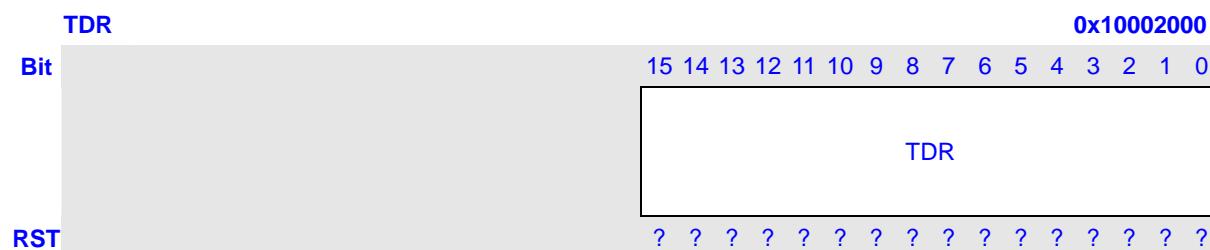| Input clock of timer: IN_CLK	Clock generated from the frequency divider (PRESCALE): DIV_CLK
PCK_EN == 0, RTC_EN == 1 and EXT_EN == 0 (IN_CLK = RTCCLK)	$f_{DIV\_CLK} < \frac{1}{2} f_{PCLK}$
PCK_EN == 0, RTC_EN == 0 and EXT_EN == 1 (IN_CLK = EXTAL)	$f_{DIV\_CLK} < \frac{1}{2} f_{PCLK}$
PCK_EN == 1, RTC_EN == 0 and EXT_EN == 0 (IN_CLK = PCLK)	ANY

1.2.2 Watchdog Enable Register (TCER)

The TCER is an 8-bit read/write register. It contains the counter enable control bits for watchdog. It is initialized to 0x00 by any reset.

| Bits	Name	Description	RW
7:1	Reserved	These bits always read 0, and written are ignored.	R
0	TCEN	Counter enable control. 0: Timer stop. 1: Timer running.	RW

1.2.3 Watchdog Timer Data Register (TDR)

The watchdog timer data register TDR is used to store the data to be compared with the content of the watchdog timer up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

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TDR   **0x10002000**

Bit		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
		TDR
RST		? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ?

1.2.4 Watchdog Timer Counter (TCNT)

The watchdog timer counter (TCNT) is a 16-bit read/write counter. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDR, the comparison match signal will be generated and a WDT reset is generated. The data can be read out at any time. The counter data can be written at any time. (Default: indeterminate)

TCNT   **0x10002008**

Bit		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
		TCNT
RST		? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ?
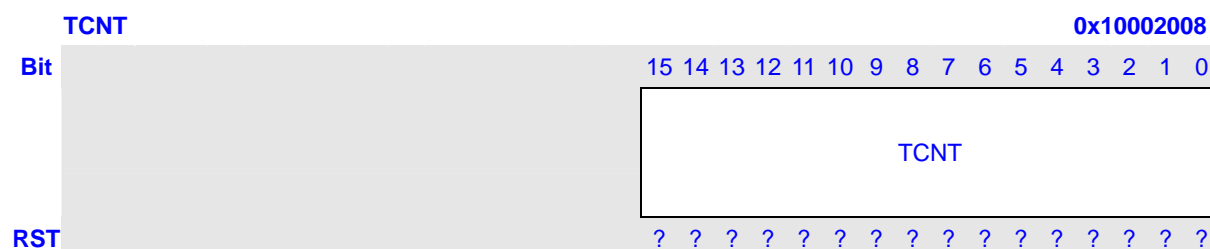
1.3 Watchdog Timer Function

The following describes steps of using WDT:

1. Setting the PRESCALE of input clock in register TCSR.
2. Set register TDR and TCNT.
3. Select the input clock and enable the input clock in register TCSR.

After initialize the register of timer, we should start the counter as follows:

4. Set TCEN bit in TCER to 1. The counter TCNT begins to count.
5. If TCNT = TDR, a WDT reset will be generated.

Note1: The input clock and PCLK should follows the rules advanced before.

Note2: The clock of WDT can be stopped by setting register TSR, and register TSR can only be set by register TSSR or TSCR. The content of register TSR, TSSR and TSCR can be found in TCU spec.