1 General-Purpose I/O Ports

1.1 Overview

The jz4740/jz4720 processor provides 128 multiplexed General Purpose I/O Ports (GPIO) for use in generating and capturing application-specific input and output signals. Each port can be programmed as an output, an input or function port that serves certain peripheral. As input, pull up/down can be enabled/disabled for the port and the port also can be configured as level or edge tripped interrupt source.

Features:

- Each port can be configured as an input, an output or an alternate function port.
- Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering. Every interrupt source can be masked independently.
- Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled.

The 124 GPIO ports, named PA00~31, PB00~31, PC00~31 and PD00~31 in jz471X/jz474X are divided into 4 GPIO groups with maximum of 32 GPIO in each group. Group A includes PA00~PA31. Group B includes PB00~31; Group C includes PC00~PC31 and Group D include PD00~PD31. GPIO output 4 interrupts, 1 for every group, to INTC.

For every group, 23 memory-mapped 32-bit registers can be used to operate the GPIO ports:

- PAPIN, PBPIN, PCPIN, PDPIN - PORT PIN Level Register
- PADAT, PBDAT, PCDAT, PDDAT - PORT Data Register
- PADATS, PBDATS, PCDATS, PDDATS - PORT Data Set Register
- PADATC, PBDATC, PCDATC, PDDATC - PORT Data Clear Register
- PAIM, PBIM, PCIM, PDIM - PORT Interrupt Mask Register
- PAIMS, PBIMS, PCIMS, PDIMS - PORT Interrupt Mask Set Register
- PAIMC, PBIMC, PCIMC, PDIMC - PORT Interrupt Mask Clear Register
- PAPE, PBPE, PCPE, PDPE - PORT PULL Disable Register
- PAPES, PBPES, PCPES, PDPES - PORT PULL Disable Set Register
- PAPEC, PBPEC, PCPEC, PDPEC - PORT PULL Disable Clear Register
- PAFUN, PBFUN, PCFUN, PDFUN - PORT Function Register
- PAFUNS, PBFUNS, PCFUNS, PDFUNS - PORT Function Set Register
- PAFUNC, PBFUNC, PBFUNC, PDFUNC - PORT Function Clear Register
- PASEL, PBSEL, PCSEL, PDSEL - PORT Select Register
- PASELS, PBSELS, PCSELS, PDSELS - PORT Select Set Register
- PASELC, PBSELC, PCSELC, PDSELC - PORT Select Clear Register
- PADIR, PBDIR, PCDIR, PDDIR - PORT Direction Register
- PADIRS, PBDIRS, PCDIRS, PDDIRS - PORT Direction Set Register

- PADIRC, PBDIRC, PCDIRC, PDDIRC - PORT Direction Clear Register
- PATRG, PBTRG, PCTRG, PDTRG - PORT Trigger Mode Register
- PATRGS, PBTRGS, PCTRGS, PDTRGS - PORT Trigger Mode Set Register
- PATRGC, PBTRGC, PCTRGC, PDTRGC - PORT Trigger Mode Clear Register
- PAFLG, PBFLG, PCFLG, PDFLG - PORT FLAG Register

Table 1-1 ~ Table 1-4 summarized pull resistor direction and shared function ports for all GPIO.

Table 1-1 GPIO Port A summary

Bit N	PA N	Pull (U/D)	Shared Function Port Selected by			
			Test Mode	PFUN = 1 & PSEL = 0	PFUN = 1 & PSEL = 1	Note
0	00	U	-	D [0] (io)	-	-
1	01	U	-	D [1] (io)	-	-
2	02	U	-	D [2] (io)	-	-
3	03	U	-	D [3] (io)	-	-
4	04	U	-	D [4] (io)	-	-
5	05	U	-	D [5] (io)	-	-
6	06	U	-	D [6] (io)	-	-
7	07	U	-	D [7] (io)	-	-
8	08	U	-	D [8] (io)	-	-
9	09	U	-	D [9] (io)	-	-
10	10	U	-	D [10] (io)	-	-
11	11	U	-	D [11] (io)	-	-
12	12	U	-	D [12] (io)	-	-
13	13	U	-	D [13] (io)	-	-
14	14	U	-	D [14] (io)	-	-
15	15	U	-	D [15] (io)	-	-
16	16	U	-	D [16] (io)	-	-
17	17	U	-	D [17] (io)	-	-
18	18	U	-	D [18] (io)	-	-
19	19	U	-	D [19] (io)	-	-
20	20	U	-	D [20] (io)	-	-
21	21	U	-	D [21] (io)	-	-
22	22	U	-	D [22] (io)	-	-
23	23	U	-	D [23] (io)	-	-
24	24	U	-	D [24] (io)	-	-
25	25	U	-	D [25] (io)	-	-
26	26	U	-	D [26] (io)	-	-
27	27	U	-	D [27] (io)	-	-
28	28	U	-	D [28] (io)	-	-
29	29	U	-	D [29] (io)	-	-
30	30	U	-	D [30] (io)	-	-
31	31	U	-	D [31] (io)	-	-

Table 1-2 GPIO Port B summary

Bit N	PB N	Pull (U/D)	Shared Function Port Selected by			
			Test Mode	PFUN = 1 & PSEL = 0	PFUN = 1 & PSEL = 1	Note
0	00	U	-	A [0] (out)	-	-
1	01	U	-	A [1] (out)	-	-
2	02	U	-	A [2] (out)	-	-
3	03	U	-	A [3] (out)	-	-
4	04	U	-	A [4] (out)	-	-
5	05	U	-	A [5] (out)	-	-
6	06	U	-	A [6] (out)	-	-
7	07	U	-	A [7] (out)	-	-
8	08	U	-	A [8] (out)	-	-
9	09	U	-	A [9] (out)	-	-
10	10	U	-	A [10] (out)	-	-
11	11	U	-	A [11] (out)	-	-
12	12	U	-	A [12] (out)	-	-
13	13	U	-	A [13] (out)	-	-
14	14	U	-	A [14] (out)	-	-
15	15	U	-	A [15] (out)	-	-
16	16	U	-	A [16] (out)	-	-
17	17	U	-	CLS (out)	A [21] (out)	
18	18	U	-	SPL (out)	A [22] (out)	
19	19	U	-	DCS_ (out)	-	-
20	20	U	-	RAS_ (out)	-	-
21	21	U	-	CAS_ (out)	-	-
22	22	U	-	SDWE_ & BUFD_ (out)	-	-
23	23	U	-	CKE (out)	-	-
24	24	U	-	CKO (out)	-	-
25	25	U	-	CS1_ (out)	-	-
26	26	U	-	CS2_ (out)	-	-
27	27	U	SCO16 (out)	CS3_ (out)	-	-
28	28	U	SCO17 (out)	CS4_ (out)	-	-
29	29	U	-	RD_ (out)	-	-
30	30	U	-	WR_ (out)	-	-
31	31	U	-	WE0_ (out)	-	-

Table 1-3 GPIO Port C summary

Bit N	PC N	Pull (U/D)	Shared Function Port Selected by			
			Test Mode	PFUN = 1 & PSEL = 0	PFUN = 1 & PSEL = 1	Note
0	00	U	SCO0 (out)	LCD_D [0] (out)	-	-
1	01	U	SCO1 (out)	LCD_D [1] (out)	-	-
2	02	U	SCO2 (out)	LCD_D [2] (out)	-	-
3	03	U	SCO3 (out)	LCD_D [3] (out)	-	-
4	04	U	SCO4 (out)	LCD_D [4] (out)	-	-
5	05	U	SCO5 (out)	LCD_D [5] (out)	-	-
6	06	U	SCO6 (out)	LCD_D [6] (out)	-	-
7	07	U	SCO7 (out)	LCD_D [7] (out)	-	-
8	08	U	SCO8 (out)	LCD_D [8] (out)	-	-
9	09	U	SCO9 (out)	LCD_D [9] (out)	-	-
10	10	U	SCO10 (out)	LCD_D [10] (out)	-	-
11	11	U	SCO11 (out)	LCD_D [11] (out)	-	-
12	12	U	SCO12 (out)	LCD_D [12] (out)	-	-
13	13	U	SCO13 (out)	LCD_D [13] (out)	-	-
14	14	U	SCO14 (out)	LCD_D [14] (out)	-	-
15	15	U	SCO15 (out)	LCD_D [15] (out)	-	-
16	16	U	-	LCD_D [16] (out)	-	-
17	17	U	-	LCD_D [17] (out)	-	-
18	18	U	SCO18 (out)	LCD_PCLK (io)	-	-
19	19	U	SCO19 (out)	LCD_HSYNC (io)	-	-
20	20	U	-	LCD_VSYNC (io)	-	-
21	21	U	-	LCD_DE (out)	-	-
22	22	U	-	LCD_PS (out)	A [19] (out)	-
23	23	U	-	LCD_REV (out)	A [20] (out)	-
24	24	U	-	WE1_ (out)	-	-
25	25	U	-	WE2_ (out)	-	-
26	26	U	-	WE3_ (out)	-	-
27	27	U	SCI04 (in)	WAIT_ (in)	-	-
28	28	U	-	FRE_ (out)	-	-
29	29	U	-	FWE_ (out)	-	-
30	30	U	-	-	-	Note1
31	31	U	-		-	Note2

Note[*1]:

PC30: GPIO group C bit 30. If NAND flash is used, it should connect to NAND FRB. (NAND flash ready/busy) If NAND flash is not used, it is used as general GPIO.

Note[*2]:

PC31 is not a chip pin. It is only used to select the function of UART or JTAG set by register PCSEL [31], the other registers is not used.

PCSEL [31]=0: Select JTAG Function
PCSEL [31]=1: Select UART Function

Table 1-4 GPIO Port D summary

Bit N	PD N	Pull (U/D)	Shared Function Port Selected by				
			Test Mode	PFUN = 1 & PSEL = 0 & PTRG = 0	PFUN = 1 & PSEL = 1 & PTRG = 0	PFUN = 1 & PSEL = 0 & PTRG = 1	Note
0	00	U	-	CIM_D0 (in)	-		Note3
1	01	U	-	CIM_D1 (in)	-		Note4
2	02	U	-	CIM_D2 (in)	-		Note5
3	03	U	-	CIM_D3 (in)	-		Note6
4	04	U	-	CIM_D4 (in)	-		Note7
5	05	U	-	CIM_D5 (in)	-		Note8
6	06	U	-	CIM_D6 (in)	-		Note9
7	07	U	-	CIM_D7 (in)	-		Note10
8	08	U	CDC_TSE	MSC_CMD (io)	-		-
9	09	U	CDC_TERST	MSC_CLK (out)	-		-
10	10	U	SCI00 (in)	MSC_D0 (io)	-		-
11	11	U	SCI01 (in)	MSC_D1 (io)	-		-
12	12	U	SCI02 (in)	MSC_D2 (io)	-		-
13	13	U	SCI03 (in)	MSC_D3 (io)	-		-
14	14	U	-	CIM_MCLK (out)	-		Note11
15	15	U	-	CIM_PCLK (in)	-		-
16	16	U	-	CIM_VSYN (in)	-		-
17	17	U	-	CIM_HSYN (in)	-		-
18	18	U	SCI08 (in)	SSI_CLK (out)	SCLK_RSTN (out)		-
19	19	U	SCI09 (in)	SSI_CE0_ (out)	BCLK (io)		-
20	20	U	SCI10 (in)	SSI_DT (out)	SDATO (out)		-
21	21	U	SCI11 (in)	SSI_DR (in)	SDATI (in)		-
22	22	U	SCI12 (in)	SSI_CE1_ & SSI_GPC (out)	SYNC (io)		-
23	23	U	SCI13 (in)	PWM0 (out)	I2C_SDA (io)		-
24	24	U	SCI14 (in)	PWM1 (out)	I2C_SCK (io)		-
25	25	U	SCI15 (in)	PWM2 (out)	UART0_TXD (out)		-
26	26	U	SCI16 (in)	PWM3 (out)	UART0_RXD (in)		-
27	27	U	SCI17 (in)	PWM4 (out)	A [17] (out)		
28	28	U	SCI18 (in)	PWM5 (out)	A [18] (out)		Note12
29	29	-	-	-	-		Note13
30	30	U	-	PWM6 (out)	UART0_CTS_ (in)	UART1_RXD (in)	-
31	31	U	-	PWM7 (out)	UART0_RTS_ (out)	UART1_TXD (out)	-

Note[*3]~Note[*13]

In CPM SPEC you can find register SCR, and the bit TPE_ADC and TPE_CDC will be used for test SADC and CODEC modules.

	PORT	SCR.TPE_ADC = 1	SCR.TPE_CDC = 1	OTHERS
Note3	PD00	TPI0_C [0] (input)	-	-
Note4	PD01	TPI1_C [1] (input)	-	-
Note5	PD02	TPI2_C [2] (input)	-	-
Note6	PD03	TPI3_C [3] (input)	-	-
Note7	PD04	TPI4_CKIN (input)	TPI4_MCLK (input)	-
Note8	PD05	TPI5_RST (input)	TPI5_BITCLK (input)	-
Note9	PD06	TPI6_PD (input)	TPI6_LRCLK (input)	-
Note10	PD07	TPI7_STDA (input)	TPI7_DA (input)	-
Note11	PD14	TPI0_CK (output)	TPI0_AD (output)	-
Note12	PD28	TPO1_PEN (output)	-	-
Note13	PD29	-	-	WAKEUP (AI) / PORM (AI)

Note[*11]:

PD14 is output 0 during the reset (PPRST_, WDT-reset and hibernating-reset) period.

Note[*13]:

PD29 is only used as input and interrupt only, and with no pull-up and pull-down.

Note:
The direction of GPD16 is controlled by PDDIR[15] when GPD16 is used as GPIO function, and PDDIR[16] is no useful. That is PDDIR[15] can control the direction of GPD15 and GPD16 at the same time.

1.2 Register Description

Table 1-2 summarized all memory-mapped registers, which can be programmed to operate GPIO port and alternate function port sharing configuration.

All registers are in 32-bits width. Usually, 1 bit in the register affects a corresponding GPIO port and every GPIO port can be operated independently.

Table 1-2 GPIO Registers

Name	Description	RW	Reset Value	Address	Size
GPIO PORT A					
PAPIN	PORT A PIN Level Register	R	0x00000000	0x10010000	32
PADAT	PORT A Data Register	R	0x00000000	0x10010010	32
PADATS	PORT A Data Set Register	W	0x????????	0x10010014	32
PADATC	PORT A Data Clear Register	W	0x????????	0x10010018	32
PAIM	PORT A Interrupt Mask Register	R	0xFFFFFFFF	0x10010020	32
PAIMS	PORT A Interrupt Mask Set Register	W	0x????????	0x10010024	32
PAIMC	PORT A Interrupt Mask Clear Register	W	0x????????	0x10010028	32
PAPE	PORT A PULL Disable Register	R	0x00000000	0x10010030	32
PAPES	PORT A PULL Disable Set Register	W	0x????????	0x10010034	32
PAPEC	PORT A PULL Disable Clear Register	W	0x????????	0x10010038	32
PAFUN	PORT A Function Register	R	0x00000000	0x10010040	32
PAFUNS	PORT A Function Set Register	W	0x????????	0x10010044	32
PAFUNC	PORT A Function Clear Register	W	0x????????	0x10010048	32
PASEL	PORT A Select Register	R	0x00000000	0x10010050	32
PASELS	PORT A Select Set Register	W	0x????????	0x10010054	32
PASELC	PORT A Select Clear Register	W	0x????????	0x10010058	32
PADIR	PORT A Direction Register	R	0x00000000	0x10010060	32
PADIRS	PORT A Direction Set Register	W	0x????????	0x10010064	32
PADIRC	PORT A Direction Clear Register	W	0x????????	0x10010068	32
PATRG	PORT A Trigger Register	R	0x00000000	0x10010070	32
PATRGS	PORT A Trigger Set Register	W	0x????????	0x10010074	32
PATRGC	PORT A Trigger Clear Register	W	0x????????	0x10010078	32
PAFLG	PORT A FLAG Register	R	0x00000000	0x10010080	32
PAFLGC	PORT A FLAG Clear Register	W	0x????????	0x10010014	32
GPIO PORT B					
PBPIN	PORT B PIN Level Register	R	0x00000000	0x10010100	32
PBDAT	PORT B Data Register	R	0x00000000	0x10010110	32
PBDATS	PORT B Data Set Register	W	0x????????	0x10010114	32
PBDATC	PORT B Data Clear Register	W	0x????????	0x10010118	32
PBIM	PORT B Interrupt Mask Register	R	0xFFFFFFFF	0x10010120	32

PBIMS	PORT B Interrupt Mask Set Register	W	0x????????	0x10010124	32
PBIMC	PORT B Interrupt Mask Clear Register	W	0x????????	0x10010128	32
PBPE	PORT B PULL Enable Register	R	0x00000000	0x10010130	32
PBPES	PORT B PULL Enable Set Register	W	0x????????	0x10010134	32
PBPEC	PORT B PULL Enable Clear Register	W	0x????????	0x10010138	32
PBFUN	PORT B Function Register	R	0x00000000	0x10010140	32
PBFUNS	PORT B Function Set Register	W	0x????????	0x10010144	32
PBFUNC	PORT B Function Clear Register	W	0x????????	0x10010148	32
PBSEL	PORT B Select Register	R	0x00000000	0x10010150	32
PBSELS	PORT B Select Set Register	W	0x????????	0x10010154	32
PBSELC	PORT B Select Clear Register	W	0x????????	0x10010158	32
PBDIR	PORT B Direction Register	R	0x00000000	0x10010160	32
PBDIRS	PORT B Direction Set Register	W	0x????????	0x10010164	32
PBDIRC	PORT B Direction Clear Register	W	0x????????	0x10010168	32
PBTRG	PORT B Trigger Register	R	0x00000000	0x10010170	32
PBTRGS	PORT B Trigger Set Register	W	0x????????	0x10010174	32
PBTRGC	PORT B Trigger Clear Register	W	0x????????	0x10010178	32
PBFLG	PORT B FLAG Register	R	0x00000000	0x10010180	32
PBFLGC	PORT B FLAG Clear Register	W	0x????????	0x10010114	32
GPIO PORT C					
PCPIN	PORT C PIN Level Register	R	0x00000000	0x10010200	32
PCDAT	PORT C Data Register	R	0x00000000	0x10010210	32
PCDATS	PORT C Data Set Register	W	0x????????	0x10010214	32
PCDATC	PORT C Data Clear Register	W	0x????????	0x10010218	32
PCIM	PORT C Interrupt Mask Register	R	0xFFFFFFFF	0x10010220	32
PCIMS	PORT C Interrupt Mask Set Register	W	0x????????	0x10010224	32
PCIMC	PORT C Interrupt Mask Clear Register	W	0x????????	0x10010228	32
PCPE	PORT C PULL Enable Register	R	0x00000000	0x10010230	32
PCPES	PORT C PULL Enable Set Register	W	0x????????	0x10010234	32
PCPEC	PORT C PULL Enable Clear Register	W	0x????????	0x10010238	32
PCFUN	PORT C Function Register	R	0x00000000	0x10010240	32
PCFUNS	PORT C Function Set Register	W	0x????????	0x10010244	32
PCFUNC	PORT C Function Clear Register	W	0x????????	0x10010248	32
PCSEL	PORT C Select Register	R	0x00000000	0x10010250	32
PCSELS	PORT C Select Set Register	W	0x????????	0x10010254	32
PCSELC	PORT C Select Clear Register	W	0x????????	0x10010258	32
PCDIR	PORT C Direction Register	R	0x00000000	0x10010260	32
PCDIRS	PORT C Direction Set Register	W	0x????????	0x10010264	32
PCDIRC	PORT C Direction Clear Register	W	0x????????	0x10010268	32
PCTRG	PORT C Trigger Register	R	0x00000000	0x10010270	32

PCTRGS	PORT C Trigger Set Register	W	0x????????	0x10010274	32
PCTRGC	PORT C Trigger Clear Register	W	0x????????	0x10010278	32
PCFLG	PORT C FLAG Register	R	0x00000000	0x10010280	32
PCFLGC	PORT C FLAG Clear Register	W	0x????????	0x10010214	32
GPIO PORT D					
PDPIN	PORT D PIN Level Register	R	0x00000000	0x10010300	32
PDDAT	PORT D Data Register	R	0x00000000	0x10010310	32
PDDATS	PORT D Data Set Register	W	0x????????	0x10010314	32
PDDATC	PORT D Data Clear Register	W	0x????????	0x10010318	32
PDIM	PORT D Interrupt Mask Register	R	0xFFFFFFFF	0x10010320	32
PDIMS	PORT D Interrupt Mask Set Register	W	0x????????	0x10010324	32
PDIMC	PORT D Interrupt Mask Clear Register	W	0x????????	0x10010328	32
PDPE	PORT D PULL Enable Register	R	0x00000000	0x10010330	32
PDPES	PORT D PULL Enable Set Register	W	0x????????	0x10010334	32
PDPEC	PORT D PULL Enable Clear Register	W	0x????????	0x10010338	32
PDFUN	PORT D Function Register	R	0x00000000	0x10010340	32
PDFUNS	PORT D Function Set Register	W	0x????????	0x10010344	32
PDFUNC	PORT D Function Clear Register	W	0x????????	0x10010348	32
PDSEL	PORT D Select Register	R	0x00000000	0x10010350	32
PDSELS	PORT D Select Set Register	W	0x????????	0x10010354	32
PDSELC	PORT D Select Clear Register	W	0x????????	0x10010358	32
P\DDIR	PORT D Direction Register	R	0x00000000	0x10010360	32
PDDIRS	PORT D Direction Set Register	W	0x????????	0x10010364	32
PDDIRC	PORT D Direction Clear Register	W	0x????????	0x10010368	32
PDTRG	PORT D Trigger Register	R	0x00000000	0x10010370	32
PDTRGS	PORT D Trigger Set Register	W	0x????????	0x10010374	32
PDTRGC	PORT D Trigger Clear Register	W	0x????????	0x10010378	32
PDFLG	PORT D FLAG Register	R	0x00000000	0x10010380	32
PDFLGC	PORT D FLAG Clear Register	W	0x????????	0x10010314	32

Note: PX**** in the description of register as follows means PA****, PB****, PC**** and PD****.

1.2.1 PORT PIN Level Register (PAPIN, PBPIN, PCPIN, PDPIN)

PAPIN, PBPIN, PCPIN and PDPIN are four 32-bit PORT PIN level registers. They are read-only registers.

PAPIN, PBPIN, PCPIN, PDPIN **0x10010000, 0x10010100, 0x10010200, 0x10010300**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PINL31	PINL30	PINL29	PINL28	PINL27	PINL26	PINL25	PINL24	PINL23	PINL22	PINL21	PINL20	PINL19	PINL18	PINL17	PINL16	PINL15	PINL14	PINL13	PINL12	PINL11	PINL10	PINL09	PINL08	PINL07	PINL06	PINL05	PINL04	PINL03	PINL02	PINL01	PINL00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
n	PINL n	Where n = 0 ~ 31 and PINL n = PINL0 ~ PINL31. The PORT PIN level can be read by reading PINL n bit in register PXPIN.	R

PAPIN bits 31-0 correspond to PA31-0; PBPIN to PB31-0; PCPIN to PC31-0 and PDPIN to PD 31-0.

1.2.2 PORT Data Register (PADAT, PBDAT, PCDAT, PDDAT)

PADAT, PBDAT, PCDAT and PDDAT are four 32-bit PORT DATA registers. They are read-only registers.

PADAT, PBDAT, PCDAT, PDDAT **0x10010010, 0x10010110, 0x10010210, 0x10010310**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA31	DATA30	DATA29	DATA28	DATA27	DATA26	DATA25	DATA24	DATA23	DATA22	DATA21	DATA20	DATA19	DATA18	DATA17	DATA16	DATA15	DATA14	DATA13	DATA12	DATA11	DATA10	DATA09	DATA08	DATA07	DATA06	DATA05	DATA04	DATA03	DATA02	DATA01	DATA00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
n	DATA n	Where n = 0 ~ 31 and DATA n = DATA0 ~ DATA31. The register is used as GPIO data register. When GPIO is used as interrupt the register is no used.	R

PADAT bits 31-0 correspond to PA31-0; PBDAT to PB31-0; PCDAT to PC31-0 and PDDAT to PD 31-0.

1.2.3 PORT Data Set Register (PADATS, PBDATS, PCDATS, PDDATS)

PADATS, PBDATS, PCDATS and PDDATA are four 32-bit PORT DATA set registers. They are write-only registers.

PADATS, PBDATS, PCDATS, PDDATS **0x10010014, 0x10010114, 0x10010214, 0x10010314**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATAS31	DATAS30	DATAS29	DATAS28	DATAS27	DATAS26	DATAS25	DATAS24	DATAS23	DATAS22	DATAS21	DATAS20	DATAS19	DATAS18	DATAS17	DATAS16	DATAS15	DATAS14	DATAS13	DATAS12	DATAS11	DATAS10	DATAS09	DATAS08	DATAS07	DATAS06	DATAS05	DATAS04	DATAS03	DATAS02	DATAS01	DATAS00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	DATAS n	Writing 1 to DATAS n will set DATA n to 1 in register PXDAT. Writing 0 to DATAS n will no use.	W

PADATS bits 31-0 correspond to PA31-0; PBDATS to PB31-0; PCDATS to PC31-0 and PDDATS to PD 31-0.

1.2.4 PORT Data Clear Register (PADATC, PBDATC, PCDATC, PDDATC)

PADATC, PBDATC, PCDATC and PDDATC are four 32-bit PORT DATA clear registers. They are write-only registers.

PADATC, PBDATC, PCDATC, PDDATC **0x10010018, 0x10010118, 0x10010218, 0x10010318**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATAC31	DATAC30	DATAC29	DATAC28	DATAC27	DATAC26	DATAC25	DATAC24	DATAC23	DATAC22	DATAC21	DATAC20	DATAC19	DATAC18	DATAC17	DATAC16	DATAC15	DATAC14	DATAC13	DATAC12	DATAC11	DATAC10	DATAC09	DATAC08	DATAC07	DATAC06	DATAC05	DATAC04	DATAC03	DATAC02	DATAC01	DATAC00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	DATAC n	Writing 1 to DATAC n will set DATA n to 0 in register PXDAT. Writing 0 to DATAC n will no use.	W

PADATC bits 31-0 correspond to PA31-0; PBDATC to PB31-0; PCDATC to PC31-0 and PDDATC to PD 31-0.

1.2.5 PORT Mask Register (PAIM, PBIM, PCIM, PDIM)

PAIM, PBIM, PCIM and PDIM are four 32-bit PORT MASK registers. They are read-only registers.

PAIM, PBIM, PCIM, PDIM **0x10010020, 0x10010120, 0x10010220, 0x10010320**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MASK31	MASK30	MASK29	MASK28	MASK27	MASK26	MASK25	MASK24	MASK23	MASK22	MASK21	MASK20	MASK19	MASK18	MASK17	MASK16	MASK15	MASK14	MASK13	MASK12	MASK11	MASK10	MASK09	MASK08	MASK07	MASK06	MASK05	MASK04	MASK03	MASK02	MASK01	MASK00
RST	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	R/W
n	MASK n	Where n = 0 ~ 31 and MASK n = MASK0 ~ MASK31. MASK n is used for mask the interrupt of GPIO n. 0: Enable the pin as an interrupt source. 1: Disable the pin as an interrupt source.	R

PAIM bits 31-0 correspond to PA31-0; PBIM to PB31-0; PCIM to PC31-0 and PDIM to PD 31-0.

1.2.6 PORT Mask Set Register (PAIMS, PBIMS, PCIMS, PDIMS)

PAIMS, PBIMS, PCIMS and PIMS are four 32-bit PORT MASK set registers. They are write-only registers.

PAIMS, PBIMS, PCIMS, PDIMS **0x10010024, 0x10010124, 0x10010224, 0x10010324**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MASKS31	MASKS30	MASKS29	MASKS28	MASKS27	MASKS26	MASKS25	MASKS24	MASKS23	MASKS22	MASKS21	MASKS20	MASKS19	MASKS18	MASKS17	MASKS16	MASKS15	MASKS14	MASKS13	MASKS12	MASKS11	MASKS10	MASKS09	MASKS08	MASKS07	MASKS06	MASKS05	MASKS04	MASKS03	MASKS02	MASKS01	MASKS00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	MASKS n	Writing 1 to MASKS n will set MASK n to 1 in register PXIM. Writing 0 to MASKS n will no use.	W

PAIMS bits 31-0 correspond to PA31-0; PBIMS to PB31-0; PCIMS to PC31-0 and PDIMS to PD 31-0.

1.2.7 PORT Mask Clear Register (PAIMC, GBPIMC, PCIMC, PDIMC)

PAIMC, PBIMC, PCIMC and PDIMC are four 32-bit PORT MASK clear registers. They are write-only registers.

PAIMS, PBIMC, PCIMC, PDIMC **0x10010028, 0x10010128, 0x10010228, 0x10010328**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MASKC31	MASKC30	MASKC29	MASKC28	MASKC27	MASKC26	MASKC25	MASKC24	MASKC23	MASKC22	MASKC21	MASKC20	MASKC19	MASKC18	MASKC17	MASKC16	MASKC15	MASKC14	MASKC13	MASKC12	MASKC11	MASKC10	MASKC09	MASKC08	MASKC07	MASKC06	MASKC05	MASKC04	MASKC03	MASKC02	MASKC01	MASKC00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	MASKC n	Writing 1 to MASKC n will set MASK n to 0 in register PXIM. Writing 0 to MASKC n will no use.	W

PAIMC bits 31-0 correspond to PA31-0; PBIMC to PB31-0; PCIMC to PC31-0 and PDIMC to PD 31-0.

1.2.8 PORT PULL Disable Register (PAPE, PBPE, PCPE, PDPE)

PAPE, PBPE, PCPE and PDPE are four 32-bit PORT PULL disable registers. They are read-only registers.

PAPE, PBPE, PCPE, PDPE **0x10010030, 0x10010130, 0x10010230, 0x10010330**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PULL31	PULL30	PULL29	PULL28	PULL27	PULL26	PULL25	PULL24	PULL23	PULL22	PULL21	PULL20	PULL19	PULL18	PULL17	PULL16	PULL15	PULL14	PULL13	PULL12	PULL11	PULL10	PULL09	PULL08	PULL07	PULL06	PULL05	PULL04	PULL03	PULL02	PULL01	PULL00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
n	PULL n	Where n = 0 ~ 31 and PULL n = PULL0 ~ PULL31. PULL n is used for setting the port to be PULL UP or PULL DOWN enable. 1: No pull up or pull down resistor connects to the port. 0: An internal pull up or pull down resistor connects to the port. Up or down is pin dependence. Please reference to Table 1-1 ~ Table 1-4 for it.	R

PAPE bits 31-0 correspond to PA31-0; PBPE to PB31-0; PCPE to PC31-0 and PDPE to PD 31-0.

1.2.9 PORT PULL Set Register (PAPES, PBPES, PCPES, PDPES)

PAPES, PBPES, PCPES and PDPES are four 32-bit PORT PULL set registers. They are write-only registers.

PAPES, PBPES, PCPES, PDPES **0x10010034, 0x10010134, 0x10010234, 0x10010334**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PULLS31	PULLS30	PULLS29	PULLS28	PULLS27	PULLS26	PULLS25	PULLS24	PULLS23	PULLS22	PULLS21	PULLS20	PULLS19	PULLS18	PULLS17	PULLS16	PULLS15	PULLS14	PULLS13	PULLS12	PULLS11	PULLS10	PULLS09	PULLS08	PULLS07	PULLS06	PULLS05	PULLS04	PULLS03	PULLS02	PULLS01	PULLS00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	PULLS n	Writing 1 to PULLS n will set PULL n to 1 in register PXPE. Writing 0 to PULLS n will no use.	W

PAPES bits 31-0 correspond to PA31-0; PBPES to PB31-0; PCPES to PC31-0 and PDPES to PD 31-0.

1.2.10 PORT PULL Clear Register (PAPEC, PBPEC, PCPEC, PDPEC)

PAPEC, PBPEC, PCPEC and PDPEC are four 32-bit PORT PULL clear registers. They are write-only registers.

PAPES, PBPEC, PCPEC, PDPEC **0x10010038, 0x10010138, 0x10010238, 0x10010338**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PULLC31	PULLC30	PULLC29	PULLC28	PULLC27	PULLC26	PULLC25	PULLC24	PULLC23	PULLC22	PULLC21	PULLC20	PULLC19	PULLC18	PULLC17	PULLC16	PULLC15	PULLC14	PULLC13	PULLC12	PULLC11	PULLC10	PULLC09	PULLC08	PULLC07	PULLC06	PULLC05	PULLC04	PULLC03	PULLC02	PULLC01	PULLC00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	PULLC n	Writing 1 to PULLC n will set PULL n to 0 in register PXPE. Writing 0 to PULLC n will no use.	W

PAPEC bits 31-0 correspond to PA31-0; PBPEC to PB31-0; PCPEC to PC31-0 and PDPEC to PD 31-0.

1.2.11 PORT Function Register (PAFUN, PBFUN, PCFUN, PDFUN)

PAFUN, PBFUN, PCFUN and PDFUN are four 32-bit PORT function registers. They are read-only registers.

PAFUN, PBFUN, PCFUN, PDFUN **0x10010040, 0x10010140, 0x10010240, 0x10010340**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FUN31	FUN30	FUN29	FUN28	FUN27	FUN26	FUN25	FUN24	FUN23	FUN22	FUN21	FUN20	FUN19	FUN18	FUN17	FUN16	FUN15	FUN14	FUN13	FUN12	FUN11	FUN10	FUN09	FUN08	FUN07	FUN06	FUN05	FUN04	FUN03	FUN02	FUN01	FUN00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
n	FUN n	Where n = 0 ~ 31 and FUN n = FUN0 ~ FUN31 In most cases, port is shared with one or more peripheral functions. FUN n controls the owner of the port n. 0: GPIO or Interrupt 1: Alternate Function (Function 0 *1 or Function 1*1) Note: 1. Please reference to Table 1-1 ~ Table 1-4 for the details.	R

PAFUN bits 31-0 correspond to PA31-0; PBFUN to PB31-0; PCFUN to PC31-0 and PDFUN to PD 31-0.

1.2.12 PORT Function Set Register (PAFUNS, PBFUNS, PCFUNS, PDFUNS)

PAFUNS, PBFUNS, PCFUNS and PDFUNS are four 32-bit PORT function set registers. They are write-only registers.

PAFUNS, PBFUNS, PCFUNS, PDFUNS **0x10010044, 0x10010144, 0x10010244, 0x10010344**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FUNS31	FUNS30	FUNS29	FUNS28	FUNS27	FUNS26	FUNS25	FUNS24	FUNS23	FUNS22	FUNS21	FUNS20	FUNS19	FUNS18	FUNS17	FUNS16	FUNS15	FUNS14	FUNS13	FUNS12	FUNS11	FUNS10	FUNS09	FUNS08	FUNS07	FUNS06	FUNS05	FUNS04	FUNS03	FUNS02	FUNS01	FUNS00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	FUNS n	Writing 1 to FUNS n will set FUN n to 1 in register PXFUN. Writing 0 to FUNS n will no use.	W

PAFUNS bits 31-0 correspond to PA31-0; PBFUNS to PB31-0; PCFUNS to PC31-0 and PDFUNS to PD 31-0.

1.2.13 PORT Function Clear Register (PAFUNC, PBFUNC, PCFUNC, PDFUNC)

PAFUNC, PBFUNC, PCFUNC and PDFUNC are four 32-bit PORT function clear registers. They are write-only registers.

PAFUNC, PBFUNC, PCFUNC, PDFUNC **0x10010048, 0x10010148, 0x10010248, 0x10010348**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FUNC31	FUNC30	FUNC29	FUNC28	FUNC27	FUNC26	FUNC25	FUNC24	FUNC23	FUNC22	FUNC21	FUNC20	FUNC19	FUNC18	FUNC17	FUNC16	FUNC15	FUNC14	FUNC13	FUNC12	FUNC11	FUNC10	FUNC09	FUNC08	FUNC07	FUNC06	FUNC05	FUNC04	FUNC03	FUNC02	FUNC01	FUNC00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	FUNC n	Writing 1 to FUNC n will set FUN n to 0 in register PXFUN. Writing 0 to FUNC n will no use.	W

PAFUNC bits 31-0 correspond to PA31-0; PBFUNC to PB31-0; PCFUNC to PC31-0 and PDFUNC to PD 31-0.

1.2.14 PORT Select Register (PASEL, PBSEL, PCFSEL, PDSEL)

PASEL, PBSEL, PCSEL and PDSEL are four 32-bit PORT select registers. They are read-only registers.

PASEL, PBSEL, PCSEL, PDSEL **0x10010050, 0x10010150, 0x10010250, 0x10010350**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SEL31	SEL30	SEL29	SEL28	SEL27	SEL26	SEL25	SEL24	SEL23	SEL22	SEL21	SEL20	SEL19	SEL18	SEL17	SEL16	SEL15	SEL14	SEL13	SEL12	SEL11	SEL10	SEL09	SEL08	SEL07	SEL06	SEL05	SEL04	SEL03	SEL02	SEL01	SEL00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
n	SEL n	Where n = 0 ~ 31 and SEL n = SEL0 ~ SEL31 SEL n is used for selecting the function of GPIO. When PXFUN = 0: 0: GPIO 1: Interrupt When PXFUN = 1: 0: Alternate Function 0[*1] 1: Alternate Function 1[*1] Note: 1. Please reference to Table 1-1 ~ Table 1-4 for the details.	R

PASEL bits 31-0 correspond to PA31-0; PBSEL to PB31-0; PCSEL to PC31-0 and PDSEL to PD 31-0.

1.2.15 PORT Select Set Register (PASELS, PBSELS, PCSELS, PDSELS)

PASELS, PBSELS, PCSELS and PDSELS are four 32-bit PORT select set registers. They are write-only registers.

PASELS, PBSELS, PCSELS, PFDSELS **0x10010054, 0x10010154, 0x10010254, 0x10010354**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SELS31	SELS30	SELS29	SELS28	SELS27	SELS26	SELS25	SELS24	SELS23	SELS22	SELS21	SELS20	SELS19	SELS18	SELS17	SELS16	SELS15	SELS14	SELS13	SELS12	SELS11	SELS10	SELS09	SELS08	SELS07	SELS06	SELS05	SELS04	SELS03	SELS02	SELS01	SELS00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	SELS n	Writing 1 to SELS n will set SEL n to 1 in register PXSEL. Writing 0 to SELS n will no use.	W

PASELS bits 31-0 correspond to PA31-0; PBSELS to PB31-0; PCSELS to PC31-0 and PDSELS to PD 31-0.

1.2.16 PORT Select Clear Register (PASELC, PBSELC, PCSELC, PDSELC)

PASELC, PBSELC, PCSELC and PDSELC are four 32-bit PORT select clear registers. They are write-only registers.

PASELC, PBSELC, PCSELC, PDSELC **0x10010058, 0x10010158, 0x10010258, 0x10010358**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SELC31	SELC30	SELC29	SELC28	SELC27	SELC26	SELC25	SELC24	SELC23	SELC22	SELC21	SELC20	SELC19	SELC18	SELC17	SELC16	SELC15	SELC14	SELC13	SELC12	SELC11	SELC10	SELC09	SELC08	SELC07	SELC06	SELC05	SELC04	SELC03	SELC02	SELC01	SELC00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	SELC n	Writing 1 to SELC n will set SEL n to 0 in register PXSEL. Writing 0 to SELC n will no use.	W

PASELC bits 31-0 correspond to PA31-0; PBSELC to PB31-0; PCSELC to PC31-0 and PDSELC to PD 31-0.

1.2.17 PORT Direction Register (PADIR, PBDIR, PCDIR, PDDIR)

PADIR, PBDIR, PCDIR and PDDIR are four 32-bit PORT direction registers. They are read-only registers.

PADIR, PBDIR, PCDIR, PDDIR **0x10010060, 0x10010160, 0x10010260, 0x10010360**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIR31	DIR30	DIR29	DIR28	DIR27	DIR26	DIR25	DIR24	DIR23	DIR22	DIR21	DIR20	DIR19	DIR18	DIR17	DIR16	DIR15	DIR14	DIR13	DIR12	DIR11	DIR10	DIR09	DIR08	DIR07	DIR06	DIR05	DIR04	DIR03	DIR02	DIR01	DIR00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
n	DIR n	Where n = 0 ~ 31 and DIR n = DIR0 ~ DIR31 DIR n is used for setting the direction of port or setting the trigger direction of interrupt trigger. GPIO Direction: (GPIO Function) 0: INPUT 1: OUTPUT Interrupt Trigger Direction: (Interrupt Function) PXTRG = 0: 0: Low Level Trigger 1: High Level Trigger PXTRG =1: 0: Falling Edge Trigger 1: Rising Edge Trigger	R

PADIR bits 31-0 correspond to PA31-0; PBDIR to PB31-0; PCDIR to PC31-0 and PDDIR to PD 31-0.

1.2.18 PORT Direction Set Register (PADIRS, PBDIRS, PCDIRS, PDDIRS)

PADIRS, PBDIRS, PCDIRS and PDDIRS are four 32-bit PORT direction set registers. They are write-only registers.

PADIRS, PBDIRS, PCDIRS, PDDIRS **0x10010064, 0x10010164, 0x10010264, 0x10010364**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIRS31	DIRS30	DIRS29	DIRS28	DIRS27	DIRS26	DIRS25	DIRS24	DIRS23	DIRS22	DIRS21	DIRS20	DIRS19	DIRS18	DIRS17	DIRS16	DIRS15	DIRS14	DIRS13	DIRS12	DIRS11	DIRS10	DIRS09	DIRS08	DIRS07	DIRS06	DIRS05	DIRS04	DIRS03	DIRS02	DIRS01	DIRS00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	DIRS n	Writing 1 to DIRS n will set DIR n to 1 in register PXDIR. Writing 0 to DIRS n will no use.	W

PADIRS bits 31-0 correspond to PA31-0; PBDIRS to PB31-0; PCDIRS to PC31-0 and PDDIRS to PD 31-0.

1.2.19 PORT Direction Clear Register (PADIRC, PBDIRC, PCDIRC, PDDIRC)

GPDIRC0, GPDIRC1, GPDIRC2 and GPDIRC3 are four 32-bit PORT direction clear registers. They are write-only registers.

PADIRS, PBDIRC, PCDIRC, PDDIRC **0x10010068, 0x10010168, 0x10010268, 0x10010368**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIRC31	DIRC30	DIRC29	DIRC28	DIRC27	DIRC26	DIRC25	DIRC24	DIRC23	DIRC22	DIRC21	DIRC20	DIRC19	DIRC18	DIRC17	DIRC16	DIRC15	DIRC14	DIRC13	DIRC12	DIRC11	DIRC10	DIRC09	DIRC08	DIRC07	DIRC06	DIRC05	DIRC04	DIRC03	DIRC02	DIRC01	DIRC00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	DIRC n	Writing 1 to DIRC n will set DIR n to 0 in register PXDIR. Writing 0 to DIRC n will no use.	W

PADIRC bits 31-0 correspond to PA31-0; PBDIRC to PB31-0; PCDIRC to PC31-0 and PDDIRC to PD 31-0.

1.2.20 PORT Trigger Register 0, 1, 2 and 3 (PATRG, PBTRG, PCTRG, PDTRG)

PATRG, PBTRG, PCTRG and PDTRG are four 32-bit PORT trigger registers. They are read-only registers.

PATRG, PBTRG, PCTRG, PDTRG **0x10010070, 0x10010170, 0x10010270, 0x10010370**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRIG31	TRIG30	TRIG29	TRIG28	TRIG27	TRIG26	TRIG25	TRIG24	TRIG23	TRIG22	TRIG21	TRIG20	TRIG19	TRIG18	TRIG17	TRIG16	TRIG15	TRIG14	TRIG13	TRIG12	TRIG11	TRIG10	TRIG09	TRIG08	TRIG07	TRIG06	TRIG05	TRIG04	TRIG03	TRIG02	TRIG01	TRIG00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
n	TRIG n	Where n = 0 ~ 31 and TRIG n = TRIG00 ~ TRIG31 TRIG n is used for setting the trigger mode for interrupt. When GPIO is used as interrupt function: 0: Level Trigger Interrupt. 1: Edge Trigger Interrupt. When GPIO is used as alternate function: 0: Alternate Function Group 0. 1: Alternate Function Group 1.	R

PATRG bits 31-0 correspond to PA31-0; PBTRG to PB31-0; PCTRG to PC31-0 and PDTRG to PD 31-0.

1.2.21 PORT Trigger Set Register (PATRGS, PBTRGS, PCTRGS, PDTRGS)

PATRGS, PBTRGS, PCTRGS and PDTRGS are four 32-bit PORT trigger set registers. They are write-only registers.

PATRGS, PBTRGS, PCTRGS, PDTRGS **0x10010074, 0x10010174, 0x10010274, 0x10010374**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRIGS31	TRIGS30	TRIGS29	TRIGS28	TRIGS27	TRIGS26	TRIGS25	TRIGS24	TRIGS23	TRIGS22	TRIGS21	TRIGS20	TRIGS19	TRIGS18	TRIGS17	TRIGS16	TRIGS15	TRIGS14	TRIGS13	TRIGS12	TRIGS11	TRIGS10	TRIGS09	TRIGS08	TRIGS07	TRIGS06	TRIGS05	TRIGS04	TRIGS03	TRIGS02	TRIGS01	TRIGS00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	TRIGS n	Writing 1 to TRIGS n will set TRIG n to 1 in register PXTRG. Writing 0 to TRIGS n will no use.	W

PATRGS bits 31-0 correspond to PA31-0; PBTRGS to PB31-0; PCTRGS to PC31-0 and PDTRGS to PD 31-0.

1.2.22 PORT Trigger Clear Register (PATRGC, PBTRGC, PCTRGC, PDTRGC)

PATRGC, PBTRGC, PCTRGC and PDTRGC are four 32-bit PORT trigger clear registers. They are write-only registers.

PATRGC, PBTRGC, PCTRGC, PDTRGC **0x10010078, 0x10010178, 0x10010278, 0x10010378**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRIGC31	TRIGC30	TRIGC29	TRIGC28	TRIGC27	TRIGC26	TRIGC25	TRIGC24	TRIGC23	TRIGC22	TRIGC21	TRIGC20	TRIGC19	TRIGC18	TRIGC17	TRIGC16	TRIGC15	TRIGC14	TRIGC13	TRIGC12	TRIGC11	TRIGC10	TRIGC09	TRIGC08	TRIGC07	TRIGC06	TRIGC05	TRIGC04	TRIGC03	TRIGC02	TRIGC01	TRIGC00
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
n	TRIGC n	Writing 1 to TRIGC n will set TRIG n to 0 in register PXTRG. Writing 0 to TRIGC n will no use.	W

PATRGC bits 31-0 correspond to PA31-0; PBTRGC to PB31-0; PCTRGC to PC31-0 and PDTRGC to PD 31-0.

1.2.23 PORT FLAG Register (PAFLG, PBFLG, PCFLG, PDFLG)

PAFLG, PBFLG, PCFLG and PDFLG are four 32-bit GPIO FLAG registers. They are read-only registers.

PAFLG, PBFLG, PCFLG, PDFLG **0x10010080, 0x10010180, 0x10010280, 0x10010380**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FLAG31	FLAG30	FLAG29	FLAG28	FLAG27	FLAG26	FLAG25	FLAG24	FLAG23	FLAG22	FLAG21	FLAG20	FLAG19	FLAG18	FLAG17	FLAG16	FLAG15	FLAG14	FLAG13	FLAG12	FLAG11	FLAG10	FLAG09	FLAG08	FLAG07	FLAG06	FLAG05	FLAG04	FLAG03	FLAG02	FLAG01	FLAG00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
n	FLAG n	Where n = 0 ~ 31 and FLAG n = FLAG00 ~ FLAG31 FLAG n is interrupt flag bit for checking the interrupt whether to happen. When GPIO is used as interrupt function and the interrupt happened, the FLAG n in PXFLG will be set to 1.	R

PAFLG bits 31-0 correspond to PA31-0; PBFLG to PB31-0; PCFLG to PC31-0 and PDFLG to PD 31-0.

1.2.24 PORT FLAG Clear Register (PAFLGC, PBFLGC, PCFLGC, PDFLGC)

PAFLGC, PBFLGC, PCFLGC and PDFLGC are four 32-bit GPIO FLAG Clear registers. They are read-only registers.

PAFLGC, PBFLGC, PCFLGC, PDFLGC **0x10010014, 0x10010114, 0x10010214, 0x10010314**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FLAGC31	FLAGC30	FLAGC29	FLAGC28	FLAGC27	FLAGC26	FLAGC25	FLAGC24	FLAGC23	FLAGC22	FLAGC21	FLAGC20	FLAGC19	FLAGC18	FLAGC17	FLAGC16	FLAGC15	FLAGC14	FLAGC13	FLAGC12	FLAGC11	FLAGC10	FLAGC09	FLAGC08	FLAGC07	FLAGC06	FLAGC05	FLAGC04	FLAGC03	FLAGC02	FLAGC01	FLAGC00
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	R/W
n	FLAGC n	When GPIO is used as interrupt function and when write 1 to the bit, the bit FLAG n in PXFLG will be cleared.	R

PAFLGC bits 31-0 correspond to PA31-0; PBFLGC to PB31-0; PCFLGC to PC31-0 and PDFLGC to PD 31-0.

1.3 Program Guide

1.3.1 GPIO Function Guide

1. Set PXFUN to choose the function of GPIO / Interrupt by writing 1 to register PXFUNC.
2. Set PXSEL to choose the function of GPIO by writing 1 to register PXSELC.
3. Set PXDIR to choose the direction of GPIO by writing 1 to register PXDIRS or PXDIRC.
4. Others.

(1) You can read the PORT PIN level by reading register PXPIN.

(2) You can use register PXDAT as normal data register. The register can be set by register PXDATS and PXDATC.

(3) You can set PXPE by writing 1 to register PXPES or PXPE to use Internal pull-up/down resistor or not.

1.3.2 Alternate Function Guide

1. Set PXFUN to 0 by writing 1 to register PXFUNC. (Ready state)

2. Set PXTRG to choose the alternate function group 0 by writing 1 to register PXTRGC.
   Set PXTRG to choose the alternate function group 1 by writing 1 to register PXTRGS.

3. Set PXSEL to choose the alternate function 0 by writing 1 to register PXSELC.
   Set PXSEL to choose the alternate function 1 by writing 1 to register PXSELS.

4. Set PXFUN to choose the function of alternate function by writing 1 to register PXFUNS.

1.3.3 Interrupt Function Guide

First you should keep GPIO status.

1. Set PXIM by writing 1 to register PXIMS.

2. Set PXTRG to choose the interrupt trigger mode by writing 1 to register PXTRGS or PXTRGC.

3. Set PXFUN to choose the function of GPIO / Interrupt by writing 1 to register or PXFUNC.
4. Set PXSEL to choose the Interrupt function by writing 1 to register PXSELS.

5. Set PXDIR to choose the direction of interrupt trigger by writing 1 to register PXDIRS or PXDIRC.

6. Set the PXFLGC register to clear the interrupt flag.
7. Clear PXIM by writing 1 to register PXIMC to enable the GPIO interrupt.

8. Others.

You should check the level interrupt whether to happen as follows:

(1) When the PIN level read from register PXPIN is the same with what you have set in register PXTRG and PXDIR, then the level interrupt happened.

(2) When the PIN level read from register PXPIN is different from what you have set in register PXTRG and PXDIR, then the level interrupt did not happen.

1.3.4 Disable Interrupt Function Guide

1. Set PXIM by writing 1 to register PXIMS.

2. Set PXTRG to 0 by writing 1 to register PXTRGC.
3. Set PXDIR to 0 by writing 1 to register PXDIRC.

4. Set PXFUN to 0 by writing 1 to register or PXFUNC.
5. Set PXSEL to 0 by writing 1 to register PXSELC.