1 CPU Core

At the heart of Jz4740 is the JzRISC processor core. JzRISC adopts a brand new micro-architecture which provides superior performance and power consumption than existent industry cores. Detailed description of JzRISC cores is specified in document titled “JzRISC Core User Manual”

Key features of JzRISC core implemented in Jz4740 are as following:

Table 1-1 JzRISC Core Features

Item	Features
RISC ISA	• Industry standard Instruction set architecture • 32 32-bit general purpose registers
Ingenic Media ISA	• Implement 60 SIMD like instructions for multimedia acceleration • See document “Ingenic Media Instruction Set Architecture”
Ingenic Floating Point ISA	• Not implemented
Multiply-Divide Unit (MDU)	• Maximum issue rate of one 32x16 multiply every clock • Maximum issue rate of one 32x32 multiply every other clock • Minimum 2 clock cycle, maximum 34 clock cycles for divide
Memory Manager Unit (MMU)	• 4 G-Bytes of address space • 32/16 dual-entry full associative joint TLB plus 4 dual-entry ITLB and 4 dual-entry DTLB respectively • 7 different page size from 4Kb to 16MB supported in any entry • Support entry lock • Space identifier ASID: 8 bits
Data Cache	• Virtually-indexed, physically-tagged • 4 way, 8-word line, alterable size: 4K, 8K, 16K bytes • LRU replacement algorithm • Write-back, write-through • 16-word depth write buffer
Instruction Cache	• Physically-indexed, physically-tagged • 4 way, 8-word line, alterable size: 4K, 8K, 16K bytes • LRU replacement algorithm
Debug&JTAG	• JTAG interface to host machine • ACC mode to accelerate JTAG memory access • Two instruction and one data breakpoint
Branch Target Buffer (BTB)	• Virtally-tagged • Up to 64 entry direct mapped • 2-bit branch history maintained
Bus Interface	• compliance with AHB protocol