1 Internal CODEC

1.1 Overview

This chapter describes internal audio CODEC embedded in the Jz4740/Jz4720 processor and related software interface.

The internal CODEC is an I2S audio CODEC with 18 bits DAC and 16 bits ADC. It also has several memory mapped registers used to control and configure the CODEC. AIC is used to interface to the CODEC for audio data replaying and recording.

1.1.1 Features

The following are internal CODEC features:

- DAC: 18 bits sample size, SNR 90dB
- ADC: 16 bits sample size, SNR 85dB
- Sample rate: 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz and 48kHz
- Head phone amplifier to support up to 16ohm load.
- Anti-pop for head phone out
- Low power dissipation mode
- Digital volume control

1.1.2 Signal Descriptions

CODEC has 5 ~ 7 signal IO pins depending on various chips. They are listed and described in Table 1-1.

Table 1-1 CODEC signal IO pin description

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
LHPO	AO	E14			LHPO: Left headphone out	VDD_{CDC}
RHPO	AO	E13			RHPO: Right headphone out	VDD_{CDC}
MICIN	AI	D14			MICIN: Microphone input	VDD_{CDC}
MICBIAS	AO	E15			MICBIAS: Microphone bias	VDD_{CDC}
LLINEIN	AI	D12			LLINEIN: Left line input	VDD_{CDC}
RLINEIN	AI	D13			RLINEIN: Right line input	VDD_{CDC}
VREF	AO	E12			VREF: Voltage Reference Output. An electrolytic capacitor more than 10μF in parallel with a 0.1μF ceramic capacitor attached from this pin to VSSCDC eliminates the effects of high frequency noise	VDD_{CDC}
VDDHP	P	G12			VDDHP: Headphone amplifier power, 3.3V	-

Pin Names	IO	4740 Loc	4720 Loc	IO Cell Char.	Pin Description	Power
VSSHP	P	G10			VSSHP: Headphone amplifier ground	-
VDDCDC	P	D11			VDDCDC: CODEC analog power, 3.3V	-
VSSCDC	P	F9			VSSCDC: CODEC analog ground	-

1.1.3 Block Diagram

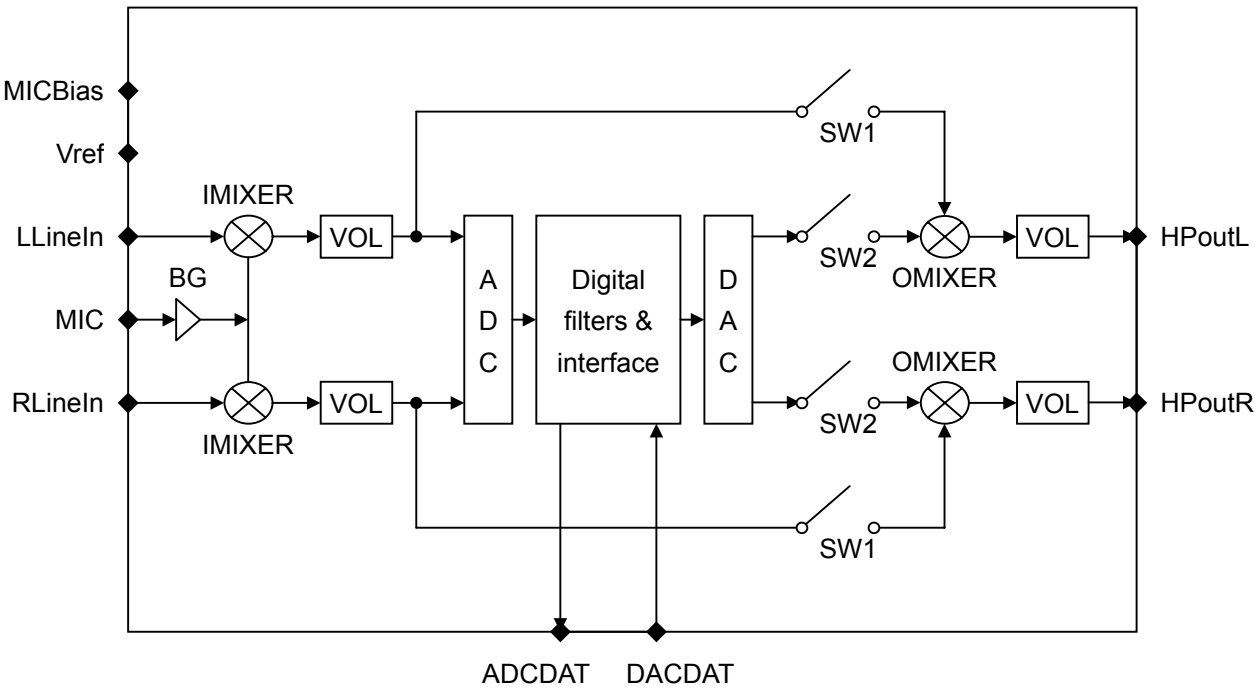


Figure 1-1 CODEC block diagram

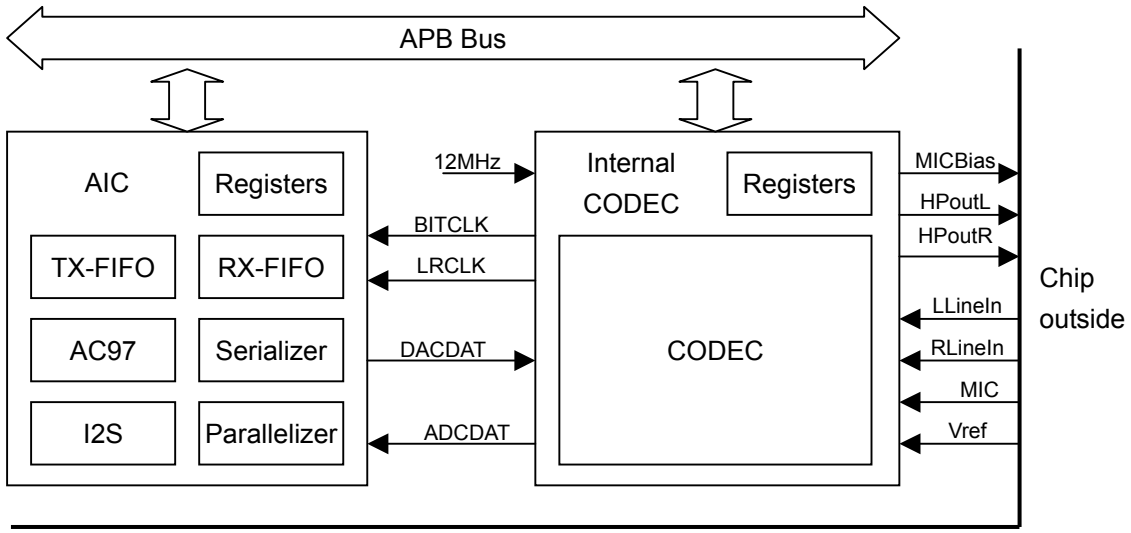


Figure 1-2 Internal CODEC works with AIC

1.2 Register Descriptions

The internal CODEC software interface includes 2 registers. They are mapped in IO memory address space so that program can access them to control the operations of the CODEC.

Table 1-2 Internal CODEC Registers Description

Name	Description	RW	Reset value	Address	Size
CDCCR1	CODEC Control Register 1	RW	0x021B2302	0x10020080	32
CDCCR2	CODEC Control Register 2	RW	0x00170803	0x10020084	32

- CDCCR1 is used to control MIC input, LINE input, headphone out, ADC, DAC, CODEC suspend/reset and anti-pop procedures.
- CDCCR2 is used to control values or gains of MIC input, LINE input and headphone, and audio sample rate.

1.2.1 CODEC Control Register 1 (CDCCR1)

CDCCR1 contains bits to control MIC input, LINE input, headphone out, ADC, DAC, CODEC suspend/reset and anti-pop procedures. Set AICFR.ICDC to 1 before write to this register, or the effect is undefined.

CDCCR1 **0x10020080**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		ELININ	EMIC	SW1ON	EADC	SW2ON	EDAC	Reserved			PDVR	PDVRA	VRPLD	VRCGL	VRCGH	Reserved	HPMUTE	HPOV0	HPCG	HPPLDM	HPPLDR	PDHPM	PDHP	Reserved						SUSPD	RST
RST	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	0	0	1	0	0	0	1	1	0	0	0	0	0	0	1	0

Bits	Name	Description	RW
31:30	Reserved	Writes to these bits have no effect and always read as 0	R
29	ELININ	LINE input enabled. ELININ: 0 — LINE input is disabled; 1 — LINE input is enabled	RW
28	EMIC	MIC input enabled. EMIC: 0 — MIC input is disabled; 1 — MIC input is enabled	RW
27	SW1ON	Switch 1 (SW1) in CODEC is on. When switch 1 is on, the input audio is taken by the output audio mixer and sends to the headphone output. SW1ON: 0 — SW1 is off; 1 — SW1 is on	RW
26	EADC	Enable ADC. EADC: 0 — The ADC is disabled. No AD convert can be down; 1 — The ADC is enabled.	RW
25	SW2ON	Switch 2 (SW2) in CODEC is on. When switch 2 is on, the audio from DAC is taken by the output audio mixer and sends to the headphone output. If this switch is off, DAC audio cannot be heard SW2ON: 0 — SW2 is off; 1 — SW2 is on	RW
24	EDAC	Enable ADC. EADC: 0 — The DAC is disabled. No DA convert can be down	RW

		1 — The DAC is enabled.	
23:21	Reserved	Writes to these bits have no effect and always read as 0	R
20	PDVR	Power down Vref.	RW
19	PDVRA	Power down Vref amplifier.	RW
18	VRPLD	Vref pull-down	RW
17	VRCGL	Charge Vref capacitors with lower current.	RW
16	VRCGH	Charge Vref capacitors with high current.	RW
15	Reserved	Writes to these bits have no effect and always read as 0	R
14	HPMUTE	Headphone Mute. **HPMUTE** / **Description** 0 — Headphone is not mute 1 — Headphone is mute	RW
13	HPOV0	Headphone amplifier value changed at the audio over zero. This bit should be set to 1 in most cases to prevent noise when change HP amplifier value by change HPVOL. It should be set to 0 in linear anti pop procedure. **HPOV0** / **Description** 0 — Headphone amplifier value changed at any time 1 — Headphone amplifier value changed at the audio over zero.	RW
12	HPCG	Change HP	RW
11	HPPLDM	Pull-down HP in M mode	RW
10	HPPLDR	Pull-down HP in R mode	RW
9	PDHPM	Power down HP in M mode	RW
8	PDHP	Power down HP	RW
7:2	Reserved	Writes to these bits have no effect and always read as 0	R
1	SUSPD	CODEC suspend. When this bit is 1, CODEC is forced to suspend mode, which consumes minimum power. Before headphone amplifier turn on procedure, change this bit to 0. If HP amplifier is on, please turn it off before set this bit to 1. Otherwise, pop noise will be found. Please reference to 1.3.3 for more details about CODEC power consumption.	RW
0	RST	Reset the CODEC. The RST should be kept for at least 2us. It should not reset CODEC for too long time. Don't reset CODEC during replay/record, or noise will be found. The CODEC should be reset every time before it wakes up or power on. **RST** / **Description** 0 — CODEC is not reset 1 — CODEC is reset	RW

1.2.2 CODEC Control Register 2 (CDCCR2)

CDCCR2 contains bits to control values or gains of MIC input, LINE input and headphone, and audio sample rate. Set AICFR.ICDC to 1 before write to this register, or the effect is undefined.

CDCCR2 **0x10020084**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												LINVOL				Reserved				SMPR				Reserved		MICBG		Reserved		HPVOL	
RST	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1

Bits	Name	Description	RW
31:21	Reserved	Writes to these bits have no effect and always read as 0	R
20:16	LINVOL	The LINE input programmable gain amplifier volume control. LINVOL: 0 → Gain: -34.5 dB; 1 → -33.0 dB; … → (LINVOL * 1.5) – 34.5; 23 → 0 dB; … → …; 30 → +10.5 dB; 31 → +12.0 dB	RW
15:12	Reserved	Writes to these bits have no effect and always read as 0	R
11:8	SMPR	The audio sample rate. There is an error of 0.04% exists for some sample rates. The sample rate for ADC and DAC is the same if then work in the same time. SMPR should be changed during AIC register AICCR.EREC=0 and AICCR.ERPL=0, or noise may be recorded/heard. SMPR / Nominal Sample Rate (kHz) / Actual Sample Rate (kHz): 0000: 8 / 8; 0001: 11.025 / 11.029; 0010: 12 / 12; 0011: 16 / 16; 0100: 22.05 / 22.059; 0101: 24 / 24; 0110: 32 / 32; 0111: 44.1 / 44.118; 1000: 48 / 48	RW
7:6	Reserved	Writes to these bits have no effect and always read as 0	R

<table>
<tr><td>5:4</td><td>MICBG</td><td>MIC Boost Gain.<table><tr><th>MICBG</th><th>MIC Boost Gain</th></tr><tr><td>00</td><td>0 dB</td></tr><tr><td>01</td><td>6 dB</td></tr><tr><td>10</td><td>12 dB</td></tr><tr><td>11</td><td>20 dB</td></tr></table></td><td>RW</td></tr>
<tr><td>3:2</td><td>Reserved</td><td>Writes to these bits have no effect and always read as 0</td><td>R</td></tr>
<tr><td>1:0</td><td>HPVOL</td><td>Headphone amplifier volume control.<table><tr><th>HPVOL</th><th>Gain</th></tr><tr><td>00</td><td>0 dB</td></tr><tr><td>01</td><td>2 dB</td></tr><tr><td>10</td><td>4 dB</td></tr><tr><td>11</td><td>6 dB</td></tr></table></td><td>RW</td></tr>
</table>

1.3 Operation

The internal CODEC can be accessed by the processor using programmed I/O instructions via memory mapped registers. CODEC memory mapped registers are only for the CODEC controlling. The audio data transferring, i.e. audio replaying and recording, is down by AIC. AIC still takes the role of I2S controller where CODEC memory mapped registers take the role of CODEC controlling interface just like L3 bus or I2C bus for an external CODEC. We will refer to many AIC operations and registers in the following audio operation descriptions. Please reference to AIC spec for the details.

1.3.1 Initialization

At power-on or other hardware reset (WDT, wakeup from hibernating mode and etc), The CODEC is reset and is put in suspend mode. The CODEC is also be reset at the time it leaves suspend mode. So if there's error found in the CODEC, set CDCCR.SUSPD to 1 and then set it to 0 will reset CODEC from the error.

To use the internal CODEC with AIC, several AIC registers should be set as,

AICFR.ICDC = 1
AICFR.AUSEL = 1
AICFR.BCKD = 0
AICFR.SYNCD = 0
I2SCR.AMSL = 0

1.3.2 CODEC controlling and typical operations

Table 1-3 CODEC settings in various applications

SUSPD	ELININ	EMIC	Set MICBG	Set LINVOL	EADC	SW1ON	EDAC	SW2ON	Set SMPR	HP Amp	HPMUTE	Set HPVOL	Applications
0	0	0	N	N	0	0	1	1	Y	ON	0	Y	Audio data replay
0	1	0	N	Y	0	1	1	1	Y	ON	0	Y	Audio data replay mixed with LINE input
0	0	1	Y	Y	0	1	1	1	Y	ON	0	Y	Audio data replay mixed with MIC input
0	1	1	Y	Y	0	1	1	1	Y	ON	0	Y	Audio data replay mixed with MIC and LINE input
0	0	1	Y	Y	1	0	1	1	Y	ON	0	Y	Audio data replay while record MIC input without
0	1	0	N	Y	0	1	0	0	N	ON	0	Y	Playback LINE input audio
0	1	0	N	Y	1	0	0	0	Y	ON	1	N	Record LINE input audio without playback 1[1]
0	1	0	N	Y	1	?	0	?	Y	OFF	?	N	Record LINE input audio without playback 2[2]
0	1	0	N	Y	1	1	0	0	Y	ON	0	Y	Record LINE input audio with playback
0	0	1	Y	Y	0	1	0	0	N	ON	0	Y	Playback MIC input audio
0	0	1	Y	Y	1	0	0	0	Y	ON	1	N	Record MIC input audio without playback 1[1]
0	0	1	Y	Y	1	?	0	?	Y	OFF	?	N	Record MIC input audio without playback 2[2]
0	0	1	Y	Y	1	1	0	0	Y	ON	0	Y	Record MIC input audio with playback
0	1	1	Y	Y	0	1	0	0	N	ON	0	Y	Playback MIC/LINE mixed input audio
0	1	1	Y	Y	1	0	0	0	Y	ON	1	N	Record MIC/LINE mixed input audio without playback 1[1]
0	1	1	Y	Y	1	?	0	?	Y	OFF	?	N	Record MIC/LINE mixed input audio without playback 2[2]
0	1	1	Y	Y	1	1	0	0	Y	ON	0	Y	Record MIC/LINE mixed input audio with playback
1	?	?	?	?	?	?	?	?	?	?	?	?	CODEC is off, no action can be taken

Notes:

1. HP amplifier turn on/turn off procedures are complicate and may produce noise.
2. Turn off HP amplifier can save power

Table 1-3 lists the CODEC settings in many applications. Following are more details for some typical operations.

1.3.2.1 Audio data replay

To replay audio data to the internal CODEC, please consult the following steps.

1. Turn HP amplifier on if it is off or the CODEC is suspended.
2. Set CDCCR1.ELININ=0, CDCCR1.EMIC=0, CDCCR1.EADC=0, CDCCR1.SW1ON=0, CDCCR1.EDAC=1, CDCCR1.SW2ON=1, CDCCR1.HPMUTE=0
3. Set proper HP amplifier volume CDCCR2.HPVOL

4. Set proper sample rate CDCCR2.SMPR
5. Set proper sample size AICCR.OSS
6. Configure other audio replaying features
7. Configure AIC TX-FIFO, interrupt
8. Setup DMA and interrupt for audio data
9. Set AICCR.ERPL=1 to replay
10. After finished the data replaying, set AICCR.ERPL=0

1.3.2.2 Audio data replay while record MIC input without playback

To replay audio data to the internal CODEC, in the same time, record audio from the internal CODEC MIC input without playback them, please consult the following steps.

1. Turn HP amplifier on if it is off or the CODEC is suspended.
2. Set CDCCR1.ELININ=0, CDCCR1.EMIC=1, CDCCR1.EADC=1, CDCCR1.SW1ON=0, CDCCR1.EDAC=1, CDCCR1.SW2ON=1, CDCCR1.HPMUTE=0
3. Set proper MIC boost gain volume CDCCR2.MICBG, input amplifier volume CDCCR2.LINVOL and HP amplifier volume CDCCR2.HPVOL
4. Set proper ADC and DAC sample rate CDCCR2.SMPR
5. Set proper DAC sample size AICCR.OSS and ADC sample size AICCR.ISS to 16 bits
6. Configure other audio replaying features
7. Configure AIC TX-FIFO, RX-FIFO, interrupt
8. Setup DMA and interrupt for both incoming and outgoing audio data
9. Set AICCR.ERPL=1 to replay and AICCR.EREC=1 to record
10. After finished the data replaying, set AICCR.ERPL=0
11. After finished the record, set AICCR.EREC=0

1.3.2.3 Playback LINE input audio

To playback audio LINE input in the internal CODEC, please consult the following steps.

1. Turn HP amplifier on if it is off or the CODEC is suspended.
2. Set CDCCR1.ELININ=1, CDCCR1.EMIC=0, CDCCR1.EADC=0, CDCCR1.SW1ON=1, CDCCR1.EDAC=0, CDCCR1.SW2ON=0, CDCCR1.HPMUTE=0
3. Set proper input amplifier volume CDCCR2.LINVOL and HP amplifier volume CDCCR2.HPVOL

1.3.2.4 Record LINE input audio with playback

To record audio from the internal CODEC LINE input, in the same time playback them, please consult the following steps.

1. Turn HP amplifier on if it is off or the CODEC is suspended.
2. Set CDCCR1.ELININ=1, CDCCR1.EMIC=0, CDCCR1.EADC=1, CDCCR1.SW1ON=1,

CDCCR1.EDAC=0, CDCCR1.SW2ON=0, CDCCR1.HPMUTE=0

3. Set proper input amplifier volume CDCCR2.LINVOL and HP amplifier volume CDCCR2.HPVOL
4. Set proper sample rate CDCCR2.SMPR
5. Set sample size AICCR.ISS to 16 bits
6. Configure other audio record features
7. Configure AIC RX-FIFO, interrupt
8. Setup DMA and interrupt for audio data
9. Set AICCR.EREC=1 to record
10. After finished the record, set AICCR.EREC=0

1.3.2.5 Record MIC input audio without playback 2

To record audio from the internal CODEC MIC input without playback them, please consult the following steps.

1. If HP amplifier is on, turn it off.
2. Set CDCCR1.SUSPD=0, CDCCR1.ELININ=0, CDCCR1.EMIC=1, CDCCR1.EADC=1, CDCCR1.EDAC=0
3. Set proper MIC boost gain volume CDCCR2.MICBG and input amplifier volume CDCCR2.LINVOL
4. Set proper sample rate CDCCR.SMPR
5. Set sample size AICCR.ISS to 16 bits
6. Configure other audio record features
7. Configure AIC RX-FIFO, interrupt
8. Setup DMA and interrupt for audio data
9. Set AICCR.EREC=1 to record
10. After finished the record, set AICCR.EREC=0

1.3.3 Power saving

1.3.4 Pop noise in HP amplifier turn on and turn off

The internal CODEC includes an amplifier for headphone output. The pop noise when headphone amplifies turning on and turning off (power on/off) is normally an issue for an audio CODEC. In Jz4740/Jz4720, we provide three approaches to reduce the pop noise.

1.3.4.1 Pre-change anti-pop HP turn-on/off procedure

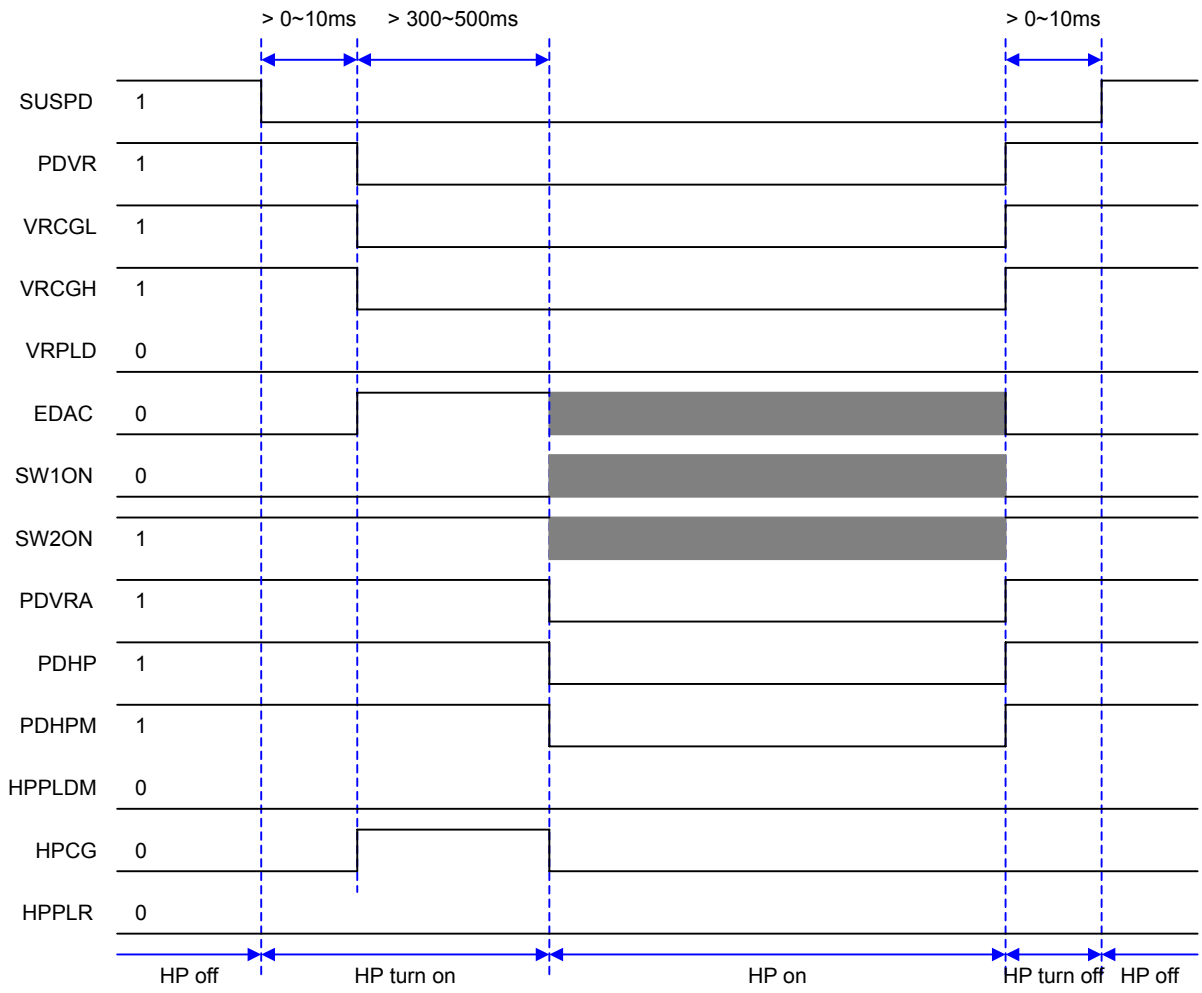


Figure 1-3 HP amplifier pre-charge anti-pop turn on/off timing diagram

1.3.4.2 VREF anti-pop HP turn-on/off procedure

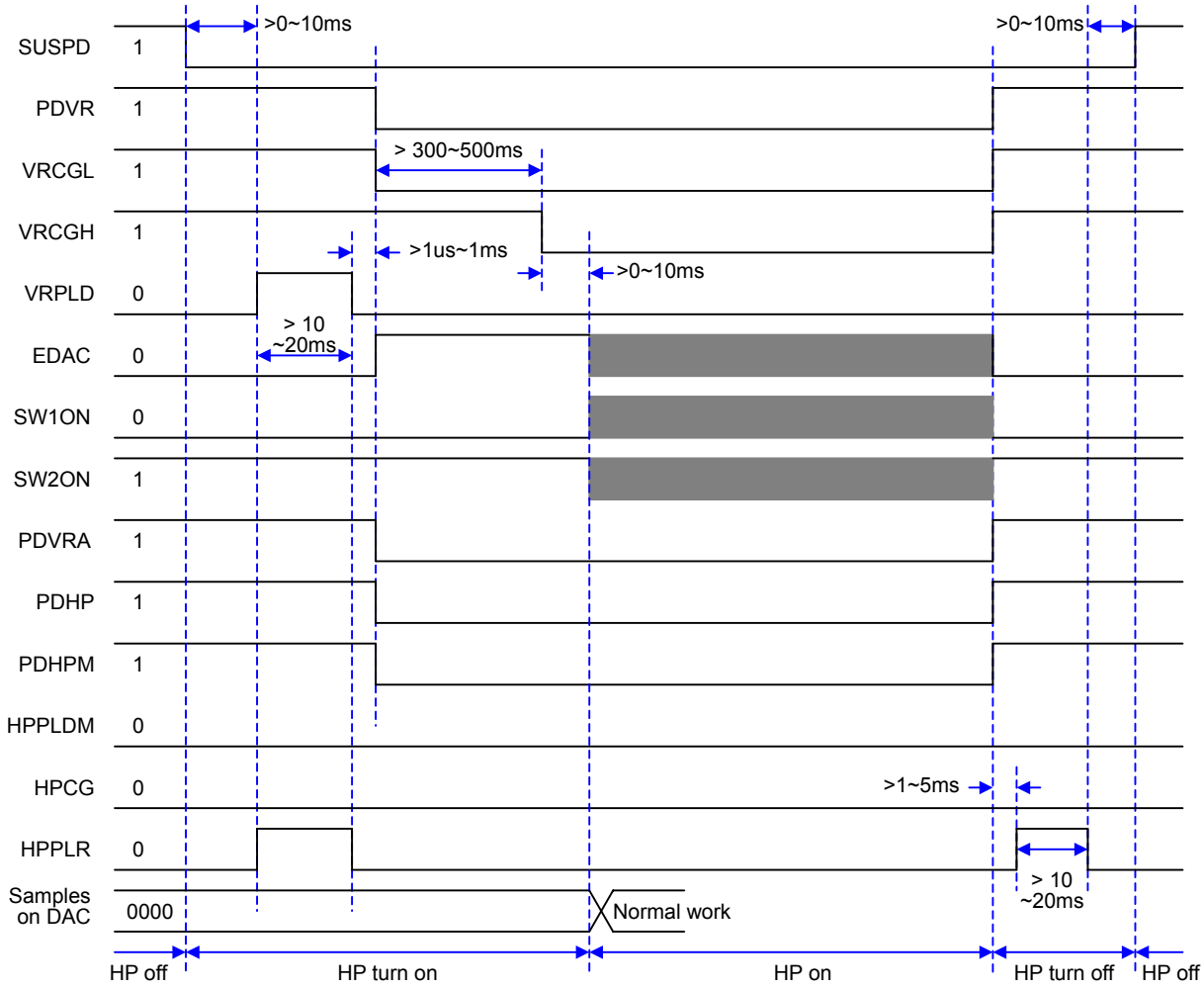


Figure 1-4 HP amplifier VREF anti-pop turn on/off timing diagram

1.3.4.3 Linear anti-pop HP turn-on/off procedure

The principle is, at HP amplifier turning on (power on), replay a piece of audio data to bring amplifier output voltage from 0 voltage, which is represented by maximum negative audio data, to mid-voltage, which is represented by zero audio data, slowly and smoothly. The turning off procedure is just the reverse. In these periods, most of the energy is spend in the frequencies lower than human hearing limitation, to reduce the noise. Figure 1-5 illustrates the procedure.

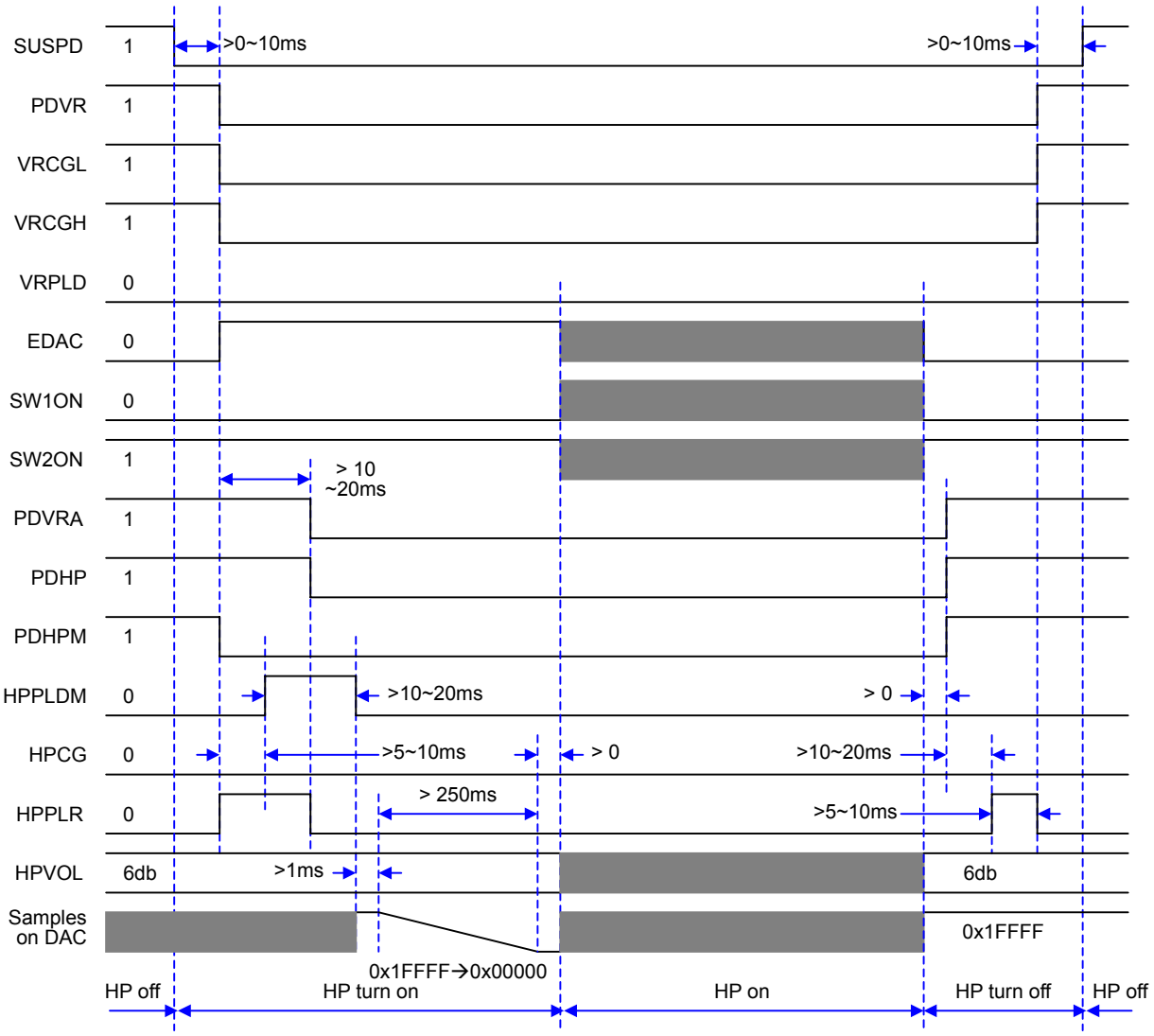
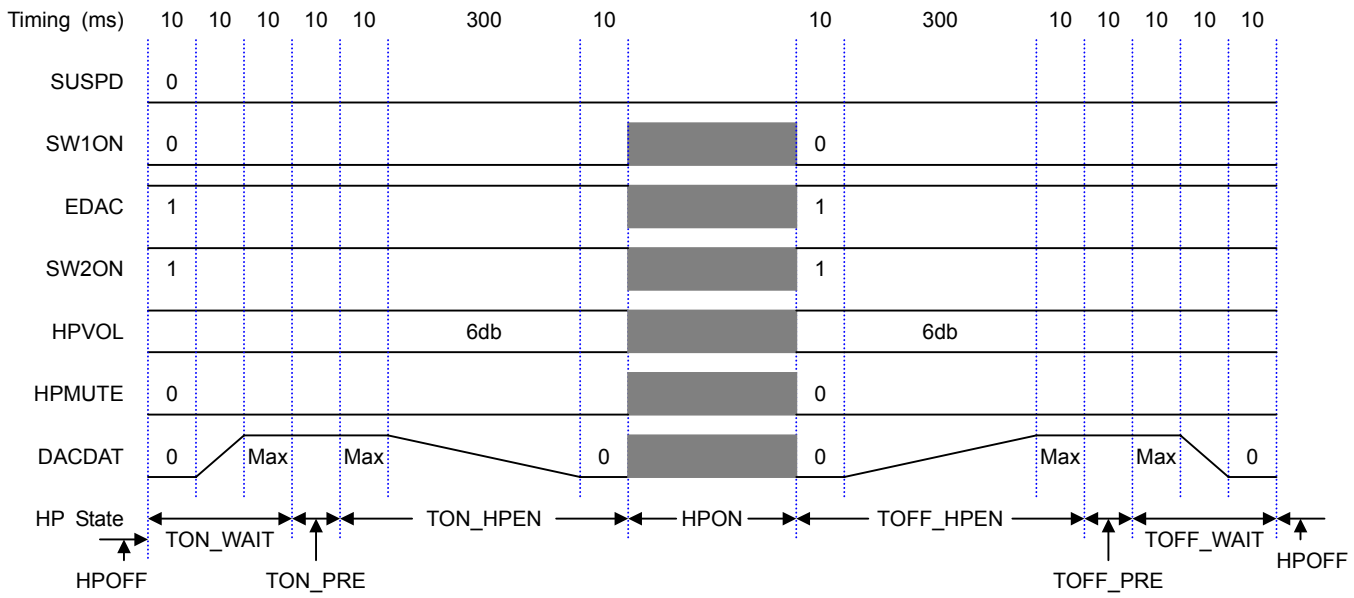


Figure 1-5 HP amplifier linear anti-pop turn on/off timing diagram



To accomplish the anti-pop tasks, hardware and software need to cooperate. 错误！未找到引用源。 shows the hardware state machine that reflects headphone amplifier state, the related operation and the state transfer.

1.4 Timing parameters

1.5 AC & DC parameters