1 Timer/Counter Unit

1.1 Overview

The TCU (Timer/Counter with PWM output) contains 8 channels of 16-bit programmable timers (timers 0 to 7). They can be used as Timer or PWM.

TCU has the following features:

- Six independent channels, each consisting of
  — Counter
  — Data register (FULL and HALF)
  — Control register
- Independent clock for each counter, selectable by software
  — PCLK, EXTAL and RTCCLK can be used as the clock for counter
  — The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
- FULL interrupt and HALF interrupt can be generated for each channel using the compare data registers
  — Timer 0 and Timer 1 have separated interrupt.
  — Timer 2-7 has one interrupt in common.
  — Timer 0-7 can be used as PWM (Set the initial signal level)

1.2 Pin Description

Table 1-1 PWM Pins Description

Name	I/O	Description
PWM [7:0]	Output	PWM channel output signals.

1.3 Register Description

In this section, we will describe the registers in timer. Following table lists all the registers definition. All timer register's 32bit address is physical address. And detailed function of each register will be described below.

Name	Description	RW	Reset Value	Address	Access Size
TSR	Timer STOP Register	R	0x00	0x1000201C	8
TSSR	Timer STOP Set Register	W	0x00	0x1000202C	8
TSCR	Timer STOP Clear Register	W	0x00	0x1000203C	8
TER	Timer Counter Enable Register	R	0x00	0x10002010	8
TESR	Timer Counter Enable Set Register	W	0x??	0x10002014	8
TECR	Timer Counter Enable Clear Register	W	0x??	0x10002018	8
TFR	Timer Flag Register	R	0x00000000	0x10002020	32
TFSR	Timer Flag Set Register	W	0x????????	0x10002024	32
TFCR	Timer Flag Clear Register	W	0x????????	0x10002028	32
TMR	Timer Mask Register	R	0x00000000	0x10002030	32
TMSR	Timer Mask Set Register	W	0x????????	0x10002034	32
TMCR	Timer Mask Clear Register	W	0x????????	0x10002038	32
TDFR0	Timer Data FULL Register 0	RW	0x????	0x10002040	16
TDHR0	Timer Data HALF Register 0	RW	0x????	0x10002044	16
TCNT0	Timer Counter 0	RW	0x????	0x10002048	16
TCSR0	Timer Control Register 0	RW	0x0000	0x1000204C	16
TDFR1	Timer Data FULL Register 1	RW	0x????	0x10002050	16
TDHR1	Timer Data HALF Register 1	RW	0x????	0x10002054	16
TCNT1	Timer Counter 1	RW	0x????	0x10002058	16
TCSR1	Timer Control Register 1	RW	0x0000	0x1000205C	16
TDFR2	Timer Data FULL Register 2	RW	0x????	0x10002060	16
TDHR2	Timer Data HALF Register 2	RW	0x????	0x10002064	16
TCNT2	Timer Counter 2	RW	0x????	0x10002068	16
TCSR2	Timer Control Register 2	RW	0x0000	0x1000206C	16
TDFR3	Timer Data FULL Register 3	RW	0x????	0x10002070	16
TDHR3	Timer Data HALF Register 3	RW	0x????	0x10002074	16
TCNT3	Timer Counter 3	RW	0x????	0x10002078	16
TCSR3	Timer Control Register 3	RW	0x0000	0x1000207C	16
TDFR4	Timer Data FULL Register 4	RW	0x????	0x10002080	16
TDHR4	Timer Data HALF Register 4	RW	0x????	0x10002084	16
TCNT4	Timer Counter 4	RW	0x????	0x10002088	16
TCSR4	Timer Control Register 4	RW	0x0000	0x1000208C	16
TDFR5	Timer Data FULL Register 5	RW	0x????	0x10002090	16
TDHR5	Timer Data HALF Register 5	RW	0x????	0x10002094	16

TCNT5	Timer Counter 5	RW	0x????	0x10002098	16
TCSR5	Timer Control Register 5	RW	0x0000	0x1000209C	16
TDFR6	Timer Data FULL Register 6	RW	0x????	0x100020A0	16
TDHR6	Timer Data HALF Register 6	RW	0x????	0x100020A4	16
TCNT6	Timer Counter 6	RW	0x????	0x100020A8	16
TCSR6	Timer Control Register 6	RW	0x0000	0x100020AC	16
TDFR7	Timer Data FULL Register 7	RW	0x????	0x100020B0	16
TDHR7	Timer Data HALF Register 7	RW	0x????	0x100020B4	16
TCNT7	Timer Counter 7	RW	0x????	0x100020B8	16
TCSR7	Timer Control Register 7	RW	0x0000	0x100020BC	16

1.3.1 Timer Control Register (TCSR)

The TCSR is a 16-bit read/write register. It contains the control bits for each channel. It is initialized to 0x00 by any reset.

TCSR0, TCSR1, TCSR2, TCSR3, TCSR4, TCSR5, TCSR6, TCSR7

0x1000204C, 0x1000205C, 0x1000206C, 0x1000207C, 0x1000208C, 0x1000209C, 0x100020AC, 0x100020BC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						SD	INITL	PWM_EN	Reserved	PRESCALE			EXT_EN	RTC_EN	PCK_EN
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
15:10	Reserved	These bits always read 0, and written are ignored.	R
9	SD	Shut Down (SD) the PWM output. 0: Graceful shutdown 1: Abrupt shutdown Graceful shutdown: The output level for PWM output will keep the level after the comparison match of FULL. Abrupt shutdown: The output level for PWM output will keep the level.	RW
8	INITL	Selects an initial output level for PWM output. 1: High 0: Low	RW
7	PWM_EN	PWM output pin control bit 1: PWM pin output enable 0: PWM pin output disable, and the PWM pin will be set to the initial level according to INITL.	RW
6	Reserved	These bits always read 0, and written are ignored.	R
5:3	PRESCALE	These bits select the TCNT count clock frequency. Don't change this field when the channel is running	RW
2	EXT_EN	Select EXTAL as the timer clock input.	RW

Bit 2	Bit1	Bit 0	Description
0	0	0	Internal clock: CLK/1
0	0	1	Internal clock: CLK/4
0	1	0	Internal clock: CLK/16
0	1	1	Internal clock: CLK/64
1	0	0	Internal clock: CLK/256
1	0	1	Internal clock: CLK/1024
110~111			Reserved

		1: Enable 0: Disable	
1	RTC_EN	Select RTCCLK as the timer clock input. 1: Enable 0: Disable	RW
0	PCK_EN	Select PCLK as the timer clock input. 1: Enable 0: Disable	RW

Note:
The input clock of timer and the PCLK should keep to the rules as follows:

Input clock of timer: IN_CLK	**Clock generated from the frequency divider (PRESCALE): DIV_CLK**
PCK_EN == 0, RTC_EN == 1 and EXT_EN == 0 (IN_CLK = RTCCLK)	$f_{DIV\_CLK} < ½ f_{PCLK}$
PCK_EN == 0, RTC_EN == 0 and EXT_EN == 1 (IN_CLK = EXTAL)	$f_{DIV\_CLK} < ½ f_{PCLK}$
PCK_EN == 1, RTC_EN == 0 and EXT_EN == 0 (IN_CLK = PCLK)	ANY

1.3.2 Timer Data FULL Register (TDFR)

The comparison data FULL registers TDFR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

TDFR0, TDFR1, TDFR2, TDFR3, TDFR4, TDFR5, TDFR6, TDFR7 — **0x10002040, 0x10002050, 0x10002060, 0x10002070, 0x10002080, 0x10002090, 0x100020A0, 0x100020B0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TDFR															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

1.3.3 Timer Data HALF Register (TDHR)

The comparison data HALF registers TDHR is used to store the data to be compared with the content of the up-counter TCNT. This register can be directly read and written. (Default: indeterminate)

TDHR0, TDHR1, TDHR2, TDHR3, TDHR4, TDHR5, TDHR6, TDHR7																0x10002044, 0x10002054, 0x10002064, 0x10002074, 0x10002084, 0x10002094, 0x100020A4, 0x100020B4
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TDHR															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

1.3.4 Timer Counter (TCNT)

TCNT is a 16-bit read/write register. The up-counter TCNT can be reset to 0 by software and counts up using the prescaler output clock. When TCNT count up to equal to TDFR, it will reset to 0 and continue to count up. The data can be read out at any time. The counter data can be written at any time. This makes it possible to change the interrupt and/or clock output cycles temporarily. (Default: indeterminate)

TCNT0, TCNT1, TCNT2, TCNT3, TCNT4, TCNT5, TCNT6, TCNT7																0x10002048, 0x10002058, 0x10002068, 0x10002078, 0x10002088, 0x10002098, 0x100020A8, 0x100020B8
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCNT															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

1.3.5 Timer Counter Enable Register (TER)

The TER is an 8-bit read-only register. It contains the counter enable control bits for each channel. It is initialized to 0x00 by any reset. It can only be set by register TESR and TECR. Since the timer enable control bits are located in the same addresses, two or more timers can be started at the same time.

TER								0x10002010
Bit	7	6	5	4	3	2	1	0
	TCEN 7	TCEN 6	TCEN 5	TCEN 4	TCEN 3	TCEN 2	TCEN 1	TCEN 0
RST	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7	TCEN 7	Enable the counter in timer 7. 1: Begin counting up	R

		0: Stop counting up	
6	TCEN 6	Enable the counter in timer 6. 1: Begin counting up 0: Stop counting up	R
5	TCEN 5	Enable the counter in timer 5. 1: Begin counting up 0: Stop counting up	R
4	TCEN 4	Enable the counter in timer 4. 1: Begin counting up 0: Stop counting up	R
3	TCEN 3	Enable the counter in timer 3. 1: Begin counting up 0: Stop counting up	R
2	TCEN 2	Enable the counter in timer 2. 1: Begin counting up 0: Stop counting up	R
1	TCEN 1	Enable the counter in timer 1. 1: Begin counting up 0: Stop counting up	R
0	TCEN 0	Enable the counter in timer 0. 1: Begin counting up 0: Stop counting up	R

1.3.6 Timer Counter Enable Set Register (TESR)

The TCCSR is an 8-bit write-only register. It contains the counter enable set bits for each channel. Since the timer enable control set bits are located in the same addresses, two or more timers can be started at the same time.

TESR **0x10002014**

Bit	7	6	5	4	3	2	1	0
	TCST 7	TCST 6	TCST 5	TCST 4	TCST 3	TCST 2	TCST 1	TCST 0
RST	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
7	TCST 7	Set TCEN 7 bit of TER. 1: Set TCEN 7 bit to 1 0: Ignore	W
6	TCST 6	Set TCEN 6 bit of TER. 1: Set TCEN 6 bit to 1	W

		0: Ignore	
5	TCST 5	Set TCEN 5 bit of TER. 1: Set TCEN 5 bit to 1 0: Ignore	W
4	TCST 4	Set TCEN 4 bit of TER. 1: Set TCEN 4 bit to 1 0: Ignore	W
3	TCST 3	Set TCEN 3 bit of TER. 1: Set TCEN 3 bit to 1 0: Ignore	W
2	TCST 2	Set TCEN 2 bit of TER. 1: Set TCEN 2 bit to 1 0: Ignore	W
1	TCST 1	Set TCEN 1 bit of TER. 1: Set TCEN 1 bit to 1 0: Ignore	W
0	TCST 0	Set TCEN 0 bit of TER. 1: Set TCEN 0 bit to 1 0: Ignore	W

1.3.7 Timer Counter Enable Clear Register (TECR)

The TECR is an 8-bit write-only register. It contains the counter enable clear bits for each channel. Since the timer enable clear bits are located in the same addresses, two or more timers can be stop at the same time.

TECR **0x10002018**

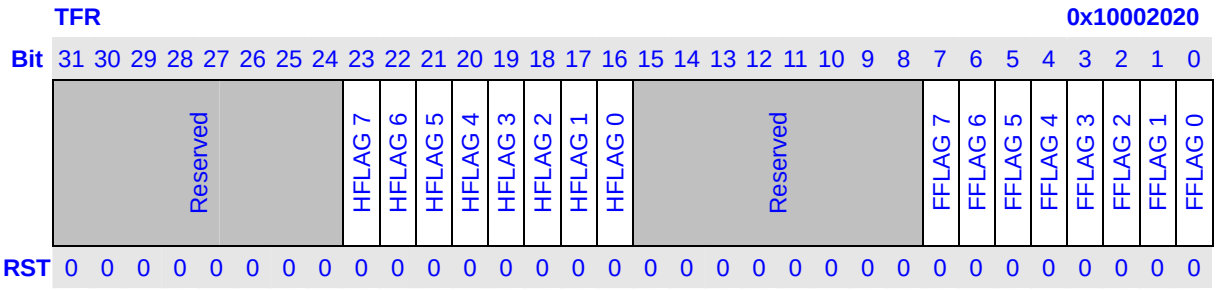
Bit	7	6	5	4	3	2	1	0
	TCCL 7	TCCL 6	TCCL 5	TCCL 4	TCCL 3	TCCL 2	TCCL 1	TCCL 0
RST	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
7	TCCL 7	Set TCEN 7 bit of TER. 1: Set TCEN 7 bit to 0 0: Ignore	W
6	TCCL 6	Set TCEN 6 bit of TER. 1: Set TCEN 6 bit to 0 0: Ignore	W
5	TCCL 5	Set TCEN 5 bit of TER. 1: Set TCEN 5 bit to 0 0: Ignore	W

4	TCCL 4	Set TCEN 4 bit of TER. 1: Set TCEN 4 bit to 0 0: Ignore	W
3	TCCL 3	Set TCEN 3 bit of TER. 1: Set TCEN 3 bit to 0 0: Ignore	W
2	TCCL 2	Set TCEN 2 bit of TER. 1: Set TCEN 2 bit to 0 0: Ignore	W
1	TCCL 1	Set TCEN 1 bit of TER. 1: Set TCEN 1 bit to 0 0: Ignore	W
0	TCCL 0	Set TCEN 0 bit of TER. 1: Set TCEN 0 bit to 0 0: Ignore	W

1.3.8 Timer Flag Register (TFR)

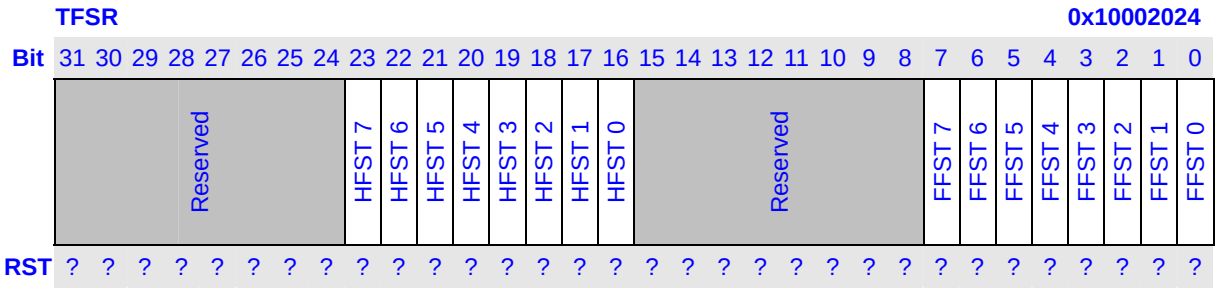
The TFR is a 32-bit read-only register. It contains the comparison match flag bits for all the channels. It can also be set by register TFSR and TFCR. It is initialized to 0x00000000 by any reset.



Bits	Name	Description	RW
31:24	Reserved	These bits always read 0, and written are ignored.	R
23:16	HFLAG 7~0	HALF comparison match flag. (TCNT = TDHR) 1: Comparison match 0: Comparison not match	R
15:8	Reserved	These bits always read 0, and written are ignored.	R
7:0	FFLAG 7~0	FULL comparison match flag. (TCNT = TDFR) 1: Comparison match 0: Comparison not match	R

1.3.9 Timer Flag Set Register (TFSR)

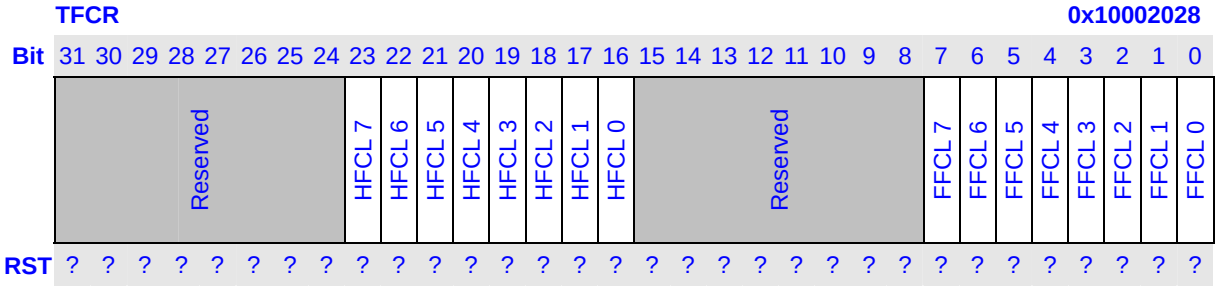
The TFSR is a 32-bit write-only register. It contains the comparison match flag set bits for all the channels.



Bits	Name	Description	RW
31:22	Reserved	-	-
23:16	HFST 7~0	Set HFLAG n bit of TFR. 1: Set HFLAG n bit to 1 0: Ignore	W
15:8	Reserved	-	-
7:0	FFST 7~0	Set FFLAG n bit of TFR. 1: Set FFLAG n bit to 1 0: Ignore	W

1.3.10 Timer Flag Clear Register (TFCR)

The TFCR is a 32-bit write-only register. It contains the comparison match flag clear bits for all the channels.



Bits	Name	Description	RW
31:24	Reserved	-	-
23:16	HFCL 7~0	Set HFLAG n bit of TFR. 1: Set FFLAG n bit to 0 0: Ignore	W
15:8	Reserved	-	-

7:0	FFCL 7~0	Set FFLAG n bit of TFR. 1: Set FFLAG n bit to 0 0: Ignore	W

1.3.11 Timer Mast Register (TMR)

The TMR is a 32-bit read-only register. It contains the comparison match flag bits for all the channels. It is initialized to 0x00000000 by any reset. It can only be set by register TMSR and TMCR.

TMR **0x10002030**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								HMASK 7	HMASK 6	HMASK 5	HMASK 4	HMASK 3	HMASK 2	HMASK 1	HMASK 0	Reserved								FMASK 7	FMASK 6	FMASK 5	FMASK 4	FMASK 3	FMASK 2	FMASK 1	FMASK 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:24	Reserved	These bits always read 0, and written are ignored.	R
23:16	HMASK 7~0	HALF comparison match interrupt mask. 1: Comparison match interrupt mask 0: Comparison match interrupt not mask	R
15:8	Reserved	These bits always read 0, and written are ignored.	R
7:0	FMASK 7~0	FULL comparison match interrupt mask. 1: Comparison match interrupt mask 0: Comparison match interrupt not mask	R

1.3.12 Timer Mask Set Register (TMSR)

The TMSR is a 32-bit write-only register. It contains the comparison match flag set bits for all the channels.

TMSR **0x10002034**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								HFST 7	HFST 6	HFST 5	HFST 4	HFST 3	HFST 2	HFST 1	HFST 0	Reserved								FFST 7	FFST 6	FFST 5	FFST 4	FFST 3	FFST 2	FFST 1	FFST 0
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:24	Reserved	-	-

23:16	HMST 7~0	Set HMASK n bit of TMR. 1: Set HMASK n bit to 1 0: Ignore	W
15:8	Reserved	-	-
7:0	FMST 7~0	Set FMASK n bit of TMR. 1: Set FMASK n bit to 1 0: Ignore	W

1.3.13 Timer Mask Clear Register (TMCR)

The TMCR is a 32-bit write-only register. It contains the comparison match flag clear bits for all the channels.

TMCR **0x10002038**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								HFCL 7	HFCL 6	HFCL 5	HFCL 4	HFCL 3	HFCL 2	HFCL 1	HFCL 0	Reserved								FFCL 7	FFCL 6	FFCL 5	FFCL 4	FFCL 3	FFCL 2	FFCL 1	FFCL 0
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:24	Reserved	-	-
25:16	HMCL 7~0	Set HMASK n bit of TMR. 1: Set HMASK n bit to 0 0: Ignore	W
15:8	Reserved	-	-
7:0	FMCL 7~0	Set FMASK n bit of TMR. 1: Set FMASK n bit to 0 0: Ignore	W

1.3.14 Timer Stop Register (TSR)

The TSR is a 32-bit read-only register. It contains the timer stop control bits for each channel and WDT timer. It is initialized to 0x00000000 by any reset. It can only be set by register TSSR and TSCR. If set, clock supplies to timer n / WDT timer is stopped, and registers of the timer/WDT cannot be accessed also.

TSR 0x1000201C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															WDTS	Reserved								STOP 7	STOP 6	STOP 5	STOP 4	STOP 3	STOP 2	STOP 1	STOP 0
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:17	Reserved	These bits always read 0, and written are ignored.	R
16	WDTS	1: The clock supplies to WDT is stopped. 0: The clock supplies to WDT is supplied.	R
15:8	Reserved	These bits always read 0, and written are ignored.	R
7	STOP 7	1: The clock supplies to timer 7 is stopped. 0: The clock supplies to timer 7 is supplied.	R
6	STOP 6	1: The clock supplies to timer 6 is stopped. 0: The clock supplies to timer 6 is supplied.	R
5	STOP 5	1: The clock supplies to timer 5 is stopped. 0: The clock supplies to timer 5 is supplied.	R
4	STOP 4	1: The clock supplies to timer 4 is stopped. 0: The clock supplies to timer 4 is supplied.	R
3	STOP 3	1: The clock supplies to timer 3 is stopped. 0: The clock supplies to timer 3 is supplied.	R
2	STOP 2	1: The clock supplies to timer 2 is stopped. 0: The clock supplies to timer 2 is supplied.	R
1	STOP 1	1: The clock supplies to timer 1 is stopped. 0: The clock supplies to timer 1 is supplied.	R
0	STOP 0	1: The clock supplies to timer 0 is stopped. 0: The clock supplies to timer 0 is supplied.	R

1.3.15 Timer Stop Set Register (TSSR)

The TCSR is an 8-bit write-only register. It contains the timer stop set bits for each channel and WDT timer. Since the timer stop control set bits are located in the same addresses, two or more timers can be started at the same time.

TSSR **0x1000202C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															WDTSS	Reserved								STPS 7	STPS 6	STPS 5	STPS 4	STPS 3	STPS 2	STPS 1	STPS 0
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:17	Reserved	-	-
16	WDTSS	Set WDTS bit of TSR. 1: Set WDTS bit to 1 0: Ignore	W
15:8	Reserved	-	-
7	STPS 7	Set STOP 7 bit of TSR. 1: Set STOP 7 bit to 1 0: Ignore	W
6	STPS 6	Set STOP 6 bit of TSR. 1: Set STOP 6 bit to 1 0: Ignore	W
5	STPS 5	Set STOP 5 bit of TSR. 1: Set STOP 5 bit to 1 0: Ignore	W
4	STPS 4	Set STOP 4 bit of TSR. 1: Set STOP 4 bit to 1 0: Ignore	W
3	STPS 3	Set STOP 3 bit of TSR. 1: Set STOP 3 bit to 1 0: Ignore	W
2	STPS 2	Set STOP 2 bit of TSR. 1: Set STOP 2 bit to 1 0: Ignore	W
1	STPS 1	Set STOP 1 bit of SR. 1: Set STOP 1 bit to 1 0: Ignore	W
0	STPS 0	Set STOP 0 bit of TSR. 1: Set STOP 0 bit to 1 0: Ignore	W

1.3.16 Timer Stop Clear Register (TSCR)

The TSCR is an 8-bit write-only register. It contains the timer stop clear bits for each channel and WDT timer. Since the timer stop clear bits are located in the same addresses, two or more timers can be stop at the same time.

TSCR **0x1000203C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															WDTSC	Reserved								STPC 7	STPC 6	STPC 5	STPC 4	STPC 3	STPC 2	STPC 1	STPC 0
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:17	Reserved	-	-
16	WDTSC	Set WDTS bit of TSR. 1: Set WDTS bit to 0 0: Ignore	W
15:8	Reserved	-	-
7	STPC 7	Set STOP 7 bit of TSR. 1: Set STOP 7 bit to 0 0: Ignore	W
6	STPC 6	Set STOP 6 bit of TSR. 1: Set STOP 6 bit to 0 0: Ignore	W
5	STPC 5	Set STOP 5 bit of TSR. 1: Set STOP 5 bit to 0 0: Ignore	W
4	STPC 4	Set STOP 4 bit of TSR. 1: Set STOP 4 bit to 0 0: Ignore	W
3	STPC 3	Set STOP 3 bit of TSR. 1: Set STOP 3 bit to 0 0: Ignore	W
2	STPC 2	Set STOP 2 bit of TSR. 1: Set STOP 2 bit to 0 0: Ignore	W
1	STPC 1	Set STOP 1 bit of TSR. 1: Set STOP 1 bit to 0 0: Ignore	W

0	STPC 0	Set STOP 0 bit of TSR. 1: Set STOP 0 bit to 0 0: Ignore	W

1.4 Operation

1.4.1 Basic Operation

The value of TDFR should be bigger than TDHR, and the minimum settings are TDHR = 0 and TDFR = 1. In this case, the timer output clock cycle is the input clock × 1/2. If TDHR > TDFR, no comparison TFHR signal is generated.

Before the timer counter begin to count up, we need to do as follows:
If you want to use PWM you should keep TCSR.PWM_EN to be 0 before you initial TCU.

1. Setting TCSR.
   (1) Writing TCSR.INITL to initialize PWM output level.
   (2) Writing TCSR.SD to setting the shutdown mode (Abrupt shutdown or Graceful shutdown).
   (3) Writing TCSR.PRESCALE to set TCNT count clock frequency.

2. Setting TCNT, TDHR and TDFR.

3. Setting TCSR.
   (1) Writing TCSR.PWM_EN to set whether enable PWM or disable PWM.
   (2) Writing TCSR.EXT_EN, TCSR.RTC_EN or TCSR.PCK_EN to 1 to select the input clock and enable the input clock. Only one of TCSR.EXT_EN, TCSR.RTC_EN and TCSR.PCK_EN can be set to 1.

After initialize the register of timer, we should start the counter as follows:

4. Setting the TESR.TCST bit to 1 to enable the TCNT.

Note: The input clock and PCLK should follows the rules advanced before.

1.4.2 Disable and Shutdown Operation

Setting the TECR.TCCL bit to 1 to disable the TCNT.

1.4.3 Pulse Width Modulator (PWM)

Timer 0~7 can be used as Pulse Width Modulator (PWM). The PWM can be used to control the back light inverter or adjust bright or contrast of LCD panel.

FULL comparison match signal and HALF comparison match signal can determine an attribute of the PWM_OUT waveform. FULL comparison match signal specifies the clock cycle for the PWM module clock. HALF comparison match signal specifies the duty ratio for the PWM module clock.