1 Real-Time Clock (RTC)

1.1 Overview

The Real-Time Clock (RTC) unit can be operated in either chip main power is on or the main power is down but the RTC power is still on. In this case, the RTC power domain consumes only a few micro watts power.

The RTC contains a 32768Hz oscillator, a power-on-reset generator, the real time and alarm logic, and the power down and wakeup control logic

1.1.1 Features

RTC module has following features:

- Embedded 32768Hz oscillator for 32k clock generation with an external 32k crystal
- 60ms power on reset, generated in RTC VDD power on procedure
- 32-bits second counter
- Programmable and adjustable counter to generate accurate 1 Hz clock
- Alarm interrupt, 1Hz interrupt
- Stand alone power supply, work in hibernating mode
- Power down controller
- External pin wakeup with up to 2s glitch filter / alarm wakeup

1.1.2 Signal Descriptions

RTC has 5 signal IO pins and 1 power pin. They are listed and described in.

Pin Names	Pin Loc	IO	IO Cell Char.	Pin Description	Power
RTCLK		AI	32768Hz	RTCLK: 32768 clock input or OSC input	VDD_{RTC}
RTCLKO		AO		RTCLKO: OSC output	VDD_{RTC}
PWRON_		AO	~2mA, Open-Draw	PWRON_: Power on/off control of main power	VDD_{RTC}
WKUP_ PD29		AI AI	Schmitt	WKUP_: Wake signal after main power down PD29: GPIO group D bit 29, input/interrupt only	VDD_{RTC}
PPRST_		AI	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDD_{RTC}
VDDRTC		P		VDDRTC: 3.3V power for RTC and hibernating mode controlling that never power down	-

- **RTCLK/RTCLKO** pins. We have an embedded oscillator for 32768Hz crystal. These two pins are the crystal XTALI and XTALO connection pins. If an input clock is used instead, please input it to RTCLKO pin.

- **PWRON**_ pin: this pin is used to control the main power on/off. Output low voltage means on and high-Z means off.
- **WKUP**_ pin: hibernating mode wakeup input
- **PPRST**_ pin: This pin should be set to low voltage only in two cases
  (1) When RTC power is turned on (so that whole chip is power on)
  (2) A RESET-KEY is pressed
  Don't set this pin to low voltage when wakeup from hibernating mode.

1.2 Register Description

Table 1-1 Registers for real time clock

Name	Description	RW	Reset Value	Address	Access Size
RTCCR	RTC Control Register	RW	0x00000081	0x10003000	32
RTCSR	RTC Second Register	RW	0x????????	0x10003004	32
RTCSAR	RTC Second Alarm Register	RW	0x????????	0x10003008	32
RTCGR	RTC Regulator Register	RW	0x00007FFF	0x1000300C	32

Table 1-2 Registers for hibernating mode

Name	Description	RW	Reset Value	Address	Access Size
HCR	Hibernate Control Register	RW	0x00000000	0x10003020	32
HWFCR	Wakeup filter counter Register in Hibernate mode	RW	0x0000????	0x10003024	32
HRCR	Hibernate reset counter Register in Hibernate mode	RW	0x00000???	0x10003028	32
HWCR	Wakeup control Register in Hibernate mode	RW	0x00000000	0x1000302C	32
HWRSR	Wakeup Status Register in Hibernate mode	RW	0x00000000	0x10003030	32
HSPR	Scratch pattern register	RW	0x????????	0x10003034	32

All these registers, include those for real time clock and for hibernating mode control, except otherwise stated, are implemented in 32k clock domain. When write to these registers, it needs about 35 ~ 65 us to actually change the register's value and allow the next write access. A bit RTCCR.WRDY is used to indicate it. When RCR.WRDY is 1, it means the previous write is finished, a right value can be read from the target register, and a new write access can be issued. So before any write access, please make sure RCR.WRDY = 1.

1.2.1 RTC Control Register (RTCCR)

RTCCR contains bits to configure the real time clock features. This register is initialized by RTC power on reset only. Reset pin reset (pp-reset), hibernating reset and WDT reset do not change its value.

RTCCR 0x10003000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								WRDY	1HZ	1HZIE	AF	AIE	AE	Reserved	RTCE
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1

Bits	Name	Description	RW
31:7	Reserved	Writes to these bits have no effect and always read as 0	R
7	WRDY	Write ready flag. It is 0 when a write is currently processing and the value has not been written to the writing target register. No write to any RTC registers can be issued in this case, or the result is undefined. The read value from the target register is also undefined. The reading is meaningful and an another write can be issued when it is 1. Please reference to descriptions in 1.2 for some more details. This bit is read only and write to it is ignored.	R
6	1HZ	1Hz flag. This bit is set by hardware once every 1 second through the 1Hz pulse if the real time clock is enabled (RTCCR.RTCE = 1). This bit can be cleared by software. Write 1 to this bit is ignored. Writing to this bit takes effect immediately without delay.	RW
5	1HZIE	1Hz interrupt enable. Writing to this bit takes effect immediately without delay. **1HZIE** / **Description** 0 / 1Hz interrupt is disabled 1 / 1Hz interrupt is enabled. RTC issues interrupt when 1HZ bit is set	RW
4	AF	Alarm flag. This bit is set by hardware when alarm match (RTCSR = RTCSAR) is found and alarm is enabled (RTCCR.AE = 1) and the real time clock is enabled (RTCCR.RTCE = 1). This bit can be cleared by software. Write 1 to this bit is ignored. Writing to this bit takes effect immediately.	RW
3	AIE	Alarm interrupt enable. **AIE** / **Description** 0 / Alarm interrupt is disabled 1 / Alarm interrupt is enabled. RTC issues interrupt when AF is set	RW
2	AE	Alarm enable.	RW

		AE	**Description**	
		0	Alarm function is disabled	
		1	Alarm function is enabled	
1	Reserved	Writes to these bits have no effect and always read as 0		R
0	RTCE	Real time clock enable.		RW
		RTCE	**Description**	
		0	Real time clock function is disabled	
		1	Real time clock function is enabled	

1.2.2 RTC Second Register (RTCSR)

RTCSR is a 32-bit width second counter. It can be read and write by software. It is increased by 1 at every 1Hz pulse if the real time clock is enabled (RTCCR.RTCE = 1). When read, it should be read continued more than once and take the value if the adjacent results are the same. RTCSR is not initialized by any reset.

RTCSR **0x10003004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RTCSR																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

1.2.3 RTC Second Alarm Register (RTCSAR)

RTCSAR serves as a second alarm register. Alarm flag (RTCCR.AF) is set to 1 when the RTCSR equals the RTCSAR in the condition of alarm is enabled (RTCCR.AE = 1) and the real time clock is enabled (RTCCR.RTCE = 1). RTCSAR can be read and write by software and is not initialized by any reset.

RTCSAR **0x10003008**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RTCSAR																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

1.2.4 RTC Regulator Register (RTCGR)

RTCGR is serves as the real time clock regulator, which is used to adjust the interval of the 1Hz pulse.

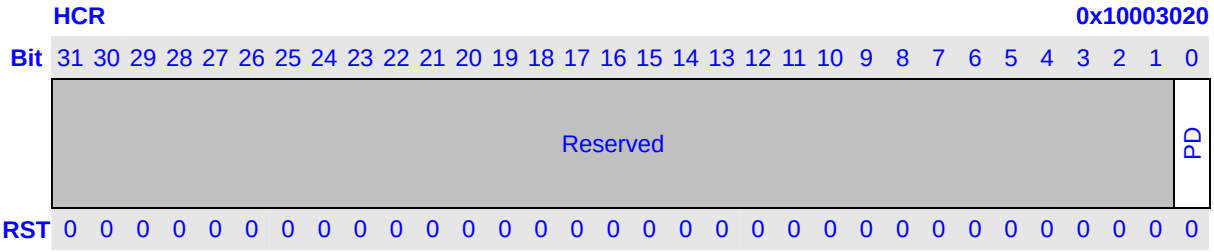
RTCGR 0x1000300C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LOCK	Reserved															ADJC														NC1HZ			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31	LOCK	Lock bit. This bit is used to safeguard the validity of the data written into the RTCGR register. Once it is set, write to RTCGR is ignored. This bit can only be set by software and cleared by (any type of) resets. LOCK: 0 – Write to RTCGR is allowed; 1 – Write to RTCGR is forbidden	RW
30:26	Reserved	Writes to these bits have no effect and always read as 0	R
25:16	ADJC	This field specifies how many times it needs to add one 32kHz cycle for the 1Hz pulse interval in every 1024 1Hz pulses. In other word, among every 1024 1Hz pulses, ADJC number of them are trigged in every (NC1HZ + 2) 32kHz clock cycles, (1024 – ADJC) number of them are trigged in every (NC1HZ + 1) 32kHz clock cycles.	RW
15:0	NC1HZ	This field specifies the number plus 1 of the working 32kHz clock cycles are contained in the 1Hz pulse interval. In other word, 1Hz pulse is trigged every (NC1HZ + 1) 32kHz clock cycles, if RTCGR.ADJC = 0	RW

1.2.5 Hibernate Control Register (HCR)

HCR contains the bit to control the main chip power on/off. This register is reset by any reset.



Bits	Name	Description	RW
31:1	Reserved	Writes to these bits have no effect and always read as 0	R
0	PD	Power down or power on bit. This bit controls the PWRON_ pin level. When co-working with some external components, this bit is used for power management of this chip with. It is supposed when 1 is written to this bit, the main power supply of the chip, except RTC power, will be shut down immediately. After this bit is set to 1, all registers in RTC module, except RTCCR.1HZ and RTCCR.1HZIE, cannot be changed by write access. In addition, reset pin reset and WDT reset are also ignored by RTC in this case. This bit is cleared by RTC power on reset and hibernating reset. The later one is asserted by wakeup procedure.	RW

PD	PWRON_	Description
0	0 V	No power down, keep power on
1	VDDRTC	Power down enable, turn power off

1.2.6 HIBERNATE mode Wakeup Filter Counter Register (HWFCR)

The HIBERNATE mode Wakeup Filter Counter Register (HWFCR) is a 32-bit read/write register .It filter the glitch generated by a dedicated wakeup pin. The HWFCR is initialized by power on and wdt reset.

HWFCR **0x10003024**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																HWFCR											Reserved					
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	0

Bits	Name	Description	RW
31:16	Reserved	Writes to these bits have no effect and always read as 0	R
15:5	HWFCR	Wakeup pin level effective minimum time in number of 32 RTCLK cycles, used as debounce filter logic. Maximum 2 seconds	RW
4:0	Reserved	Writes to these bits have no effect and always read as 0	R

1.2.7 Hibernate Reset Counter Register (HRCR)

The Hibernate Reset Counter Register is a 32-bit read/write register that specifies hibernate reset assertion time. The HRCR is initialized by power on and wdt reset

HRCR **0x10003028**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																				HRCR								Reserved			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description	RW
31:12	Reserved	Writes to these bits have no effect and always read as 0	R
11:5	HRCR	HIBERNATE Reset waiting time. Number of 32 RTCLK cycles. Maximum 125 ms	RW
4:0	Reserved	Writes to these bits have no effect and always read as 0	R

1.2.8 HIBERNATE Wakeup Control Register (HWCR)

The HIBERNATE Wakeup Control Register is a 32-bit read/write register that controls wake up source , wake up enable, wakeup level trigger bits. The HWCR is initialized to 0x00000000 by poweron and WDT reset.

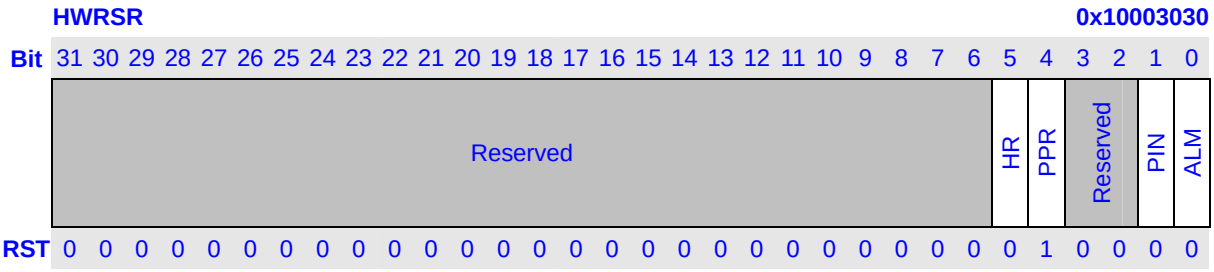
HWCR **0x1000302C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														EPIN	EALM
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:2	Reserved	Writes to these bits have no effect and always read as 0	R
1	EPIN	Wakeup pin wakeup enable 0: disable 1: enable	RW
0	EALM	RTC Alarm wakeup enable 0: disable 1: enable	RW

1.2.9 HIBERNATE Wakeup Status Register (HWRSR)

The HIBERNATE Wakeup Status Register is a 32-bit read/write register that reflects wakeup status bits. The HWRSR is initialized to 0x00000000 by power-on and WDT reset.



Bits	Name	Description	RW
31:6	Reserved	Writes to these bits have no effect and always read as 0	R
5	HR	Hibernate Reset. When a Hibernate reset detected, HR is set and remains set until software clears it or another reset occurs. This bit can only be written with 0. Write with 1 is ignored 0: Hibernate reset has not occurred since the last time the software clears this bit 1: Hibernate reset has occurred since the last time the software clears this bit	RW
4	PPR	PPR reset 0: PPRST_ reset has not occurred since last time the software clears this bit 1: PPRST_ reset has occurred since last time the software clears this bit	RW
3:2	Reserved	Writes to these bits have no effect and always read as 0	R
1	PIN	Wakeup Pin Status bit. The bit is set when level is detect of wakeup pin. The bit can be cleared by software. Set 1 to the bit has no effect. 0: HIBERNATE mode is not waken up due to level detect on wakeup pin 1: HIBERNATE mode is waken up due to level detect on wakeup pin	RW
0	ALM	RTC Alarm Status bit. The bit is set when RTC Alarm occurs. The bit can be cleared by software. Set 1 to the bit has no effect. 0: HIBERNATE mode is not waken up due to RTC Alarm 1: HIBERNATE mode is waken up due to RTC Alarm	RW

1.2.10 Hibernate Scratch Pattern Register (HSPR)

This is a scratch register used to hold a pattern. The software can check the pattern is kept to know whether RTC power has ever been down and whether it is needed to setup the real time clock.

HSPR **0x10003034**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAT																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	RW
31:0	PAT	The pattern	RW

1.3 Time Regulation

Because of the inherent inaccuracy of crystal and other variables, the time counter may be inaccurate. This requires a slight adjustment. The application processor, through the RTCGR, lets you adjust the 1Hz time base to an error of less than 1ppm. Such that if the Hz clock were set to be 1Hz, there would be an error of less than 5 seconds per month.

To determine the value programmed into the RTCGR, you must first measure the output frequency at the oscillator multiplex (approximately 32 kHz) using an accurate time base, such as a frequency counter. This clock is externally visible by selecting the alternate function of GPIO[?]
To gain access to the clock, program this pin as an output and then switch to the alternate function. To trim the clock, divide the output of the oscillator by an integer value and fractional adjust it by periodically deleting clocks from the stream driving this integer divider.

After the true frequency of the oscillator is known, it must be split into integer and fractional portions. The integer portion of the value (minus one) is loaded into the DIV field of the RTCGR.

The fractional part of the adjustment is done by periodically deleting clocks from the clock stream driving the Hz divider. The trim interval period is hardwired to be 1024 1Hz clock cycles (approximately 17 minutes). The number of clocks (represented by ADC field of RTCGR) are deleted from the input clock stream per trim interval. If ADC is programmed to be zero, then no trim operations occur and the RTC is clocked with the raw 32 kHz clock. The relationship between the Hz clock frequency and the nominal 32 kHz clock (f1 and f32K, respectively) is shown in the following equation.

$$f1 = \frac{2^{10} \times (DIV + 1)}{2^{10} \times (DIV + 1) + ADC} \times \frac{f32k}{DIV + 1}$$

f1 = actual frequency of 1Hz clock
f32k = frequency of either 32.768KHz crystal output or 3.6864MHz crystal output further divided down to 32.914KHz

1.3.1 HIBERNATE Mode

When Software writes 1 to PD bit of HCR, the system at once enters HIBERNATE mode. The powers of CORE and IO are disconnected by PWRON_ pin, no power consumption to core and IO. When a wakeup event occurs, the core enters through a hibernate reset. Only CPM wake up logic and RTC is operating in HIBERNATE mode.

1.3.1.1 Procedure to Enter HIBERNATE mode

Before enter HIBERNATE mode, software must complete following steps:

- Finish the current operation and preserve all data to flash
- Configure the wake-up sources properly by configure HWCSR
- Set HIBERNATE MODE (Set PD bit in HCR to 1.)

1.3.1.2 Procedure to Wake-up from HIBERNATE mode

- The internal hibernate reset signal will be asserted if one of the wake-up sources is issued.
- Check RSR to determine what caused the reset
- Check PIN/ALM bits of HWCSR in order to know whether or not the power-up is caused by which wake-up from HIBERNATE mode.
- Configure the SDRAM memory controller.
- Recover the data from flash