1 LCD Controller

1.1 Overview

The JZ integrated LCD controller has the capabilities to driving the latest industry standard STN and TFT LCD panels. It also supports some special TFT panels used in consuming electronic products. The controller performs the basic memory based frame buffer and palette buffer to LCD panel data transfer through use of a dedicated DMA controller. Temporal dithering (frame rate modulation) is supported for STN LCD panels.

Features:

(1) Basic Features:

- Support ITU601/656 data format.
- Single and Dual panel displays in STN mode.
- Single panel displays in TFT mode.
- Display size up to 800x600.
- Internal palette RAM 256x16 bits.

(2) Colors Supports:

- Encoded pixel data of 1, 2, 4, 8 or 16 BPP in STN mode.
- Support 2, 4, 16 grayscales and up to 4096 colors in STN mode.
- Encoded pixel data of 1, 2, 4, 8, 16, 18 or 24 BPP in TFT mode.
- Support 65,536(65K), 262,144(260K) and up to 16,777,216 (16M) colors in TFT mode.

(3) Panel Supports:

- Support 1, 2, 4, 8 data output pins in STN mode.
- Support 8-bit serial data output for 1bpp, 2bpp, 4bpp, 8bpp, 16bpp, 18bpp and 24bpp in TFT mode.
- Support 16-bit parallel data output for 1bpp, 2bpp, 4bpp, 8bpp and 16bpp in TFT mode.
- Support 18-bit parallel data output for 1bpp, 2bpp, 4bpp, 8bpp, 16bpp, 18bpp and 24bpp in TFT mode.

1.2 Pin Description

Table 1-1 LCD Controller Pins Description

Name	I/O	Description
Lcd_pclk	Input/Output	Display device pixel clock
Lcd_vsync	Input/Output	Display device vertical synchronize pulse
Lcd_hsync	Input/Output	Display device horizontal synchronize pulse
Lcd_de	Output	Display device is STN: AC BIAS Pin Display device is NOT STN: data enable Pin
Lcd_d[17:0]	Output	Display device data pins
Lcd_spl*[1]	Output	Programmable special pin for generating control signals
Lcd_cls*[1]	Output	Programmable special pin for generating control signals
Lcd_ps*[1]	Output	Programmable special pin for generating control signals
Lcd_rev*[1]	Output	Programmable special pin for generating control signals

Note1:

The mode and timing of special pin Lcd_spl, Lcd_cls, Lcd_ps and Lcd_rev can be seen in **part 1.7 LCD Controller Pin Mapping.**

1.3 Block Diagram

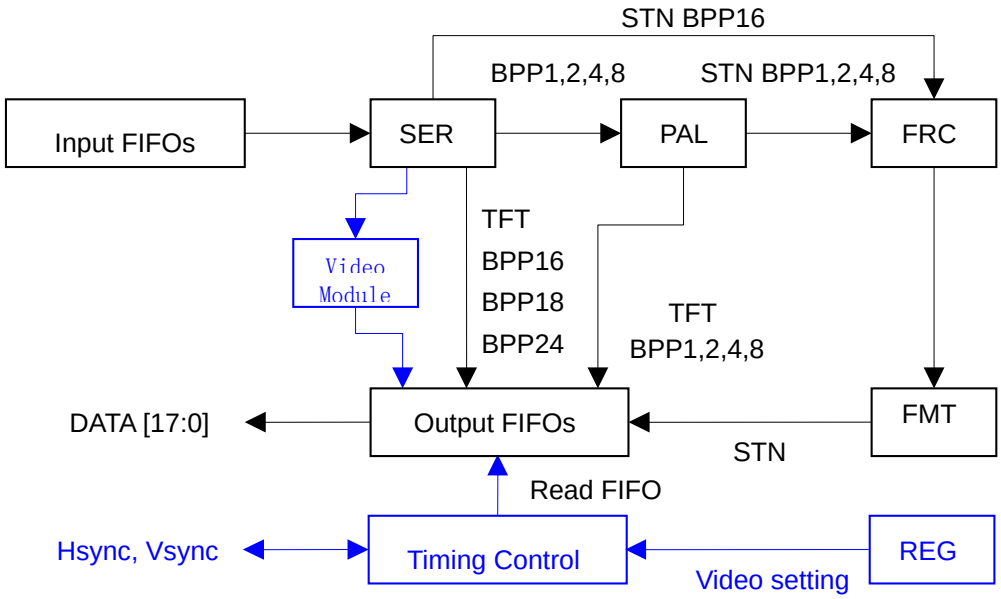


Figure 1-1 Block Diagram

1.4 LCD Display Timing

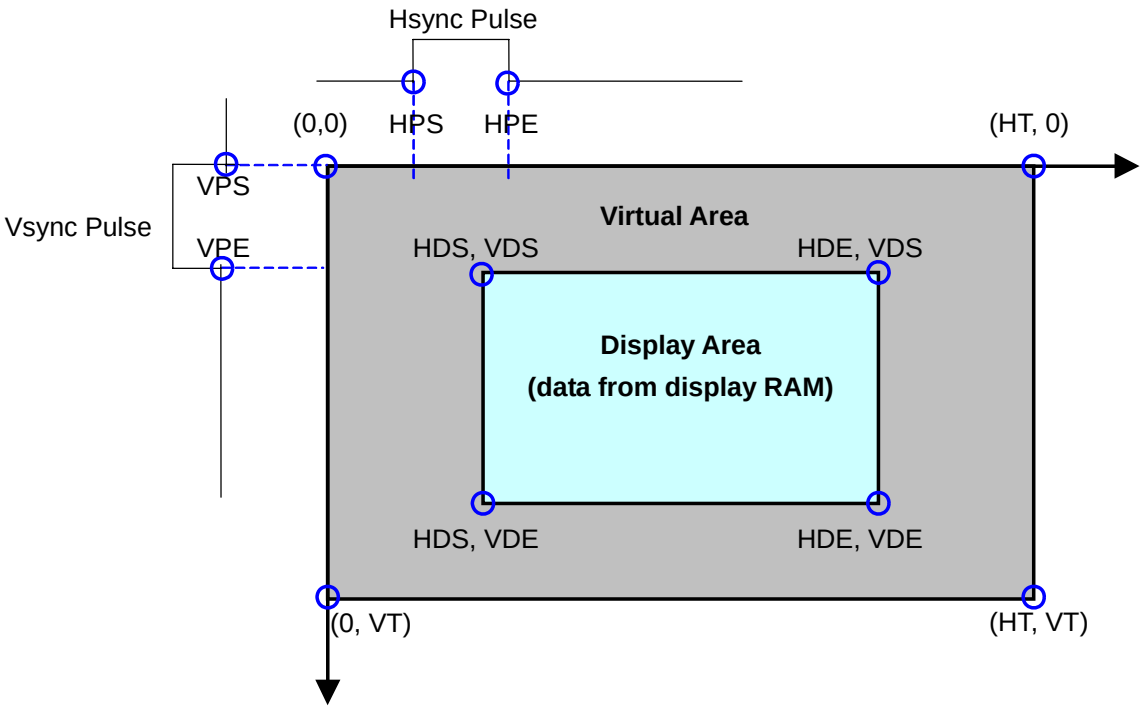


Figure 1-2 Display Parameters

Note1:

VPS === 0

VSYNC pulse always start at point (0,0)

Note2:

H: Horizontal V: Vertical T: Total

D: Display Area P: Pulse

S: Start point E: End point

In the (H, V) Coordinates:

1. The gray rectangle (0, 0) to (HT, VT) is “Virtual Area”;
2. The blue rectangle (HDS, VDS) to (HDE, VDE) is “Display Area”;
3. VPS, VPE defines the VSYNC signal timing; (VPS always be zero)
4. HPS, HPE defines the HSYNC signal timing;

All timing parameters start with “H” is measured in lcd_pclk ticks.
All timing parameters start with “V” is measured in lcd_hsync ticks.

This diagram describes the general LCD panel parameters, these can be set via the registers that describes in next section.

1.5 TV Encoder Timing

Some of Video Encoders for TV (Tele Vision) require interlaced timing interface.

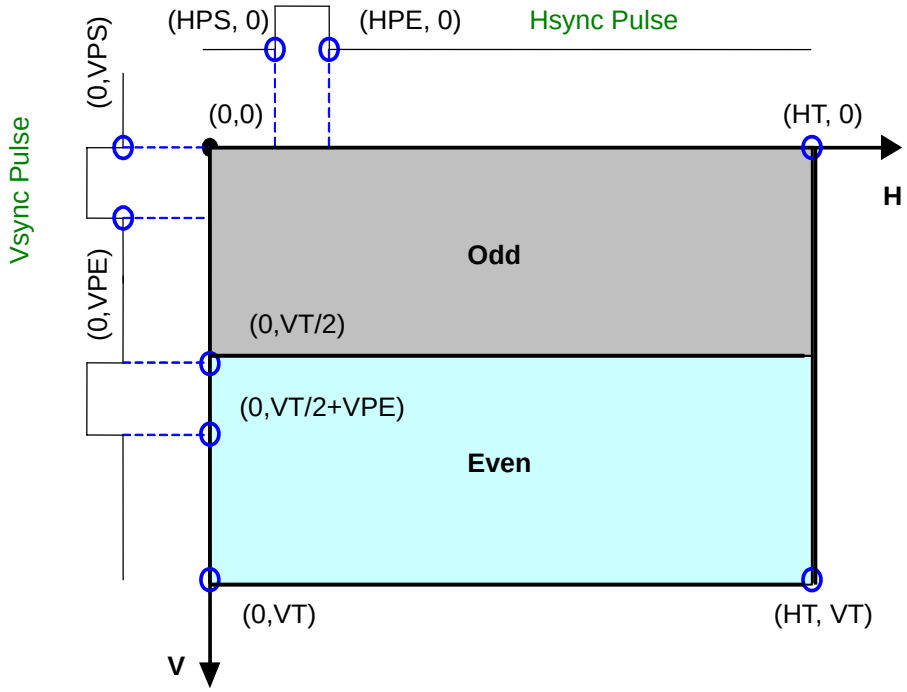


Figure 1-2 TV-Encoder Display Parameters

Note1:

Even Field contains one more blank line.

e.g. For standard PAL timing, Odd filed has 312 lines while even field has 313 lines.

Note2:

Interlace mode generate 2 vsync pulse for each field. The second vsync start at (VT/2), end at (VT/2 + VPE)

Note3:

Display Area & Virtual Area has the same size. VDS=HDS=0, VDE=VT, HDE=HT

1.6 Register Description

Table 1-2 LCD Controller Registers Description

Name	RW	Reset Value	Address	Access Size
LCDCFG	RW	0x00000000	0x13050000	32
LCDVSYNC	RW	0x00000000	0x13050004	32
LCDHSYNC	RW	0x00000000	0x13050008	32
LCDVAT	RW	0x00000000	0x1305000C	32
LCDDAH	RW	0x00000000	0x13050010	32
LCDDAV	RW	0x00000000	0x13050014	32
LCDPS*1	RW	0x00000000	0x13050018	32
LCDCLS*1	RW	0x00000000	0x1305001C	32
LCDSPL*1	RW	0x00000000	0x13050020	32
LCDREV*1	RW	0x00000000	0x13050024	32
LCDCTRL	RW	0x00000000	0x13050030	32
LCDSTATE	RW	0x00000000	0x13050034	32
LCDIID	R	0x00000000	0x13050038	32
LCDDA0	RW	0x00000000	0x13050040	32
LCDSA0	R	0x00000000	0x13050044	32
LCDFID0	R	0x00000000	0x13050048	32
LCDCMD0	R	0x00000000	0x1305004C	32
LCDDA1*2	RW	0x00000000	0x13050050	32
LCDSA1*2	R	0x00000000	0x13050054	32
LCDFID1*2	R	0x00000000	0x13050058	32
LCDCMD1*2	R	0x00000000	0x1305005C	32

Note: *1: These registers are only used for SPECIAL TFT panels.

*2: These registers are only used for Dual Panel STN panels.

1.6.1 Configure Register (LCDCFG)

LCDCFG **0x13050000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCDPIN	Reserved							PSM	CLSM	SPLM	REVM	HSYNM	PCLKM	INVDAT	SYNDIR	PSP	CLSP	SPLP	REVP	HSP	PCP	DEP	VSP	18/16	Reserved	PDW		MODE			
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31	LCDPIN[*1]	LCD PIN Select bit. These two bits are used to choose the function of LCD PINS or SLCD PINS. The function of pins is as follows: **LCDPIN** / **PIN SELECT** 0 / LCD PIN 1 / SLCD PIN	RW
30:24	Reserved	These bits always read 0, and written are ignored.	R
23	PSM	PS signal mode bit: 1 – disabled, 0 – enabled.	RW
22	CLSM	CLS signal mode bit: 1 – disabled, 0 – enabled.	RW
21	SPLM	SPL signal mode bit: 1 – disabled, 0 – enabled.	RW
20	REVM	REV signal mode bit: 1 – disabled, 0 – enabled.	RW
19	HSYNM	H-Sync signal polarity choice function: 1 – disabled, 0 – enabled.	RW
18	PCLKM	Dot clock signal polarity choice function: 1 – disabled, 0 – enabled.	RW
17	INVDAT	Inverse output data: 0 – normal, 1 – inverse.	RW
16	SYNDIR	V-Sync and H-Sync direction: 0 – output, 1 – input.	RW
15	PSP	PS pin reset state	RW
14	CLSP	CLS pin reset state	RW
13	SPLP	SPL pin reset state	RW
12	REVP	REV pin reset state	RW
11	HSP	H-Sync polarity: 0 – active high, 1 – active low	RW
10	PCP	Pix-clock polarity: 0 – data translations at rising edge. 1 – data translations at falling edge.	RW
9	DEP	Data Enable polarity: 0 – active high, 1 – active low	RW
8	VSP	V-Sync polarity: 0 – leading edge is rising edge. 1 – leading edge is falling edge.	RW
7	18/16	18-bit TFT Panel or 16-bit TFT Panel. This bit will be available when MODE [3:2] is equal to 0, 0 - 16-bit TFT Panel. 1 - 18-bit TFT Panel.	RW

<table>
<tr><td>6</td><td>Reserved</td><td>These bits always read 0, and written are ignored.</td><td>R</td></tr>
<tr><td>5:4</td><td>PDW</td><td>STN pins utilization
<table>
<tr><th></th><th>Signal Panel</th></tr>
<tr><td>00</td><td>Lcd_d[0]</td></tr>
<tr><td>01</td><td>Lcd_d[0:1]</td></tr>
<tr><td>10</td><td>Lcd_d[0:3]</td></tr>
<tr><td>11</td><td>Lcd_d[0:7]</td></tr>
<tr><th></th><th>Dual-Monochrome Panel</th></tr>
<tr><td>00</td><td>Reserved</td></tr>
<tr><td>01</td><td>Reserved</td></tr>
<tr><td>10</td><td>Upper panel: lcd_d[3:0], lower panel: lcd_d[11:8]</td></tr>
<tr><td>11</td><td>Upper panel: lcd_d[7:0], lower panel: lcd_d[15:8]</td></tr>
</table></td><td>RW</td></tr>
<tr><td>3:0</td><td>MODE</td><td>Display Device Mode Select
<table>
<tr><th></th><th>LCD Panel</th></tr>
<tr><td>0000</td><td>Generic 16-bit/18-bit Parallel TFT Panel</td></tr>
<tr><td>0001</td><td>Special TFT Panel Mode1</td></tr>
<tr><td>0010</td><td>Special TFT Panel Mode2</td></tr>
<tr><td>0011</td><td>Special TFT Panel Mode3</td></tr>
<tr><td>0100</td><td>Non-Interlaced CCIR656</td></tr>
<tr><td>0101</td><td>Reserved</td></tr>
<tr><td>0110</td><td>Interlaced CCIR656</td></tr>
<tr><td>0111</td><td>Reserved</td></tr>
<tr><td>1000</td><td>Single-Color STN Panel</td></tr>
<tr><td>1001</td><td>Single-Monochrome STN Panel</td></tr>
<tr><td>1010</td><td>Dual-Color STN Panel</td></tr>
<tr><td>1011</td><td>Dual-Monochrome STN Panel</td></tr>
<tr><td>1100</td><td>8-bit Serial TFT</td></tr>
<tr><td>1101</td><td>Reserved</td></tr>
<tr><td>1110</td><td>Reserved</td></tr>
<tr><td>1111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
</table>

Note[*1]

LCDPIN	PIN25	PIN24	PIN23	PIN22	PIN21	PIN20	PIN19	PIN18	PIN17-0
0	LCD PCLK	LCD VSYNC	LCD HSYNC	LCD DE	LCD REV	LCD PS	LCD CLS	LCD SPL	LCD D [17:0]
1	SLCD CLK	SLCD CS	SLCD RS						SLCD D [17:0]

The direction of PIN25 is set by register LPCDR.LCS in CPM SPEC.

The direction of PIN23 and PIN23 are set by register LCDCFG.SYNDIR

1.6.2 Vertical Synchronize Register (LCDVSYNC)

LCDVSYNC **0x13050004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					VPS											Reserved					VPE										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	These bits always read 0, and written are ignored.	R
26:16	VPS	V-Sync Pulse start position, fixed to 0 (in line clock)	R
15:11	Reserved	These bits always read 0, and written are ignored.	R
10:0	VPE	V-Sync Pulse end position (in line clock)	RW

1.6.3 Horizontal Synchronize Register (LCDHSYNC)

LCDHSYNC **0x13050008**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					HPS											Reserved					HPE										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	These bits always read 0, and written are ignored.	R
26:16	HPS	H-Sync pulse start position (in dot clock)	RW
15:11	Reserved	These bits always read 0, and written are ignored.	R
10:0	HPE	H-Sync pulse end position (in dot clock)	RW

1.6.4 Virtual Area Setting (LCDVAT)

LCDVAT **0x1305000C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					HT											Reserved					VT										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	These bits always read 0, and written are ignored.	R
26:16	HT	Horizontal Total size (in dot clock, sum of display area and blank space)	RW
15:11	Reserved	These bits always read 0, and written are ignored.	R
10:0	VT	Vertical Total size (in line clock, sum of display area and blank space)	RW

1.6.5 Display Area Horizontal Start/End Point (LCDDAH)

LCDDAH **0x13050010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					HDS											Reserved					HDE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	These bits always read 0, and written are ignored.	R
26:16	HDS	Horizontal display area start (in dot clock)	RW
15:11	Reserved	These bits always read 0, and written are ignored.	R
10:0	HDE	Horizontal display area end (in dot clock)	RW

1.6.6 Display Area Vertical Start/End Point (LCDDAV)

LCDDAV **0x13050014**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					VDS											Reserved					VDE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	These bits always read 0, and written are ignored.	R
26:16	VDS	Vertical display area start position (in line clock)	RW
15:11	Reserved	These bits always read 0, and written are ignored.	R
10:0	VDE	Vertical display area end position (in line clock)	RW

1.6.7 PS Signal Setting (LCDPS)

LCDPS **0x13050018**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					PSS											Reserved					PSE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	These bits always read 0, and written are ignored.	R
26:16	PSS	PS signal start position (in dot clock). In STN mode, PS signal is ignored. But this register is used to define the AC BIAs signal. AC BIAs signal will toggle very N lines per frame. PSS defines the Toggle position.	RW
15:11	Reserved	These bits always read 0, and written are ignored.	R
10:0	PSE	PS signal end position (in dot clock). In STN mode, PSE defines N, which described in PSS.	RW

1.6.8 CLS Signal Setting (LCDCLS)

LCDCLS **0x1305001C**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					CLSS											Reserved					CLSE											
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	These bits always read 0, and written are ignored.	R
26:16	CLSS	CLS signal start position (in dot clock)	RW
15:11	Reserved	These bits always read 0, and written are ignored.	R
10:0	CLSE	CLS signal end position (in dot clock)	RW

1.6.9 SPL Signal Setting (LCDSPL)

LCDSPL **0x13050020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					SPLS											Reserved					SPLE										
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	These bits always read 0, and written are ignored.	R
26:16	SPLS	SPL signal start position (in dot clock)	RW
15:11	Reserved	These bits always read 0, and written are ignored.	R
10:0	SPLE	SPL signal end position (in dot clock)	RW

1.6.10 REV Signal Setting (LCDREV)

LCDREV **0x13050024**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					REVS											Reserved															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:27	Reserved	These bits always read 0, and written are ignored.	R
26:16	REVS	REV signal start position (in dot clock)	RW
15:0	Reserved	These bits always read 0, and written are ignored.	R

1.6.11 Control Register (LCDCTRL)

LCDCTRL **0x13050030**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		BST		RGB	OFUP		FRC					PDD				Reserved		EOFM	SOFM	OFUM	IFUM0	IFUM1	LDDM	QDM	BEDN	PEDN	DIS	ENA		BPP	
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th><th>RW</th></tr>
<tr><td>31:30</td><td>Reserved</td><td>These bits always read 0, and written are ignored.</td><td>R</td></tr>
<tr><td>29:28</td><td>BST</td><td>Burst Length Selection
<table>
<tr><th></th><th>Burst Length</th></tr>
<tr><td>00</td><td>4 word</td></tr>
<tr><td>01</td><td>8 word</td></tr>
<tr><td>10</td><td>16 word</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>27</td><td>RGB</td><td>RGB mode: 0 – RGB565, 1 – RGB555.</td><td>RW</td></tr>
<tr><td>26</td><td>OFUP</td><td>Output FIFO under run protection: 0 – disable, 1 – enable.</td><td>RW</td></tr>
<tr><td>25:24</td><td>FRC</td><td>STN FRC Algorithm Selection
<table>
<tr><th></th><th>Grayscale</th></tr>
<tr><td>00</td><td>16 grayscale</td></tr>
<tr><td>01</td><td>4 grayscale</td></tr>
<tr><td>10</td><td>2 grayscale</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
<tr><td>23:16</td><td>PDD</td><td>Load Palette Delay Counter</td><td>RW</td></tr>
<tr><td>15:14</td><td>Reserved</td><td>These bits always read 0, and written are ignored.</td><td>R</td></tr>
<tr><td>13</td><td>EOFM</td><td>Mask end of frame interrupt: 0 – enabled, 1 – masked</td><td>RW</td></tr>
<tr><td>12</td><td>SOFM</td><td>Mask start of frame interrupt: 0 – enabled, 1 – masked</td><td>RW</td></tr>
<tr><td>11</td><td>OFUM</td><td>Mask out FIFO under run interrupt: 0 – enabled, 1 – masked</td><td>RW</td></tr>
<tr><td>10</td><td>IFUM0</td><td>Mask in FIFO 0 under run interrupt: 0 – enabled, 1 – masked</td><td>RW</td></tr>
<tr><td>9</td><td>IFUM1</td><td>Mask in FIFO 1 under run interrupt: 0 – enabled, 1 – masked</td><td>RW</td></tr>
<tr><td>8</td><td>LDDM</td><td>Mask LCD disable done interrupt: 0 – enabled, 1 – masked</td><td>RW</td></tr>
<tr><td>7</td><td>QDM</td><td>Mask LCD quick disable done interrupt: 0 – enabled, 1 – masked</td><td>RW</td></tr>
<tr><td>6</td><td>BEDN</td><td>Endian selection: 0 – same as system Endian, 1 – reverse endian format</td><td>RW</td></tr>
<tr><td>5</td><td>PEDN</td><td>Endian in byte: 0 – msb first, 1 – lsb first</td><td>RW</td></tr>
<tr><td>4</td><td>DIS</td><td>Disable controller indicate bit: 0 – enable, 1 – in disabling or disabled</td><td>RW</td></tr>
<tr><td>3</td><td>ENA</td><td>Enable controller: 0 – disable, 1 – enable</td><td>W</td></tr>
<tr><td>2:0</td><td>BPP</td><td>Bits Per Pixel
<table>
<tr><th></th><th>Bits Per Pixel</th></tr>
<tr><td>000</td><td>1 bpp</td></tr>
<tr><td>001</td><td>2 bpp</td></tr>
<tr><td>010</td><td>4 bpp</td></tr>
<tr><td>011</td><td>8 bpp</td></tr>
<tr><td>100</td><td>15/16 bpp</td></tr>
<tr><td>101</td><td>18 bpp/24bpp</td></tr>
<tr><td>110</td><td>Reserved</td></tr>
<tr><td>111</td><td>Reserved</td></tr>
</table></td><td>RW</td></tr>
</table>

1.6.12 Status Register (LCDSTATE)

LCDSTATE																										0x13050034							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																									QD	Reserved	EOF	SOF	OUF	IFU0	IFU1	LDD
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
7	QD	LCD Quick disable: 0 – not been quick disabled, 1 – quick disabled done.	RW
6	Reserved	These bits always read 0, and written are ignored.	R
5	EOF	End of Frame indicate bit.	RW
4	SOF	Start of Frame indicate bit.	RW
3	OUF	Out FIFO under run.	RW
2	IFU0	In FIFO 0 under run.	RW
1	IFU1	In FIFO 1 under run.	RW
0	LDD	LCD disable: 0 – not been normal disabled, 1 – been normal disabled	RW

1.6.13 Interrupt ID Register (LCDIID)

LCDIID is a read-only register that contains a copy of the Frame ID register (LCDFID) from the descriptor currently being processed when a start of frame (SOF) or end of frame (EOF) interrupt is generated. LCDIID is written to only when an unmasked interrupt of the above type is signaled and there are no other unmasked interrupts in the LCD controller pending. As such, the register is considered to be sticky and will be overwritten only when the signaled interrupt is cleared by writing the LCD controller status register. For dual-panel displays, LCDIID is written only when both channels have reached a given state.

LCDIID is written with the last channel to reach that state. (i.e. LCDFID of the last channel to reach SOF would be written in LCDIID if SOF interrupts are enabled). Reserved bits must be written with zeros and reads from them must be ignored.

LCDIID																																0x13050038	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IID																																
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	IID	A copy of Frame ID register, which transferred from Descriptor.	RW

1.6.14 Descriptor Address Register0, 1 (LCDDA0, 1)

A frame descriptor is a 4-word block, aligned on 4-word (16-byte) boundary, in external memory:

WORD [0] contains the physical address for next LCDDAx
WORD [1] contains the physical address for LCDSAx
WORD [2] contains the value for LCDFIDx
WORD [3] contains the value for LCDCMDx

Software must write the physical address of the first descriptor to LCDDAx before enabling the LCD Controller. Once the LCD Controller is enabled, the first descriptor is read, and all 4 registers are written by the DMAC. The next frame descriptor pointed to by LCDDAx is loaded into the registers for the associated DMA channel after all data for the current descriptor has been transferred.

Note: If only one frame buffer is used in external memory, the LCDDAx field (word [0] of the frame descriptor) must point back to itself. That is to say, the value of LCDDAx is the physical address of itself.

Read/write registers LCDDA0 and LCDDA1, corresponding to DMA channels 0 and 1, contain the physical address of the next descriptor in external memory. The DMAC fetches the descriptor at this location after finishing the current descriptor. On reset, the bits in this register are zero. The target address must be aligned to 16-byte boundary. Bits [3:0] of the address must be zero.

LCDDA0, LCDDA1 **0x13050040, 0x13050050**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DA0, 1																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	DA0, 1	Next descriptor physical address. And descriptor structure as following: WORD [0]: next descriptor physical address. WORD [1]: the buffer physical address. WORD [2]: the buffer ID value. (Only for debug) WORD [3]: the buffer property. The value is same as LCDCMD.	RW

1.6.15 Source Address Register0, 1 (LCDSA0, 1)

Registers LCDSA0 and LCDSA1, corresponding to DMA channels 0 and 1, contain the **physical** address of frame buffer or palette buffer in external memory. The address must be aligned on an 4, 8, or 16 word boundary according to register LCDCTRL .BST. If this descriptor is for palette data, LCDSA0 points to the memory location of the palette buffer. If this descriptor is for frame data, LCDSAx points to the memory location of the frame buffer. This address is incremented by hardware as the DMAC fetches data from memory. If desired, the Frame ID Register can be used to hold the initial frame source address.

LCDSA0, LCDSA1 **0x13050044, 0x13050054**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SA0, 1																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	SA0, 1	Buffer start address. (Only for driver debug)	R

1.6.16 Frame ID Register0 (LCDFID0,1)

Registers LCDFID0 and LCDFID1, corresponding to DMA channels 0 and 1, contain an ID field that describes the current frame. The particular use of this field is up to the software. This ID register is copied to the LCD Controller Interrupt ID Register when an interrupt occurs.

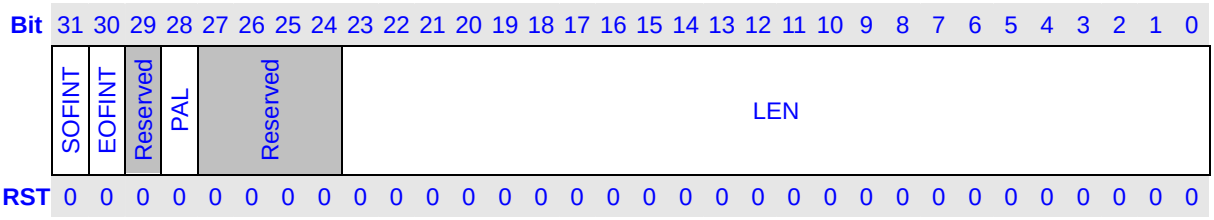
LCDFID0, LCDFID1 **0x13050048, 0x13050058**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FID0, 1																															
RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description	RW
31:0	FID0, 1	Frame ID. (Only for debug)	R

1.6.17 DMA Command Register0, 1 (LCDCMD0, 1)

LCDCMD0, LCDCMD1 **0x1305004C, 0x1305005C**



Bits	Name	Description	RW
31	SOFINT	Enable start of frame interrupt. When SOFINT =1, the DMAC sets the start of frame bit (LCDSTATE.SOF) when starting a new frame. The SOF bit is set after a new descriptor is loaded from memory and before the palette/frame data is fetched. In dual-panel mode, LCDSTATE.SOF is set only when both channels reach the start of frame and both frame descriptors have SOFINT set. SOFINT must not be set for palette descriptors in dual-panel mode, since only one channel is ever used to load the palette descriptor.	R
30	EOFINT	Enable end of frame interrupt. When EOFINT =1, the DMAC sets the end of frame bit (LCDSTATE.EOF) after fetching the last word in the frame buffer. In dual-panel mode, LCDSTATE.EOF is set only when both channels reach the end of frame and both frame descriptors have EOFINT set. EOFINT must not be set for palette descriptors in dual-panel mode, since only one channel is ever used to load the palette descriptor.	R
29	Reserved	These bits always read 0, and written are ignored.	R
28	PAL	The descriptor contains a palette buffer. PAL indicates that data being fetched will be loaded into the palette RAM. If PAL =1, the palette RAM data is loaded via DMA channel 0 as follows: In bpp1, 2, 4, 8 mode, software must load the palette at least once after enabling the LCD. In bpp16 mode, PAL must be 0.	R
27:24	Reserved	These bits always read 0, and written are ignored.	R
23:0	LEN	The buffer length value (in WORD). The LEN bit field determines the number of bytes of the buffer size pointed by LCDSAx. LEN = 0 is not valid. DMAC fetch data according to LEN. Each time one or more word(s) been fetched, LEN is increased automatically. Software can read LEN.	R

1.7 LCD Controller Pin Mapping

There are several mapping schemes for different LCD panels.

1.7.1 TFT and CCIR656 Pin Mapping

Pin	Generic 8-bit Serial TFT	Generic 18-bit Parallel TFT	Generic 16-bit Parallel TFT	Special TFT 1 16-bit Parallel	Special TFT 2 16-bit Parallel	Special TFT 3 16-bit Parallel	CCIR656 8-bit	CCIR656 16-bit
Lcd_pclk	CLK	CLK	CLK	DCLK	CLK	HCLK	CLK	CLK
Lcd_vsync	VSYNC	VSYNC	VSYNC	SPS	GSRT	STV	VSYNC	VSYNC
Lcd_hsync	HSYNC	HSYNC	HSYNC	LP	GPCK	STH	HSYNC	HSYNC
Lcd_de	DE	DE	DE	-	-	-	-	-
Lcd_ps	-	-	-	Pulse mode	Toggle mode	Toggle mode	-	-
Lcd_cls	-	-	-	Pulse mode	Pulse mode	Pulse mode	-	-
Lcd_rev	-	-	-	Toggle mode	Toggle mode	Toggle mode	-	-
Lcd_spl	-	-	-	Pulse mode	Pulse mode	**Toggle mode**	-	-
Lcd_dat17	-	R5	-	-	-	-	-	-
Lcd_dat16	-	R4	-	-	-	-	-	-
Lcd_dat15	-	R3	R5	R5	R5	R5	-	D15
Lcd_dat14	-	R2	R4	R4	R4	R4	-	D14
Lcd_dat13	-	R1	R3	R3	R3	R3	-	D13
Lcd_dat12	-	R0	R2	R2	R2	R2	-	D12
Lcd_dat11	-	G5	R1	R1	R1	R1	-	D11
Lcd_dat10	-	G4	G5	G5	G5	G5	-	D10
Lcd_dat9	-	G3	G4	G4	G4	G4	-	D9
Lcd_dat8	-	G2	G3	G3	G3	G3	-	D8
Lcd_dat7	R7/G7/B7	G1	G2	G2	G2	G2	D7	D7
Lcd_dat6	R6/G6/B6	G0	G1	G1	G1	G1	D6	D6
Lcd_dat5	R5/G5/B5	B5	G0	G0	G0	G0	D5	D5
Lcd_dat4	R4/G4/B4	B4	B5	B5	B5	B5	D4	D4
Lcd_dat3	R3/G3/B3	B3	B4	B4	B4	B4	D3	D3
Lcd_dat2	R2/G2/B2	B2	B3	B3	B3	B3	D2	D2
Lcd_dat1	R1/G1/B1	B1	B2	B2	B2	B2	D1	D1
Lcd_dat0	R0/G0/B0	B0	B1	B1	B1	B1	D0	D0

1.7.2 Single STN Pin Mapping

Pin	Color STN	Mono STN			
	PDW=3	PDW=0	PDW=1	PDW=2	PDW=3
Lcd_pclk	CLK	CLK	CLK	CLK	CLK
Lcd_vsync	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
Lcd_hsync	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
Lcd_de	BIAS	BIAS	BIAS	BIAS	BIAS
Lcd_ps	-	-	-	-	-
Lcd_cls	-	-	-	-	-
Lcd_rev	-	-	-	-	-
Lcd_spl	-	-	-	-	-
Lcd_dat17	-	-	-	-	-
Lcd_dat16	-	-	-	-	-
Lcd_dat15	-	-	-	-	-
Lcd_dat14	-	-	-	-	-
Lcd_dat13	-	-	-	-	-
Lcd_dat12	-	-	-	-	-
Lcd_dat11	-	-	-	-	-
Lcd_dat10	-	-	-	-	-
Lcd_dat9	-	-	-	-	-
Lcd_dat8	-	-	-	-	-
Lcd_dat7	D7	-	-	-	D7
Lcd_dat6	D6	-	-	-	D6
Lcd_dat5	D5	-	-	-	D5
Lcd_dat4	D4	-	-	-	D4
Lcd_dat3	D3	-	-	D3	D3
Lcd_dat2	D2	-	-	D2	D2
Lcd_dat1	D1	-	D1	D1	D1
Lcd_dat0	D0	D0	D0	D0	D0

1.7.3 Dual Panel STN Pin Mapping

Pin	Color STN	Mono STN			
	PDW=3	PDW=0	PDW=1	PDW=2	PDW=3
Lcd_pclk	CLK	-	-	CLK	CLK
Lcd_vsync	VSYNC	-	-	VSYNC	VSYNC
Lcd_hsync	HSYNC	-	-	HSYNC	HSYNC
Lcd_de	BIAS	-	-	BIAS	BIAS
Lcd_ps	-	-	-	-	-
Lcd_cls	-	-	-	-	-
Lcd_rev	-	-	-	-	-
Lcd_spl	-	-	-	-	-
Lcd_dat17	-	-	-	-	-
Lcd_dat16	-	-	-	-	-
Lcd_dat15	UD7	-	-	-	UD7
Lcd_dat14	UD6	-	-	-	UD6
Lcd_dat13	UD5	-	-	-	UD5
Lcd_dat12	UD4	-	-	-	UD4
Lcd_dat11	UD3	-	-	UD3	UD3
Lcd_dat10	UD2	-	-	UD2	UD2
Lcd_dat9	UD1	-	-	UD1	UD1
Lcd_dat8	UD0	-	-	UD0	UD0
Lcd_dat7	LD7	-	-	-	LD7
Lcd_dat6	LD6	-	-	-	LD6
Lcd_dat5	LD5	-	-	-	LD5
Lcd_dat4	LD4	-	-	-	LD4
Lcd_dat3	LD3	-	-	LD3	LD3
Lcd_dat2	LD2	-	-	LD2	LD2
Lcd_dat1	LD1	-	-	LD1	LD1
Lcd_dat0	LD0	-	-	LD0	LD0

1.8 Display Timing

1.8.1 General 16-bit and 18-bit TFT Timing

This section shows the general 16-bit and 18-bit TFT LCD timing diagram, the polarity of signal “Vsync”, “Hsync”, and “PCLK” can be programmed correspond to the LCD panel specification.

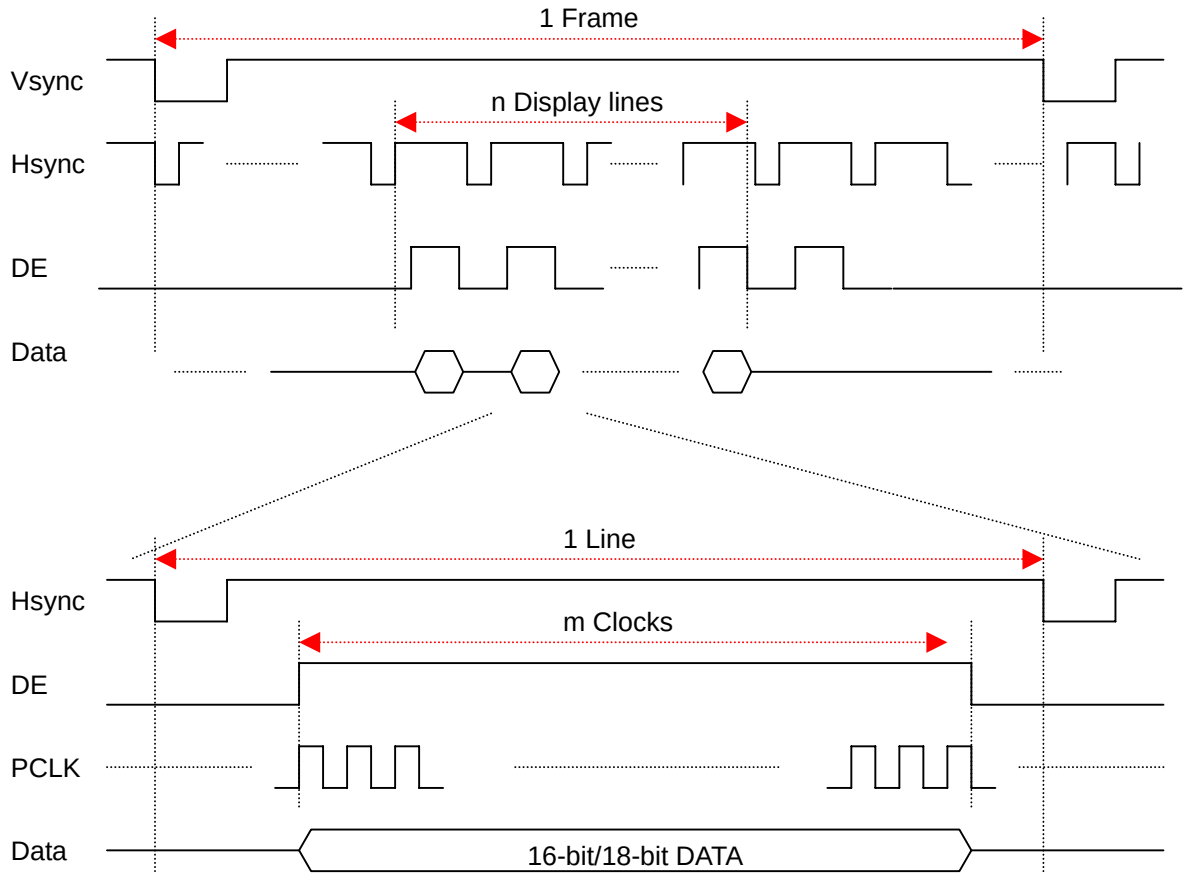


Figure 1-2 General 16-bit and 18-bit TFT LCD Timing

1.8.2 8-bit Serial TFT Timing

This section shows the 8-bit serial TFT LCD timing diagram, the polarity of signal “Vsync”, “Hsync”, and “PCLK” can be programmed correspond to the LCD panel specification.

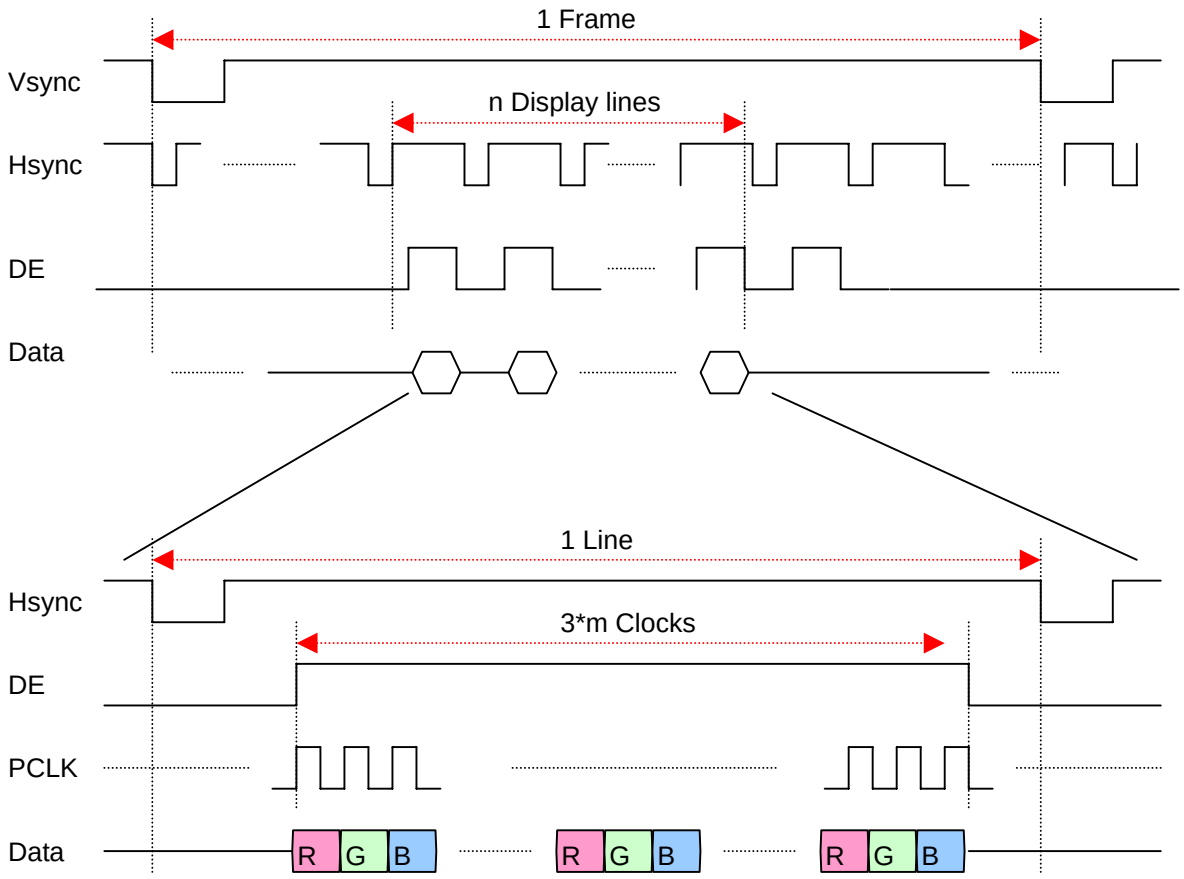


Figure 1-3 8-bit serial TFT LCD Timing (24bpp)

1.8.3 Special TFT Timing

Based on the general TFT LCD support, this controller also provides 4 special signals that can be programmed to general some special timing used for some panel. All 4 signals are worked in two modes: pulse mode and toggle mode. Signal “CLS” is fixed in pulse mode, and “REV” in toggle mode. The work mode of signals “SPL” and “PS” are defined in the special TFT LCD mode 1 to mode 3, either pulse mode or toggle mode. The position and polarity of these 4 signals can be programmed via registers. The Figures show the two modes as follows: (The toggle mode of signal “SPL” is different with the others signal. “SPL” does toggle after display line.)

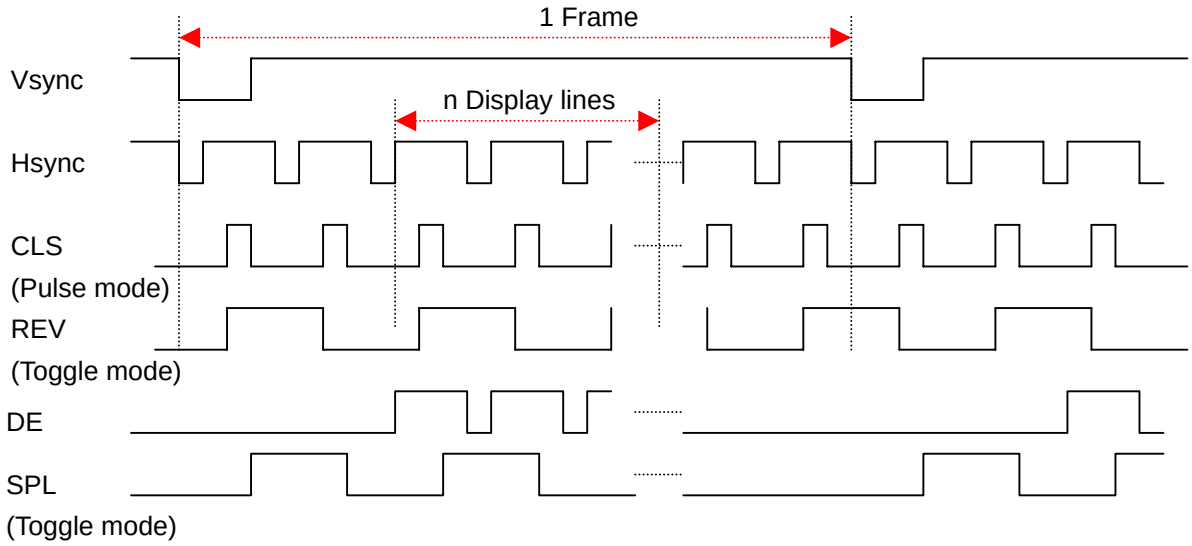


Figure 1-3 Special TFT LCD Timing 1

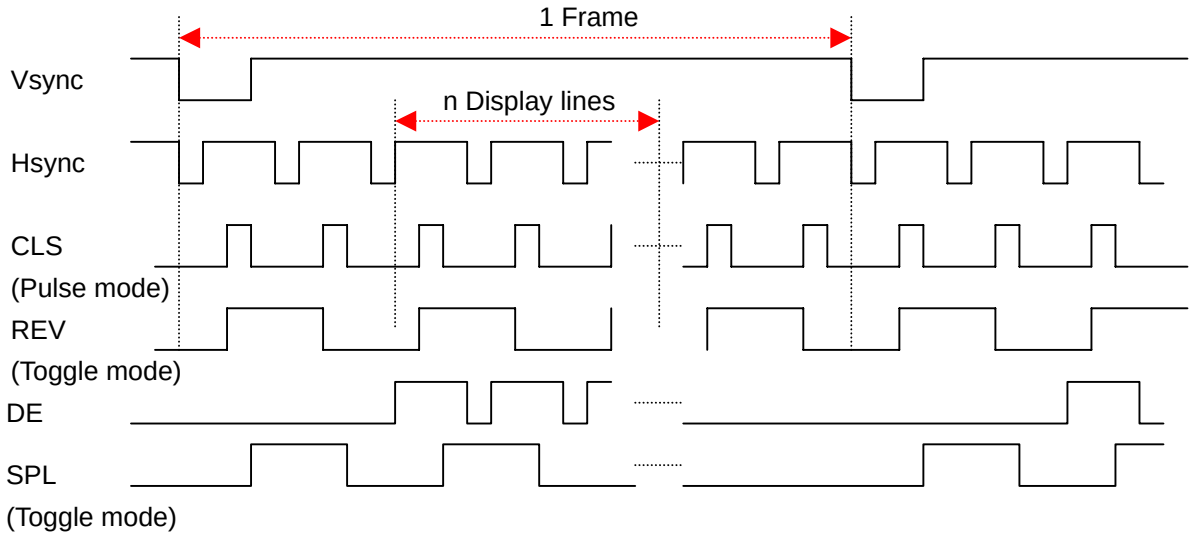


Figure 1-4 Special TFT LCD Timing 2

These two Figures show the timing of pulse mode and toggle mode, the pulse mode timing is same and the toggle mode timing is different. Timing 1 shows the condition when the total lines in 1 frame is odd (the number of display is even and the number of blank is odd), so the phase of REV inverse at the first line of each frame and the phase of SPL dose not inverse at the first line of each frame. Timing 2 shows the condition when the total lines in 1 frame is even (the number of display is even and the number of blank is even), so the phase of REV and SPL dose not inverse at the first line of each frame.

When LCDC is enabled ,there will be a null line to be add before transferring data to LCD panel. So the toggle mode exept SPL signal of special 3 TFT mode is when reset level is high,the first valid edge will be rising edge. SPL signal of special 3 TFT mode is when reset level is high,the first valid edge will be falling edge.

1.9 Format of Palette

This LCD controller contains a palette RAM with 256-entry x 16-bit used only for BPP8, BPP4, BPP2 and BPP1. Palette RAM data is loaded directly from the external memory palette buffer by DMAC channel 0. Each word of palette buffer contains 2 palette entries.

- In 8-bpp modes, palette buffer size is128 words.
- In 4-bpp modes, palette buffer size is 8 words.
- In 2-bpp modes, palette buffer size is 2 words.
- In 1-bpp modes, palette buffer size is 1 word.
- In 16/18/24-bpp modes, has no palette buffer.

Palette buffer base address	Bit: 31 . . . 16	Bit: 15 . . . 0
Palette entry	Entry-1 bit: 15 . . . 0	Entry-0 bit: 15 . . . 0
Palette buffer base address + 4	Bit: 31 . . . 16	Bit: 15 . . . 0
Palette entry	Entry-3 bit: 15 . . . 0	Entry-2 bit: 15 . . . 0
Palette buffer base address + 8	Bit: 31 . . . 16	Bit: 15 . . . 0
Palette entry	Entry-5 bit: 15 . . . 0	Entry-4 bit: 15 . . . 0

1.9.1 STN

For STN Panel, 16-bpp pixel data is encoded with RGB 565 or RGB 555.
Please refer to register LCDCTRL.RGB.

BPP 16, RGB 565, pixel encoding for STN Panel

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

BPP 16, RGB 555, pixel encoding for STN Panel

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

1.9.2 TFT

BPP 16, RGB 565, pixel encoding for TFT Panel

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

Note: For BPP 16, 18, 24, palette is bypass.

1.10 Format of Frame Buffer

1.10.1 16bpp

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

1.10.2 18bpp

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	R5	R4	R3	R2	R1	R0	0	0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G5	G4	G3	G2	G1	G0	0	0	B5	B4	B3	B2	B1	B0	0	0

1.10.3 24bpp

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	R7	R6	R5	R4	R3	R2	R1	R0
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

1.11 Format of Data Pin Utilization

1.11.1 Mono STN

In Mono STN mode, data pin pixel ordering of one LCD screen row. Column 0 is the first pixel of a screen row.

Upper panel								
Panel data width	**Col0**	**Col1**	**Col2**	**Col3**	**Col4**	**Col5**	**Col6**	**Col7**
1 bit	D0	D0	D0	D0	D0	D0	D0	D0
2 bit	D1	D0	D1	D0	D1	D0	D1	D0
4 bit	D3	D2	D1	D0	D3	D2	D1	D0
8 bit	D7	D6	D5	D4	D3	D2	D1	D0
Lower panel (dual-panel mode)								
4 bit	D11	D10	D9	D8	D11	D10	D9	D8
8 bit	D15	D14	D13	D12	D11	D10	D9	D8

1.11.2 Color STN

In Color STN mode, data pin pixel ordering of one LCD screen row. Column 0 is the first pixel of a screen row.

Upper panel							
Col0 (R)	**Col0 (G)**	**Col0 (B)**	**Col1 (R)**	**Col1 (G)**	**Col1 (B)**	**Col2 (R)**	**Col2 (G)**
D7	D6	D5	D4	D3	D2	D1	D0
Lower panel (dual-panel mode)							
D15	D14	D13	D12	D11	D10	D9	D8

1.11.3 18-bit Parallel TFT

Col0 (RGB)																	
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

1.11.4 16-bit Parallel TFT

Col0 (RGB)															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

1.11.5 8-bit Serial TFT (24bpp)

Col0 (R)							
D7	D6	D5	D4	D3	D2	D1	D0
Col0 (G)							
D7	D6	D5	D4	D3	D2	D1	D0
Col0 (B)							
D7	D6	D5	D4	D3	D2	D1	D0

1.12 LCD Controller Operation

1.12.1 Set LCD Controller Device Clock and Pixel Clock

The LCD Controller has 2 clock input: device clock and pixel clock. The both clocks are generated by CPM (Clock and Power Manager). The frequency of the 2 clocks can be set by CPM registers. CPM registers CPCCR.LDIV and CPCCR.PCS set LCD device clock division ratio, and LPCDR set LCD pixel clock division ratio. Please refer to CPM spec for detail.

LCD device clock is the LCD controller's internal clock while LCD pixel clock is output to drive LCD panel. There have 2 rules for LCD clocks:

(1) For TFT Panel, the frequency of LCD device clock must be at least 1.5 times of LCD pixel clock.
(2) For STN Panel, the frequency of LCD device clock must be at least 3 times of LCD pixel clock.

LCD panel determines the frequency of LCD pixel clock.

1.12.2 Enabling the Controller

If the LCD controller is being enabled for the first time after system reset or sleep reset, all of the LCD registers must be programmed as follows:

(1) Write the frame descriptors and, if needed, the palette descriptor to memory.

(2) Program the entire LCD configuration registers except the Frame Descriptor Address Registers (LCDDAx) and the LCD Controller enable bit (LCDCTRL.ENA).

(3) Program LCDDAx with the memory address of the palette/frame descriptor.

(4) Enable the LCD controller by writing to LCDCTRL.ENA.

If the LCD controller is being re-enabled, there has not been a reset since the last programming; only the registers LCDDAx and LCDCTRL.ENA need to be reprogrammed. The LCD Controller Status Register (LCDSTATE) must also be written to clear any old status flags before re-enabling the LCD controller.

Once the LCD controller has been enabled, do not write new values to LCD registers except LCDCTRL.ENA or DIS or LCDDA0/1.

1.12.3 Disabling the Controller

The LCD controller can be disabled in two ways: regular and quick.

(1) Regular disabling:
Regular disabling is accomplished by setting the disable bit, LCDCTRL.DIS. The other bits in LCDCTRL must not be changed — read the register, set the DIS bit, and rewrite the register. This method causes the LCD controller to stop cleanly at the end of a frame. The LCD Disable Done bit, LCDSTATE.LDD, is set when the LCD controller finishes displaying the last frame, and the enable bit, LCDCTRL.ENA, is cleared automatically by hardware.
LCDCTRL.DIS must be set zero when enabling the controller.

(2) Quick disabling:
Quick disabling is accomplished by clearing the enable bit, LCDCTRL.ENA. The LCD controller will finish any current DMA transfer, stop driving the panel, setting the LCD Quick Disable bit (LCDSTATE.QD) and shut down immediately. This method is intended for situations such as a battery fault, where system bus traffic has to be minimized immediately so the processor can have enough time to store critical data to memory before the loss of power. The LCD controller must not be re-enabled until the QD bit is set, indicating that the quick shutdown is complete. Do not set the DIS bit when a quick disabling command has been issued.

Note: It is strongly recommended that software set the “LCD Module Stop Bit” in PMC to shut down LCDC clock supply to save power consumption after disable LCDC. Please refer to PMC for detailed information.

1.12.4 Resetting the Controller

At reset, the LCD Controller is disabled. All LCD Controller Registers are reset to the conditions shown in the register descriptions.

1.12.5 Frame Buffer & Palette Buffer

The starting address of frame buffer stored in external memory must be aligned to 4, 8 or 16 words boundary according to register LCDCTRL.BST. The length of buffer must be multiple of word (32-bit).

If LCDCTRL .BST = 0, align frame and palette buffer to 16 word boundary
If LCDCTRL .BST = 1, align frame and palette buffer to 8 word boundary
If LCDCTRL .BST = 2, align frame and palette buffer to 4 word boundary

One frame buffer contains encoded pixel data of multiple of screen lines; each line of encoded pixel data must be aligned to word boundary. If the length of a line is not the multiple of word, extra bits must be applied to reach a word boundary. It is suggested that the extra bits to be set zero.