1 Overview

Jz4740 is a 32 Bits RISC processor targeting for handheld and general embedded applications. Incorporate the JzRISC core based on leading microarchitecture technology, this processor provides high integration, high performance and low power consumption solution for embedded device.

The JzRISC is the advanced and power-efficient 32-bit RISC core with 16K I-Cache and 16K D-Cache in this processor, operating at speeds up to 400MHz. On-chip modules such as LCD controller, AC97/I2S controller and camera interface offer designers a rich suite of peripherals for multimedia application. The memory interface supports a variety of memory types that allow flexible design requirements, include the glueless connection to NAND Flash for cost sensitive applications. WLAN, Bluetooth and expansion options are provided through the PCMCIA/CF, USB, and MMC/SD host controllers. And the other peripherals such as UART, SPI, and Ethernet controller as well as general-system resources provide enough compute and connectivity capability for many applications. For the processor block diagram, refer to .

1.1 Block Diagram

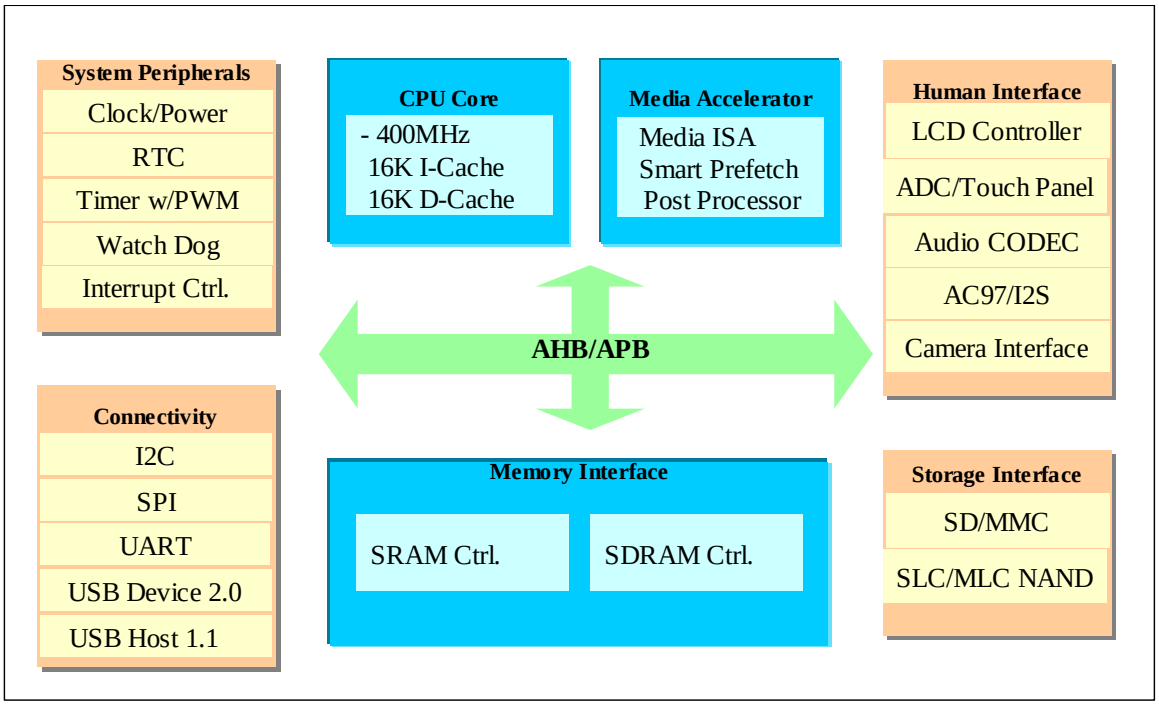

Figure 1-1 Jz4740 Diagram

1.2 Features

1.2.1 CPU Core

- 8-stage pipeline
- 16K I-Cache, 16K D-Cache
- 32-entry dual-pages joint-TLB, 4 entry Instruction TLB and 4 entry data TLB
- With SIMD/DSP unit to support media accelerattion extension instructions
- With smart prefect to accelerate media applications

1.2.2 Vedio post processing (CSC and resize)

- Vedio frame resize
- 420/444/422 YUV to RGB convert
- DMA memory access

1.2.3 Memory sub-system

EMC (External Memory Controller)

- Support ROM, burst ROM, SRAM, NOR flash maximum size of 128kB
- NAND flash and boot supported, 8/16-bit, 512+16 or 2048+64 page size, 2 or 3 cycle page address, hardware ECC supported
- MLC NAND flash supported
- 16-bit or 32-bit SDRAM data bus
- SDRAM chip
- SDRAM burst operation, page mode, auto-refresh and self-refresh functions

DMAC (Direct Memory Access Controller)

- 6 channels DDMA (descibed DMA)
- one transfer unit: 8-bit, 16-bit, 32-bit, 16-byte, 32-byte
- on-chip and auto-request
- act as AHB-APB bridge

1.2.4 System Peripherals

GPIO (General Purpose Input/Output)

- 124 gpio pins
- each pin can be configured to function, input, interrupt input, output
- level or edge interrupt detect
- pull up, no pull configurable

CPM (Clock and Power Management)

- Clock Input (crystal or clock input)
  - EXCLK: 12MHz, frequncy error < 50 PPM, cycle-to-cycle jitter < 150 ps, to PLL, USB PHY, audio CODEC and some peripherals
  - RTCLK: 32768

- Clock dividers: input from PLL, provides: cclk, hclk(mclk), pclk
- Low power mode :
  - CPU doze: CPU stop and run interlaced in 32 RTCLK cycles one round. The stop/run cycles can be programmed.
  - Module stop: stop selected peripherals
  - CPU idle: stop CPU
  - Sleep: stop all clocks include EXCLK OSC, except RTCLK. (**Typical current 100uA**)
  - Hibernate: Main power down. In additional to sleep mode, all of 1.8V and most parts of 3.3V power down, RTCLK is still alive run. See below for the detials. (**Typical current 5uA**)

RTC (Real Time Clock)

- 32-bit second counter
- 1Hz from 32768hz
- Alarm interrupt
- Independent power
- A 16-bits register used to indicate there's no power down happens for RTC power

INTC (Interrupt Controller)

- Individual masking of sources
- Software priority
- extend interrupt pending register to 32bit

WDT & 6 TCU (Timer, Counter with PWM out)

- WDT and 6 separate Timer/PWM channels
- 16-bit counter
- Counting clock select: pclk, exclk, rtclk
- Counting clock divieded by 1, 4, 16, 64, 256 and 1024 selectable
- Generate power-on reset for WDT
- Two 16-bit comparators, generate interrupt when equal to the counter (none WDT)
- Pulse output controlled by the two comparators (none WDT)

1.2.5 Human Interface Peripherals

LCDC (LCD controller)

- Single/Dual panel STN, Single panel TFT,
- 2, 4, 16 grayscales and up to 4096 colors in STN mode
- 2, 4, 16, 256, 4K, 32K, 64K, 256K and 16M colors in TFT mode
- 18 bit data bus support 1,2,4,8 pins STN panel, 16bit and 18bit TFT and 8bit I/F TFT
- Display size up to 800x600

SLCDC (Smart LCD controller)

- Supports a large variety of LCD Module from different vendors.
- Supports parallel and serial interfaces.

- Supports different size of display panel.
- Supports different width of pixel data.
- Supports DMA operation and register operation.

SADC

- 12-bit, 2Mbps, SNR@500kHz is 61dB, THD@500kHz is -71dB
- XP/XN, YP/YN inputs for touch screen
- 2 generic input Channels
- Triggered by
  - Software
  - Timer periodly
  - External pin

Audio CODEC

- 18-bit DAC, SNR: 88dB
- 16-bit ADC, SNR: 85dB
- Sample rate: 8/11.025/12/16/22.05/24/32/44.1/48kHz

AIC (AC97/I2S Controller)

- Two 32 entries FIFOs
- 8/16/20/24 bit sample supported
- DMA supported
- Compliant with AC'97 standard
- Compliant with I2S standard
- Low power CODEC mode supported
- Variety sample rate supported

CIM (Camera interface module)

- Input image size up to 2048×2048 pixels
- Supports CCIR656 data format
- 32×32 image data receive FIFO with DMA support

1.2.6 Storage Peripherals

MSC (MMC and SD controller)

- Fully compatible with the *MMC System Specification version 3.3*
- Fully compatible with the *SD Memory Card Specification 1.01* and *SD I/O Specification 1.0*
- 20-80 Mbps maximum data rate
- Single or multi block access to the card including erase operation and maximum block length is 2048 bytes
- Stream access to the card
- Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access

NAND Flash Controller

- Support both SLC and MLC type NAND flash
- Reed-Solomon ECC for MLC NAND flash support
- Support boot from NAND flash

1.2.7 Connectivity & Communication Peripherals

I2C

- 2-pin serial port
- single master mode

SSI

- Three synchronous serial interface formats
- 2 channels
- DMA transfer
- Up to 20M bps
- 16 fifo depth

UART

- 16550 compliant uart with 2 pins
- IrDA function up to 115200bps baudrate
- uart up to 921.6kbps baudrate
- dma transfer

UHC (USB 1.1 Host Controller)

- Compliant with USB 1.1 standard
- Full speed
- Embedded USB 1.1 PHY

UDC (USB 2.0 Device Controller)

- Compliant with USB 2.0 standard
- High/full speed
- Embedded USB 2.0 PHY

1.3 Characteristic

Item	Characteristic
Process Technology	0.18um CMOS
Power supply voltage	I/O: 3.3 ± 0.3V Core: 1.8 ± 0.2
Package	193 BGA 13mm * 13mm
Operating frequency	336 – 400MHz
Power consumption	250mw @ 400MHz