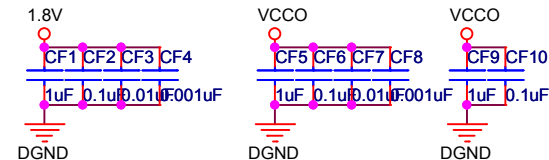
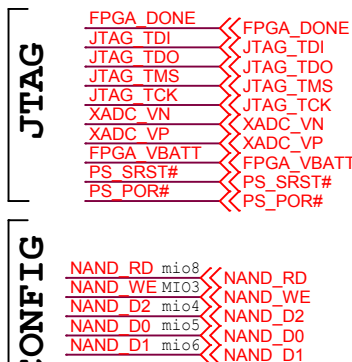
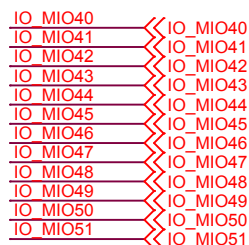
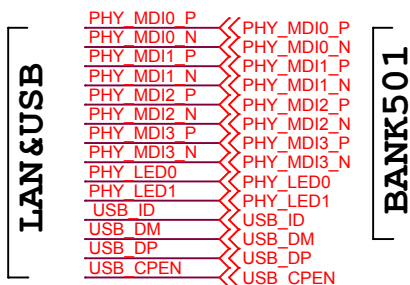
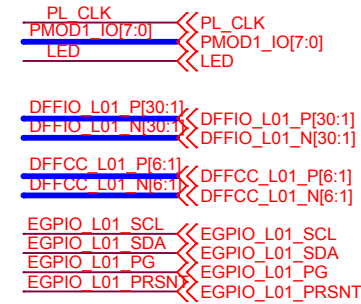
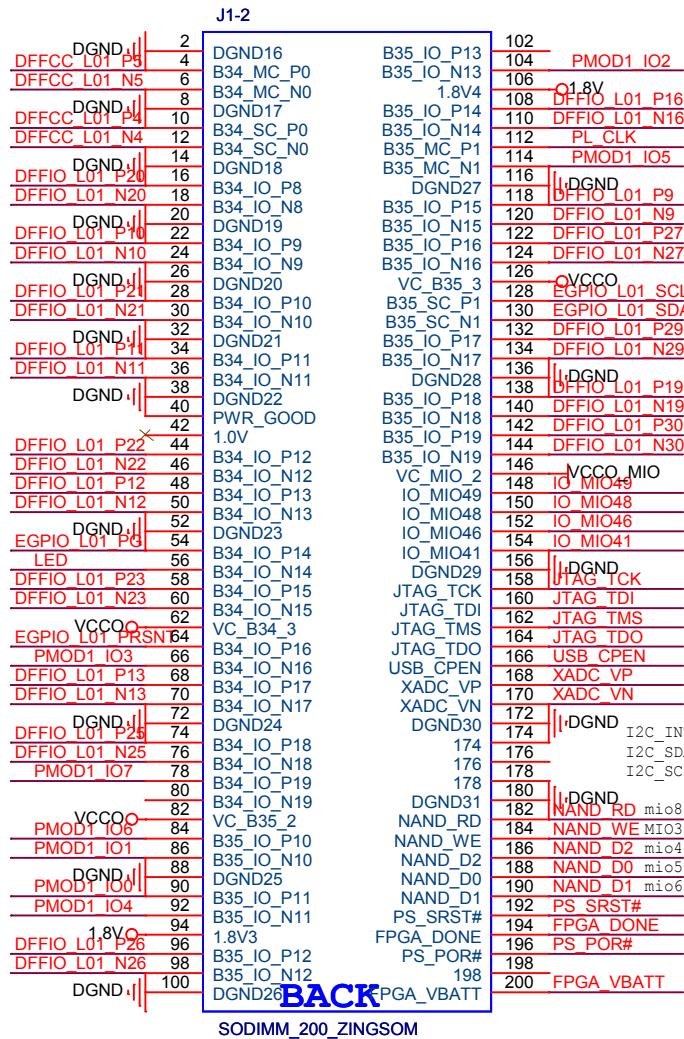
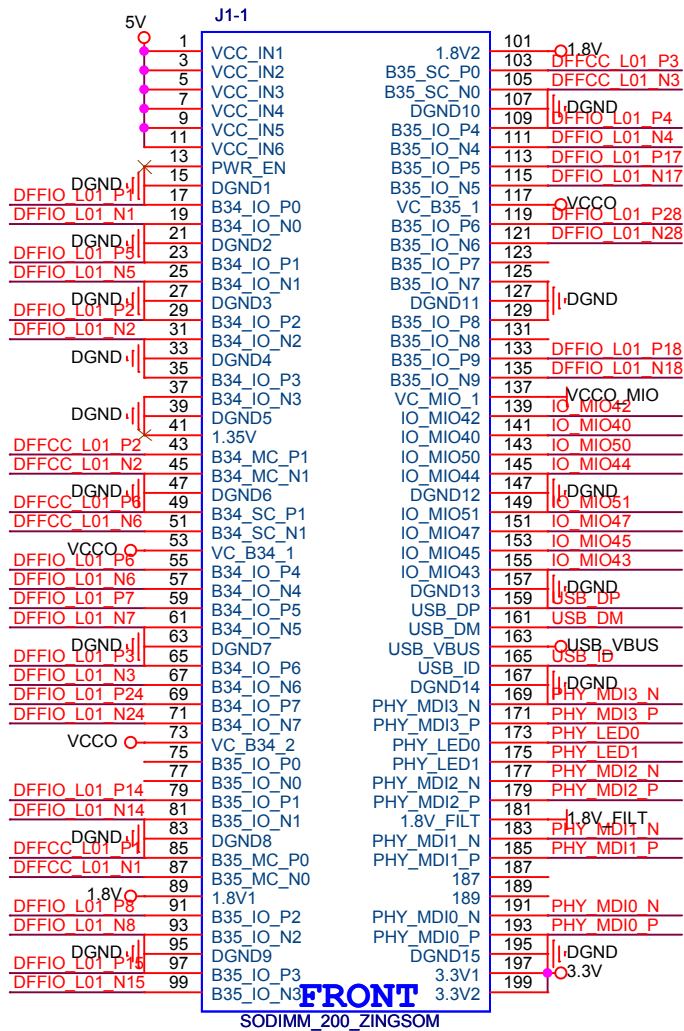


YunSDR V3.0

PAGE01	00	TOP
PAGE02	01	ZINGSOM_SODIMM
PAGE03	02	CONFIG
PAGE04	03	DEVICE_MIO
PAGE05	04	LAN&USBOTG
PAGE06	09	FMC-LPC
PAGE07	06	SMA
PAGE08	07	PL_PIO
PAGE09	08	SYS_POWER

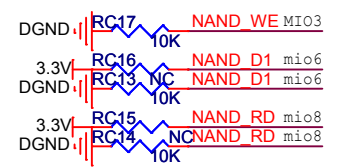
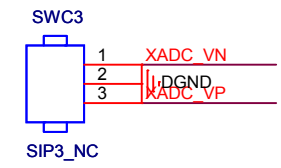
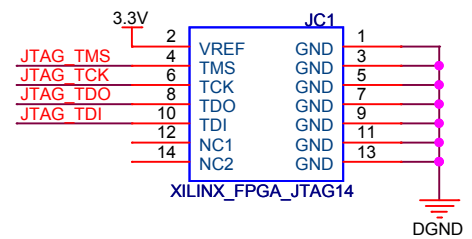
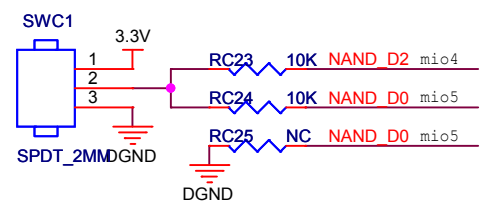
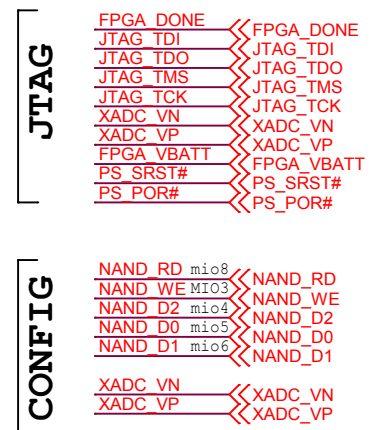
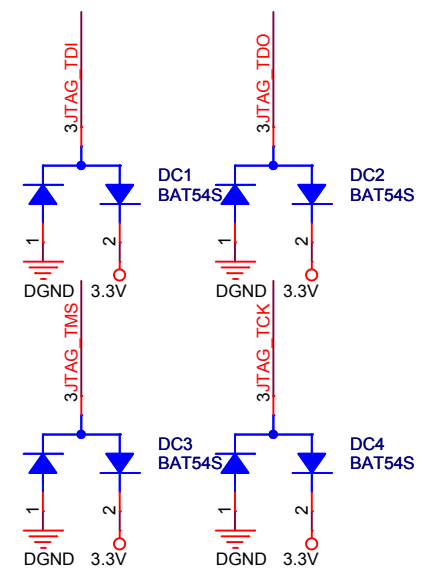
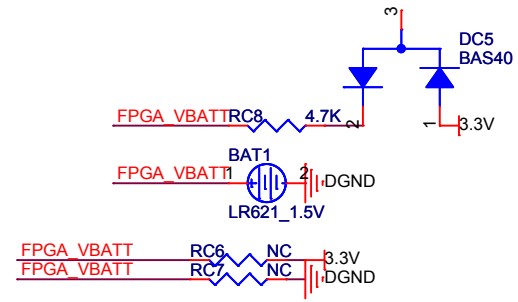
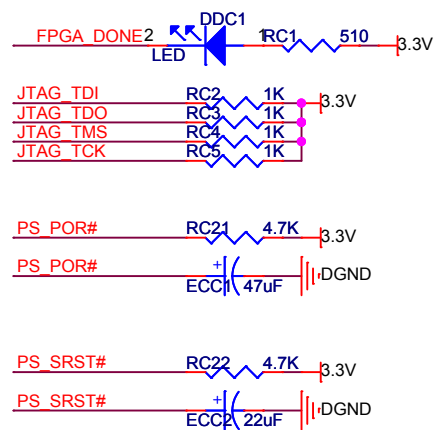


D

C

B

A



	MIO[6]	MIO[5]	MIO[4]	MIO[3]
JTAG	0	0	0	0
NAND	0	1	1	0
SD	1	1	1	0

PLL Used 0

PLL Bypassed 1

MIO Bank1 Voltage

MIO8 0 2.5 V, 3.3 V

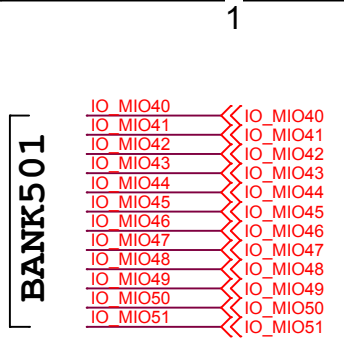
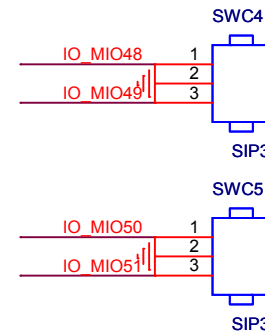
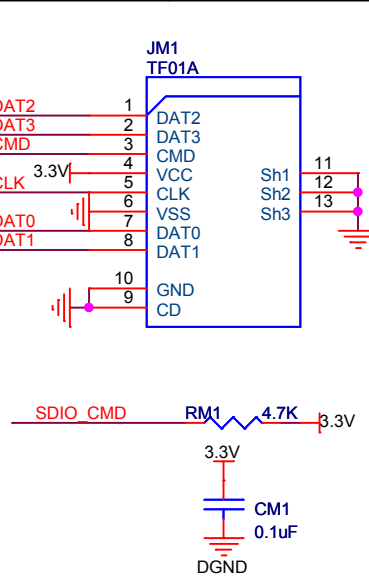
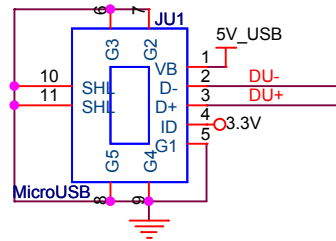
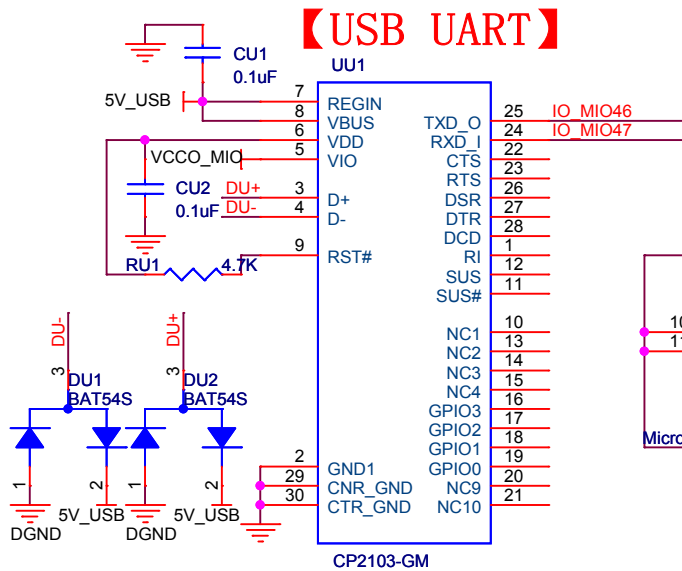
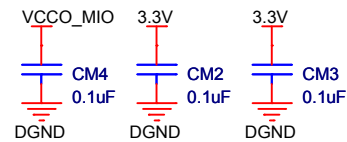
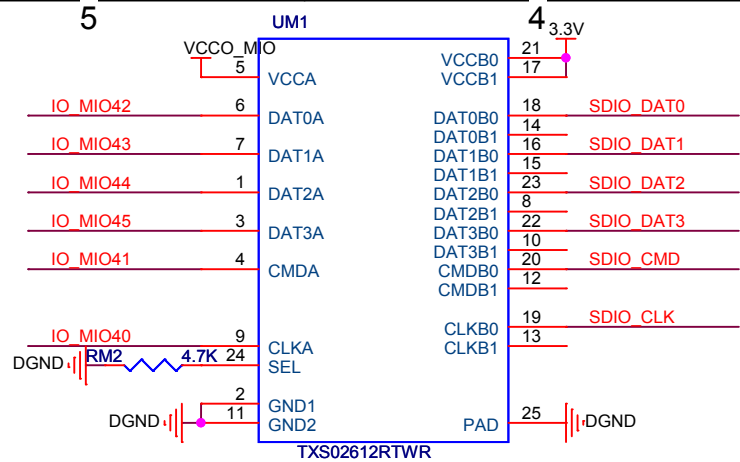
MIO8 1 1.8 V

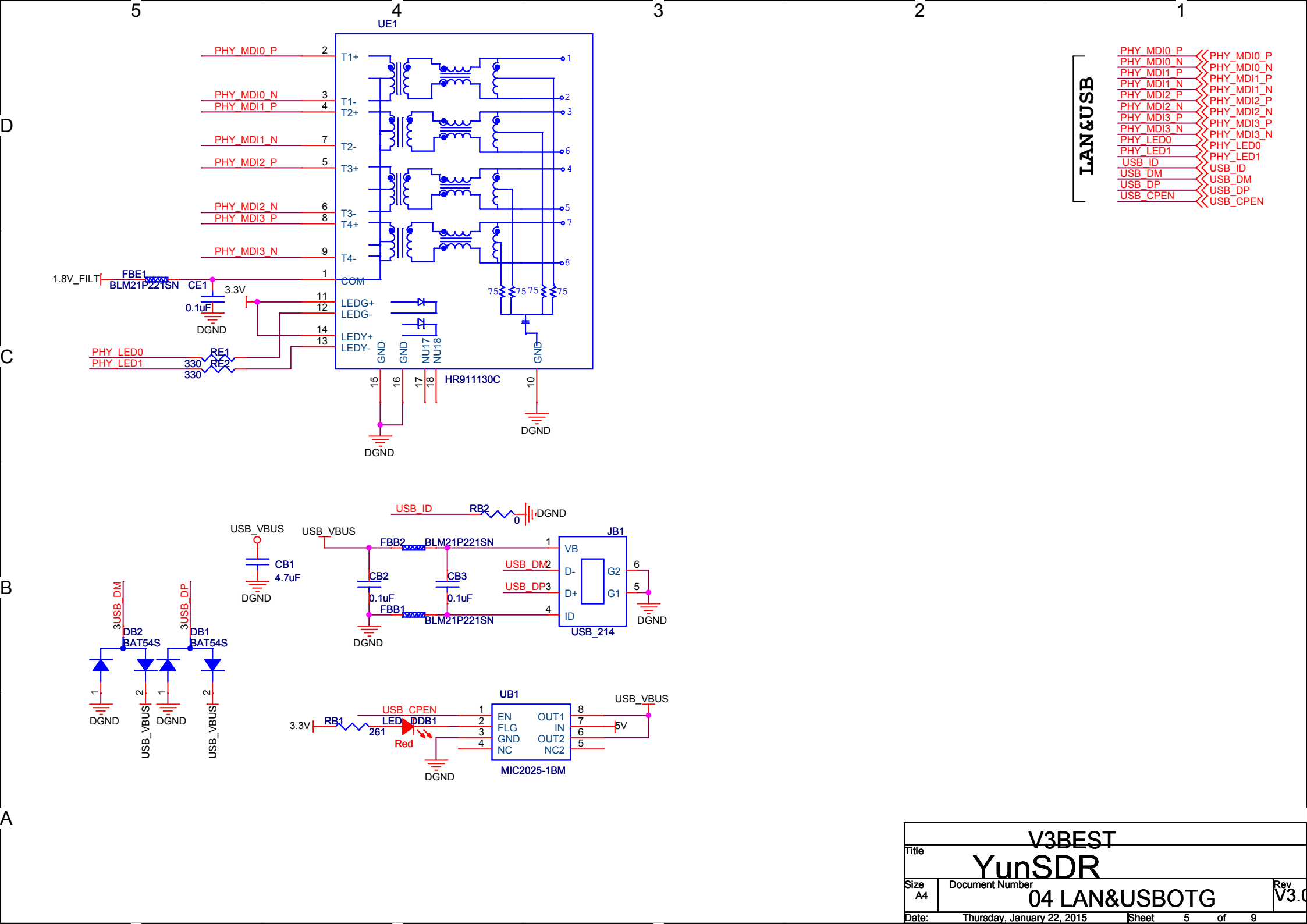
D

C

B

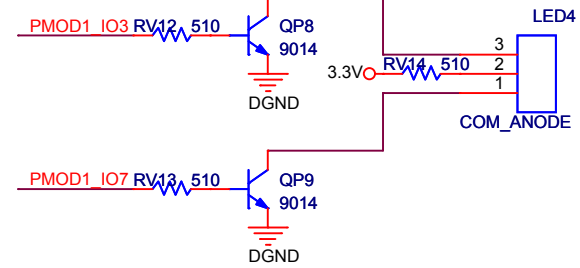
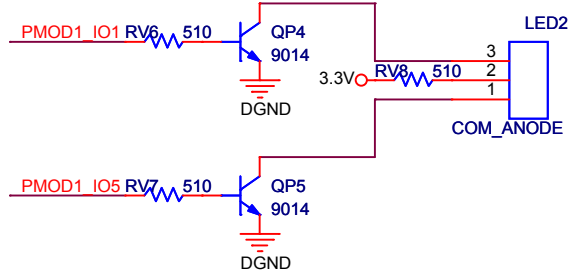
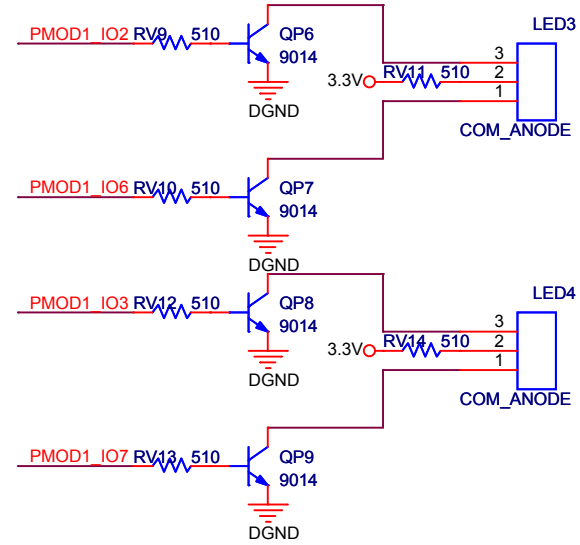
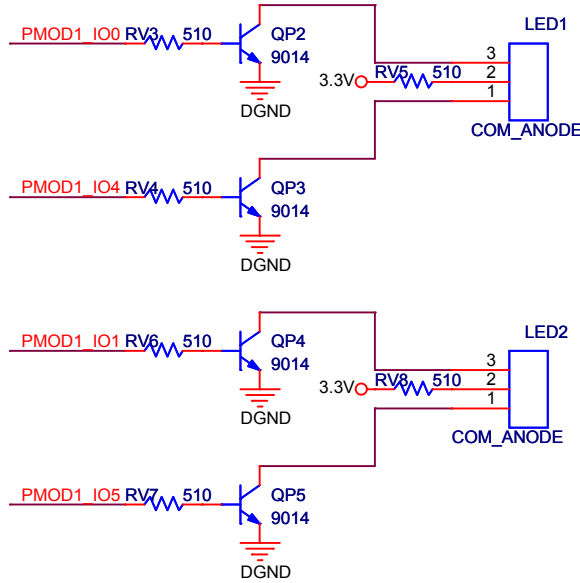
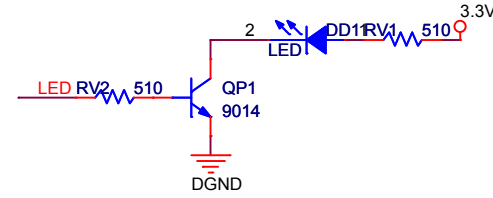
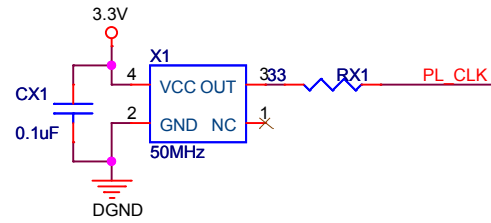
A







PL_CLK
PMOD1_IO[7:0]
LED

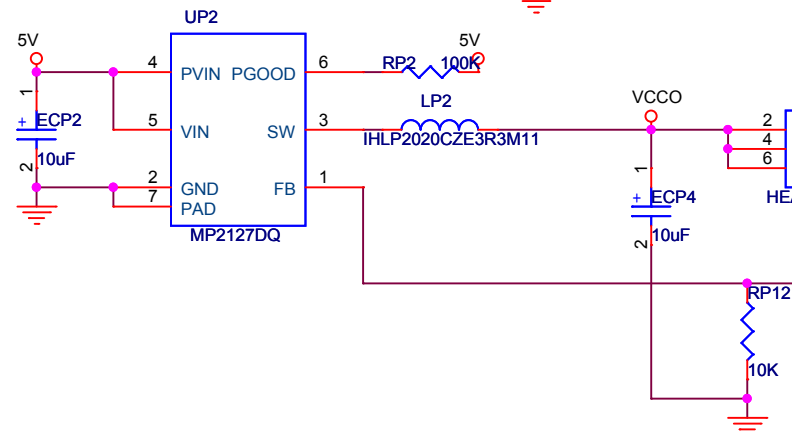
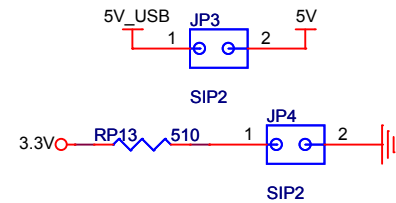
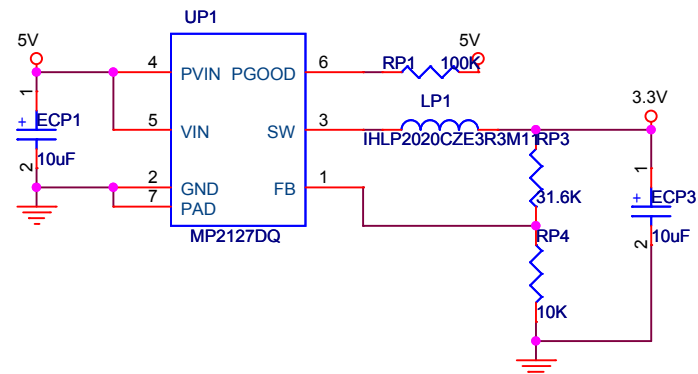


D

C

B

A



VADJ@2A

1.8V

2.5V

3.3V DEFAULT

