Design Rules Verification Report

Filename : C:\Users\Hitech95\Documents\Altium\Projects\xMas-Tree\BoardPanel.PcbDo

Warnings 0
Rule Violations 85

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.127mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	11
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.127mm) (Max=25.4mm) (Preferred=0.127mm) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.3mm) (Conductor Width=0.127mm) (Air Gap=0.127mm)	0
Minimum Annular Ring (Minimum=0.076mm) (All)	0
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.25mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.127mm) (IsPad),(All)	13
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=1.6mm) (All)	4
Board Clearance Constraint (Gap=0mm) (All)	57
Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)	0
Total	85

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint: Net NetLED6_3 Between Via (15.684mm,-27.688mm) from Top Layer to Bottom Layer And Via (82.1mm,-41.2mm) from
Un-Routed Net Constraint: Net 5V0 Between Via (16.434mm,27.238mm) from Top Layer to Bottom Layer And Via (17.566mm,32.162mm) from Top
Un-Routed Net Constraint: Net 5V0 Between Via (16.434mm,-27.238mm) from Top Layer to Bottom Layer And Via (17.566mm,-32.162mm) from Top
Un-Routed Net Constraint: Net NetLED9_3 Between Via (16.73mm,32.664mm) from Top Layer to Bottom Layer And Via (18.316mm,-31.712mm) from
Un-Routed Net Constraint: Net NetLED6_3 Between Via (17.9mm,-1.498mm) from Top Layer to Bottom Layer And Via (17.9mm,1.502mm) from Top
Un-Routed Net Constraint: Net GND Between Via (26mm,-19.5mm) from Top Layer to Bottom Layer And Via (29.5mm,-26mm) from Top Layer to
Un-Routed Net Constraint: Net NetLED9_3 Between Via (30.4mm,-40.5mm) from Top Layer to Bottom Layer And Via (69.6mm,-2.094mm) from Top
Un-Routed Net Constraint: Net GND Between Via (63.5mm,15.5mm) from Top Layer to Bottom Layer And Via (70.5mm,14.5mm) from Top Layer to
Un-Routed Net Constraint: Net NetLED9_3 Between Via (69.6mm,-1.494mm) from Top Layer to Bottom Layer And Via (69.6mm,1.506mm) from Top
Un-Routed Net Constraint: Net NetLED9_3 Between Via (80.6mm,2.098mm) from Top Layer to Bottom Layer And Via (80.6mm,-1.502mm) from Top
Un-Routed Net Constraint: Net 5V0 Between Via (81.516mm,-3.016mm) from Top Layer to Bottom Layer And Via (82.1mm,-2.102mm) from Top Layer

Silk To Solder Mask (Clearance=0.127mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.127mm) Between Pad C7-1(21.57mm,36.8mm) on Top Layer And Polygon Region (1
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.127mm) Between Pad C7-2(20.03mm,36.8mm) on Top Layer And Polygon Region (1
Silk To Solder Mask Clearance Constraint: (0.12mm < 0.127mm) Between Pad Free-0(79.1mm,1.8mm) on Bottom Layer And Polygon Region (3
Silk To Solder Mask Clearance Constraint: (0.12mm < 0.127mm) Between Pad Free-0(79.1mm,-1.8mm) on Bottom Layer And Polygon Region (3
Silk To Solder Mask Clearance Constraint: (0.12mm < 0.127mm) Between Pad Free-0(83.6mm,1.8mm) on Bottom Layer And Polygon Region (3
Silk To Solder Mask Clearance Constraint: (0.101mm < 0.127mm) Between Pad Free-0(83.6mm,-1.8mm) on Bottom Layer And Polygon Region (3
Silk To Solder Mask Clearance Constraint: (0.077mm < 0.127mm) Between Pad Free-2(80.6mm,1.798mm) on Bottom Layer And Polygon Region (3
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.127mm) Between Pad Free-2(82.1mm,-1.802mm) on Bottom Layer And Polygon Region (3
Silk To Solder Mask Clearance Constraint: (0.075mm < 0.127mm) Between Pad Free-3(80.6mm,-1.8mm) on Bottom Layer And Polygon Region (3
Silk To Solder Mask Clearance Constraint: (0.079mm < 0.127mm) Between Pad Free-3(82.1mm,1.796mm) on Bottom Layer And Polygon Region (3
Silk To Solder Mask Clearance Constraint: (0.11mm < 0.127mm) Between Pad U2-8(22.5mm,-18.9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.061mm < 0.127mm) Between Pad USBC-2(12.52mm,-23.775mm) on Multi-Layer And Polygon Region (C
Silk To Solder Mask Clearance Constraint: (Collision < 0.127mm) Between Pad USBC-4(12.52mm,-27.575mm) on Multi-Layer And Polygon Region (C

Net Antennae (Tolerance=1.6mm) (All)
Net Antennae: Via (80.6mm,-1.502mm) from Top Layer to Bottom Layer
Net Antennae: Via (80.6mm,-2.102mm) from Top Layer to Bottom Layer
Net Antennae: Via (82.1mm,-1.502mm) from Top Layer to Bottom Layer
Net Antennae: Via (82.1mm,-2.102mm) from Top Layer to Bottom Layer

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (0mm < 0.2mm) Between Area Fill (-4.6mm,-14.8mm) (11.4mm,-8mm) on Bottom Layer And Board Edge
Board Outline Clearance(Outline Edge): (0mm < 0.2mm) Between Area Fill (-4.6mm,-14.8mm) (11.4mm,-8mm) on Top Layer And Board Edge
Board Outline Clearance(Cutout Edge): (Collision < 0.2mm) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Pad
Board Outline Clearance(Cutout Edge): (Collision < 0.2mm) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Track
Board Outline Clearance(Cutout Edge): (Collision < 0.2mm) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Track
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Board Outline Clearance(Cutout Edge): (0.2mm < 0.2mm) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Via
Board Outline Clearance(Cutout Edge): (0.2mm < 0.2mm) Between Board Cutout (Multi-Layer)Region (0 hole(s)) Multi-Layer And Via
Board Outline Clearance(Outline Edge): (Collision < 0.2mm) Between Board Edge And Track (0mm,-19.4mm)(0mm,-11.4mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.2mm) Between Board Edge And Track (0mm,-19.4mm)(7.5mm,-19.4mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.2mm) Between Board Edge And Track (0mm,-3.4mm)(0mm,-11.4mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.2mm) Between Board Edge And Track (0mm,-3.4mm)(7.5mm,-3.4mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.2mm) Between Board Edge And Track (0mm,40mm)(33mm,20mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (Collision < 0.2mm) Between Board Edge And Track (0mm,-40mm)(33mm,-20mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (Collision < 0.2mm) Between Board Edge And Track (0mm,40mm)(33mm,20mm) on Top Layer
Board Outline Clearance(Outline Edge): (Collision < 0.2mm) Between Board Edge And Track (0mm,-40mm)(33mm,-20mm) on Top Layer
Board Outline Clearance(Outline Edge): (Collision < 0.2mm) Between Board Edge And Track (67mm,20mm)(100mm,0mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (Collision < 0.2mm) Between Board Edge And Track (67mm,-20mm)(100mm,0mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (Collision < 0.2mm) Between Board Edge And Track (67mm,20mm)(100mm,0mm) on Top Layer

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (Collision < 0.2mm) Between Board Edge And Track (67mm,-20mm)(100mm,0mm) on Top Layer