Hitesh Gehlot

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Relevant Coursework

- VLSI Design
- Computer Architecture
- Static Timing Analysis(STA)
- Digital Electronics
- Digital IC Design
- CMOS Circuits
- VLSI Physical Design

Experience

eInfochips- an Arrow company **June 2024 -July 2024**
ASIC Intern- OpenROAD, Linux, Verilog HDL, Yosys *Ahmedabad, Gujarat*

- Worked on **RTL to GDSII flow**, including **synthesis** using OpenROAD and Nangate45 technology.
- Processed the **PicoRV32 Processor GitHub repository** with all Verilog files and constraints for implementation.
- Used Yosys for logic synthesis, generating gate-level netlists.

Sasken Silicon Technologies **Feb 2025 – Present**
Analog Circuit Design Intern – Cadence Virtuoso, CMOS Design *Ahmedabad, Gujarat*

- **Project: GPIO Interface Design (1.8V & 3.3V)**
- Designed a **GPIO interface** operating at **125MHz**, covering both **receiver** and **transmitter paths** between **1.8V GPIO** and **0.7V core**, adhering to **1.8V device limits**.
- Developed a **2x design architecture** to support **3.3V GPIO operation** while keeping devices within **1.8V limits**.
- Designed the **receiver path** using a **Schmitt Trigger**, **high-to-low level shifter**, and **buffer chain**.
- Designed the **transmitter path** with a **low-to-high level shifter**, **pre-driver**, and **driver stages**.
- Implemented **Fail-Safe Circuits** in both **1.8V and 3.3V GPIO paths** to protect devices under fault scenarios.
- Verified complete **AC/DC specifications** including **VIH, VIL, VOH, VOL, IOH, IOL, rise/fall times, delay**, and **duty cycle** across all **PVT corners**.

Projects

Gem5 Simulator | *Linux, Computer Architecture*

- Analyzed **C code performance** with L1 and L2 cache configurations and no-cache setups using gem5's TimingSimpleCPU model.
- Evaluated **execution time, CPI, cache hit rates, and power** to analyze the effect of different cache levels on system performance.

Single Cycle Datapath for Micro-MIPS Processor | *Verilog, Computer Architecture*

- Implemented a **single-cycle MIPS datapath** with a register file, ALU, and memory.
- Developed and integrated **Verilog modules** for instruction execution.

Technical Skills

Languages: Verilog HDL, C++, Bash Shell Scripting

Developer Tools: Quartus II, Keil uVision, Microwind, MATLAB, Cadence Virtuoso, ModelSim Altera, Arduino IDE

Education

Nirma University **2021 – 2025**
B.Tech. - Electronics and Communication Engineering- CGPA: 8.4 / 10 *Ahmedabad, Gujarat*

Hillgrove Col's Academy School, Sumerpur **2020**
12th | CBSE | Percentage: 82 / 100 *Sumerpur, Rajasthan*

H.C. Bafna International School, Sumerpur **2018**
10th | BSER | Percentage: 87.33 / 100 *Sumerpur, Rajasthan*

Publications

Linux based Real Time Certificate Generation and Auto-emailing through API and CRON
3rd International Conference on Applied Artificial Intelligence and Computing - No. of Authors: 3