

EE230: Experiment 2

Non-idealities in Op-amps

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1 Overview of the experiment

1.1 Aim of the experiment

In reality, no OpAmps are ideal, they all have some non-idealities which can affect our measurement. Some of these major non-idealities of UA741 Op-amp are:

- a) Input Offset voltage
- b) Input Bias currents
- c) Finite open-loop gain.

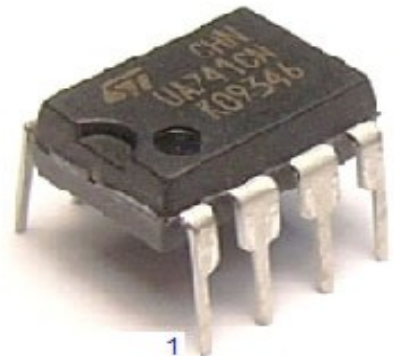
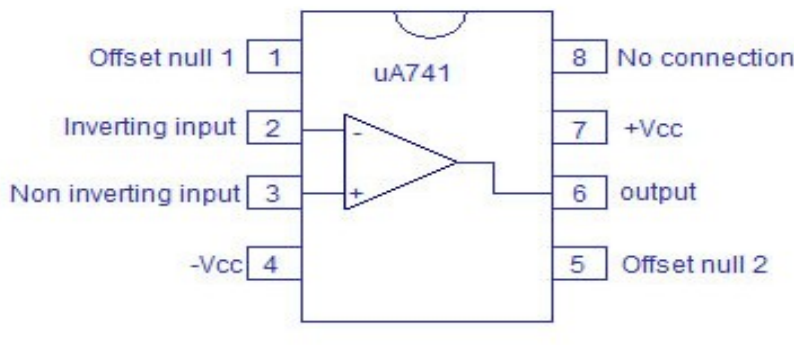


Figure 1: Pinout and external appearance of Op Amp 741

1.2 Methods

- (i) For measuring the non-idealities such as offset voltage and input bias currents, we design circuits that enhance the contributions one of these parameters while keeping the other two contributions small.
- (ii) DC open loop gain is measured in such a way that it actually contributes to the high closed loop gain of the non-inverting amplifier, the circuit is designed considering the appropriate values of resistance such that even the gain is high and op-amp doesn't go in saturation.
- (iii) We also measured open loop gain of AC input signal for different frequencies to understand a brief relation of open loop gain with frequency.

2 Design of Op-amp 741

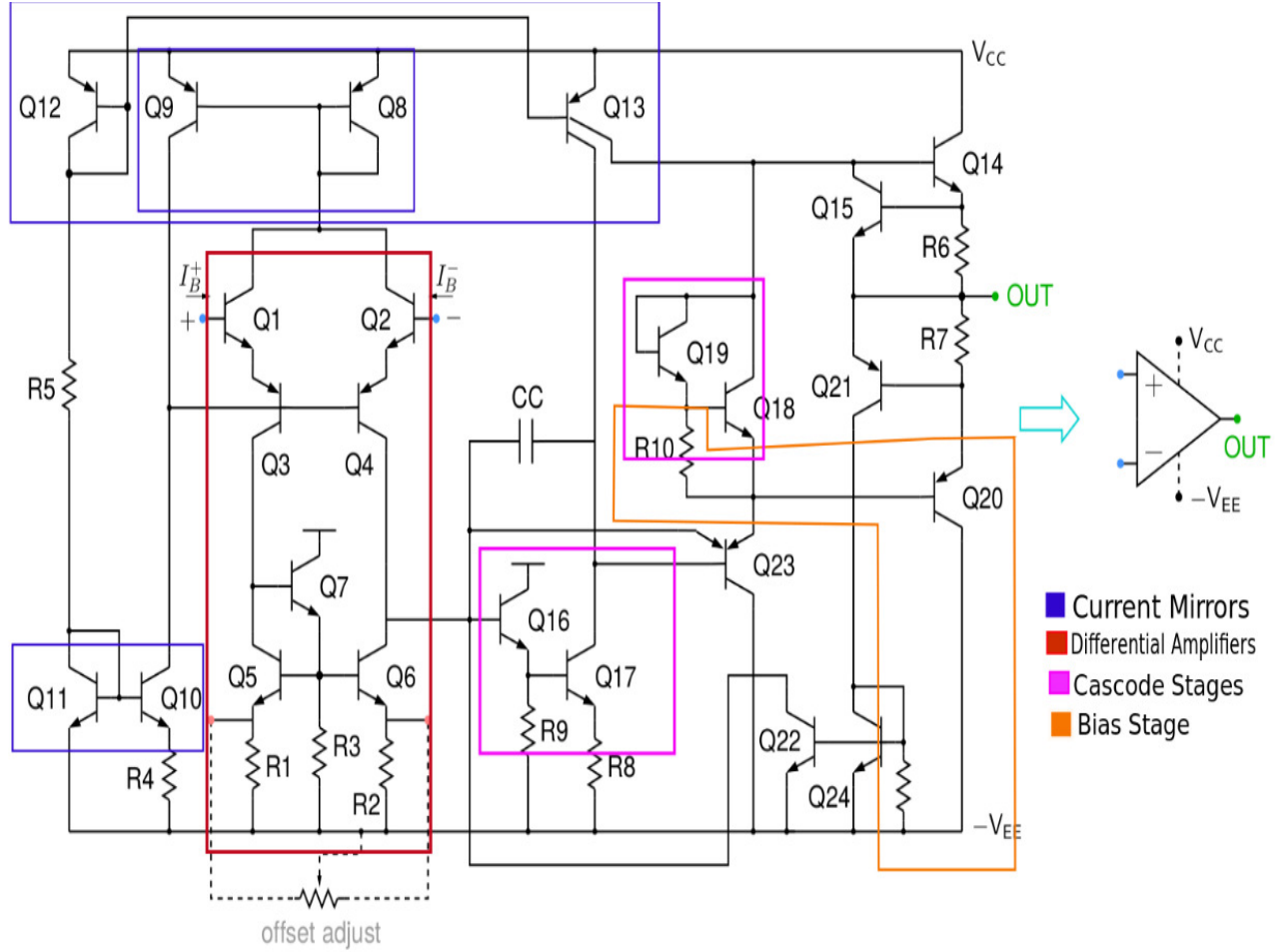


Figure 2: Internal circuit of Op Amp 741

- The current mirror circuit copies or mirrors the current flowing in one active device in another, keeping the output current constant regardless of loading. An ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well or it is a current-controlled current source (CCCS). The current mirror is used to provide bias currents and active loads to circuits.
- The differential amplifier amplifies the voltage difference present on its inverting and non-inverting inputs.
- A single stage of amplifier can provide only a limited current gain or voltage gain. Therefore for a higher voltage gain or current gain, several amplifier stages are connected in cascade i.e. connected such that the output of one stage becomes the input to the next stage.

3 Experimental results

3.1 Input offset voltage measurement

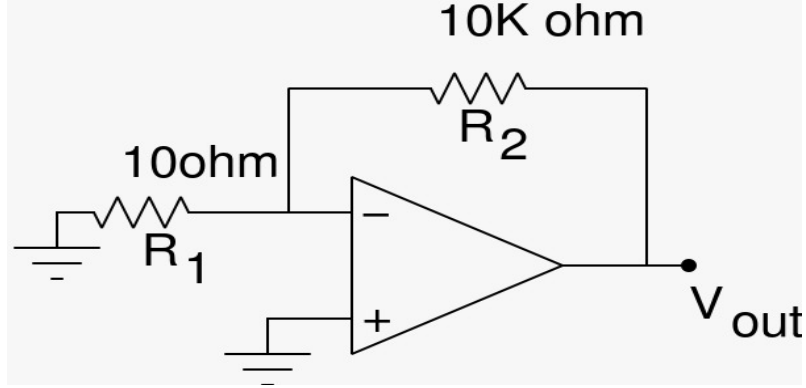


Figure 3: Circuit diagram for measuring V_{OS}

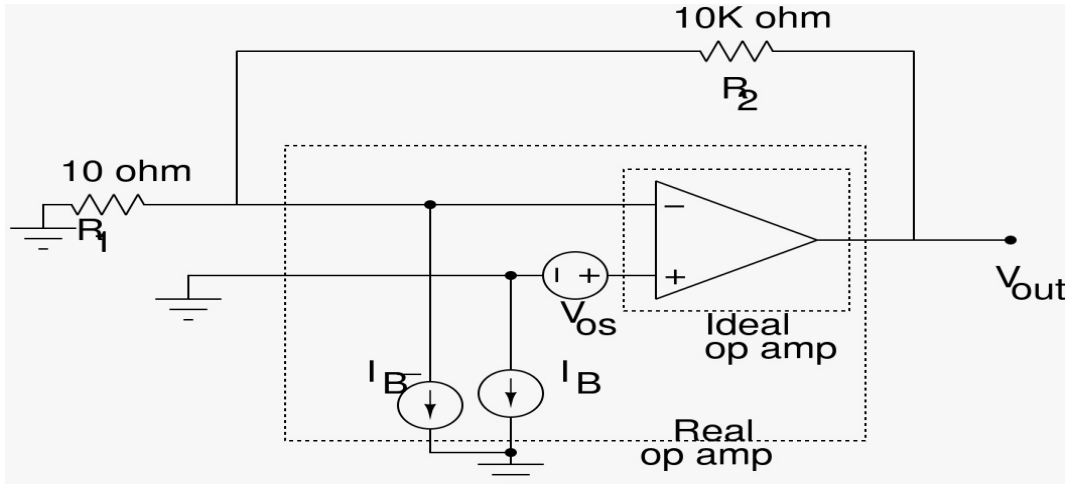


Figure 4: Equivalent circuit

$$V_0 = V_{OS} \left(1 + \frac{R_2}{R_1} \right) + R_2 I_B^- \quad (1)$$

By choosing R_1 and R_2 as given in the circuit, we can neglect the second term in the above equation as $V_{OS} \approx 5mV$ and $I_B \approx 100nA$. Hence

$$V_{OS} = \frac{V_0}{1 + \frac{R_2}{R_1}} \approx \frac{V_0}{\frac{R_2}{R_1}} \quad (2)$$

The observed output value for ua741 is 1.11V, hence $V_{OS} = 1.11mV$

3.2 Bias currents measurement

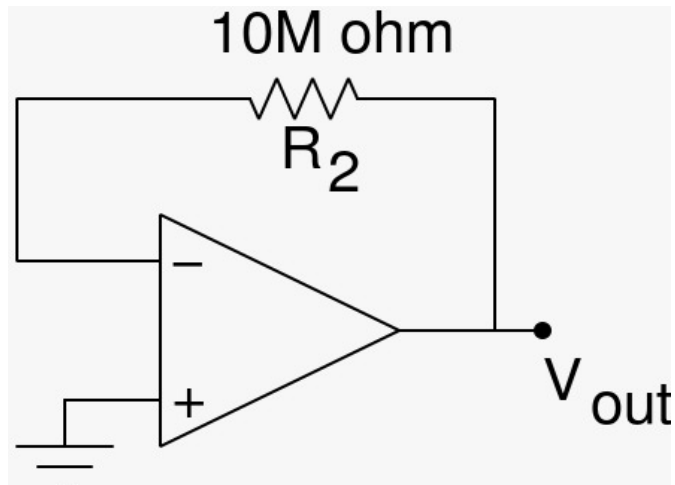


Figure 5: Circuit diagram for measuring I_B^-

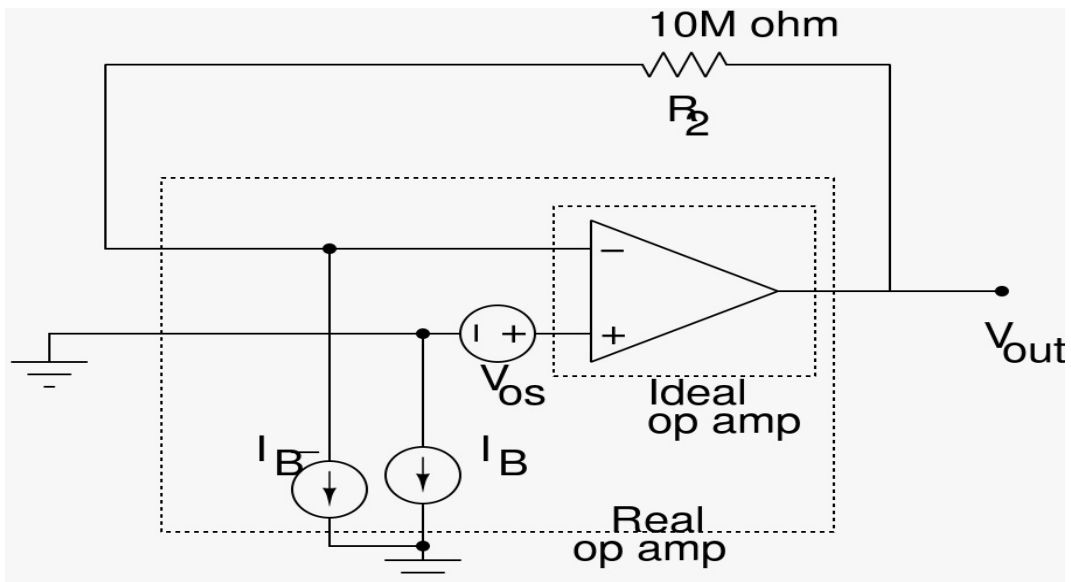


Figure 6: Equivalent internal circuit

$$V_0 = V_{OS} + RI_B^- \quad (3)$$

R has chosen large so that the second term is large enough to neglect the first term, hence

$$I_B^- = \frac{V_0}{R} \quad (4)$$

The observed output value for *ua741* is 0.354V, hence $I_B^- = 35.4\text{nA}$

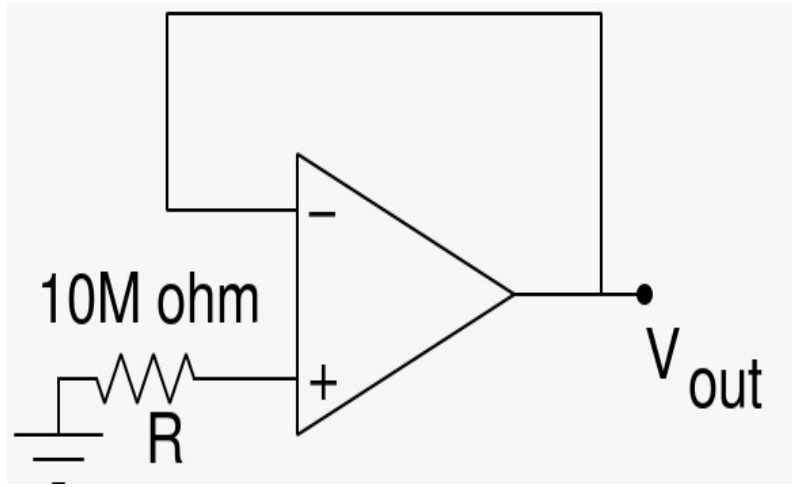


Figure 7: Circuit diagram for measuring I_B^+

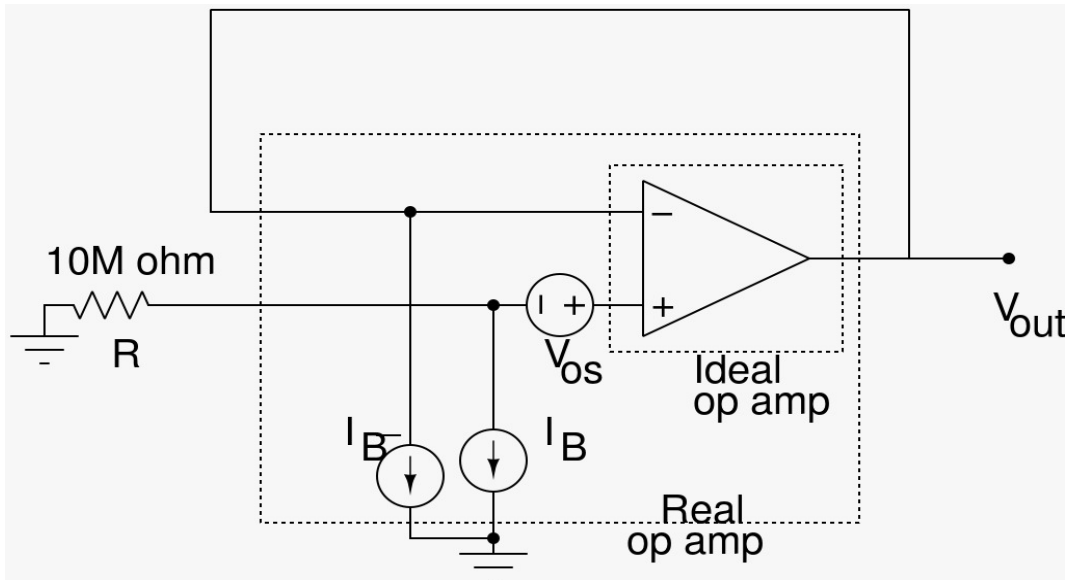


Figure 8: Equivalent internal circuit

$$V_0 = V_{OS} - RI_B^+ \quad (5)$$

Similarly the equation can be approximated to

$$I_B^+ = -\frac{V_0}{R} \quad (6)$$

The observed output value for *ua741* is $-0.343V$, hence $I_B^+ = 34.3nA$

3.3 DC open-loop gain measurement

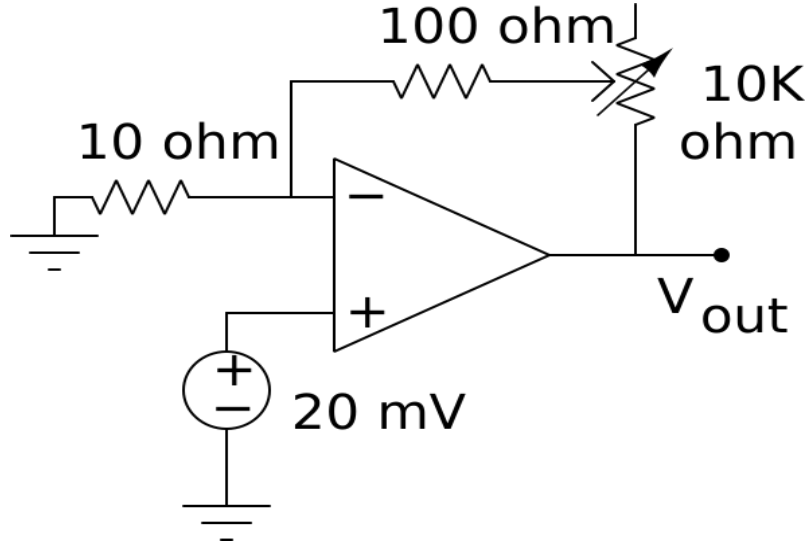


Figure 9: Circuit diagram for measuring DC open loop gain

The actual gain expression for the above circuit is

$$Gain = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + \left(1 + \frac{R_2}{R_1}\right) \frac{1}{A_v}} \quad (7)$$

To find the open loop gain(A_v), we found the gain for large values of $\left(1 + \frac{R_2}{R_1}\right)$ so that A_v contributes for the actual gain

Also we have taken care of choosing $\left(1 + \frac{R_2}{R_1}\right)$ so that op-amp does not saturate and the actual gain can be measured

For $1 + \frac{R_2}{R_1} = 870$ we observed a gain of 663.5 and so A_v was 2.8×10^3

The challenge we faced in this experiment was finding the feedback resistance as it's a variable resistance, we had to find out the current and the voltage through and across the feedback resistor to find it's resistance along with the output voltage to find the gain. So we ended up with using all the multimeters we have.

Note: Instead of nullifying offset voltage in this experiment using pin 1 and pin 5 of the IC, we included it in the Gain expression. The Gain was adapted to

$$Gain = \frac{V_{out}}{V_{in} + V_{OS}} \quad (8)$$

3.4 Variation of open-loop gain with frequency

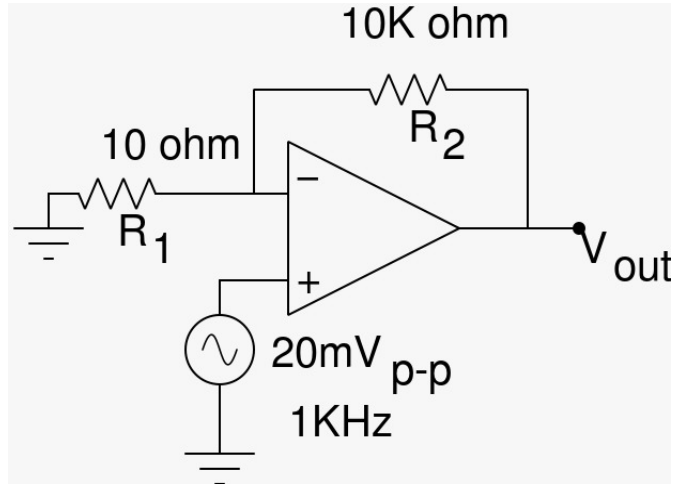


Figure 10: Circuit diagram for measuring open loop gain A_v

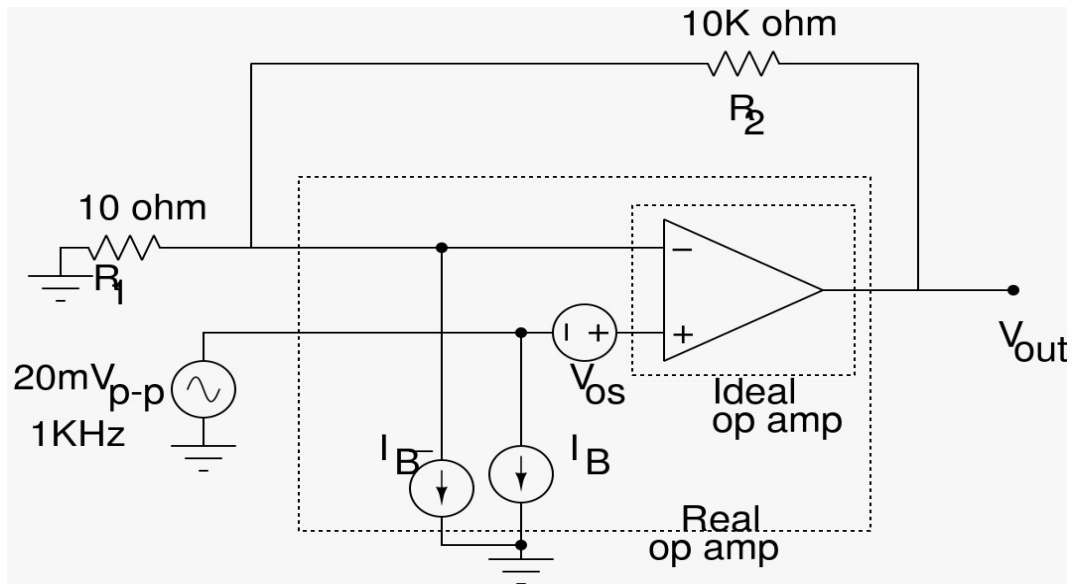
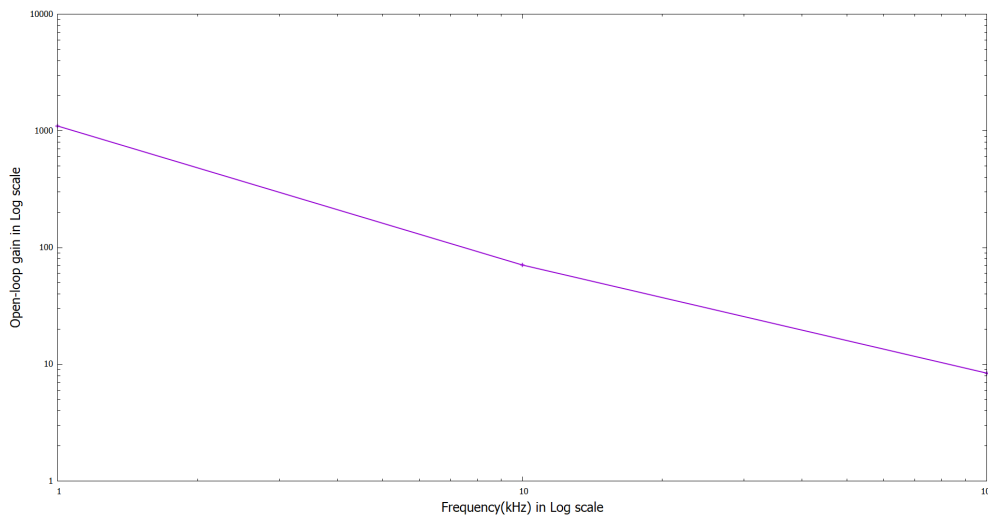


Figure 11: Equivalent internal circuit

Analysis of open-loop gain with frequency was achieved with AC input which is similar to the previous section with just a change in values of $R_2 = 10K\Omega$ and $R_1 = 10\Omega$ here the closed loop gain was 1000, the observations were



frequency(kHz)	A_v
1	1100
10	70.93
100	8.4

(a) A_v Vs frequency in log scale

This plot is linear and matches approximately with the open-loop gain vs frequency curve in log scale given in the datasheet of UA741.

Frequency response of IC 741:

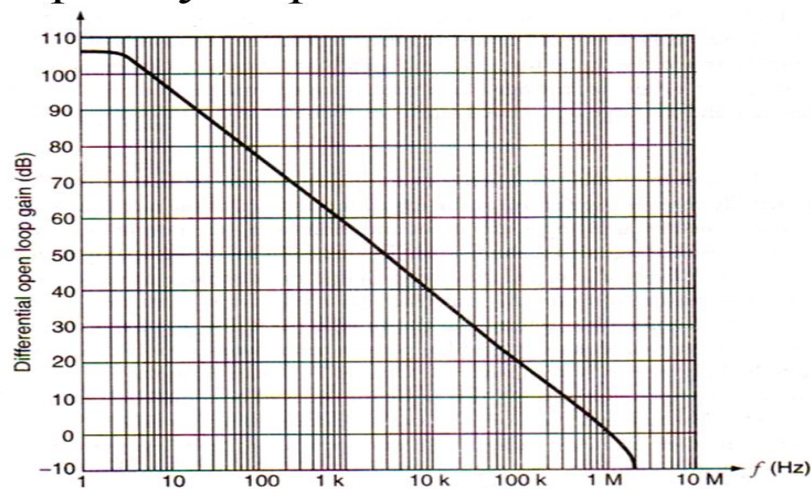


Figure 13: Amplification v/s Frequency

4 Questions for reflection

1. If the method for null-adjustment is as simple as the one you performed in lab, why isn't the 741 op-amp sold with the offset voltage internally calibrated?

Ans. Some of the reasons could be:

- Input offset voltage value may change with temperature or age.

- Since offset voltage is itself generated because of manufacturing process, its value could not be known for sure.
- One cannot remove the offset voltage completely, it can be reduced to few microvolts.

That is why 741 op-amp isn't sold with the offset voltage internally calibrated.

2. If the temperature in the lab were different from what it was when you performed the experiment, do you expect the pot value you ended up with will still give you offset nullification? Explain your answer. Hint: Look at the internal circuit diagram and figure out what parameters may change when the temperature changes.

Ans. No. With the change in temperature, offset voltage changes and hence the pot value required for offset nullification would change.

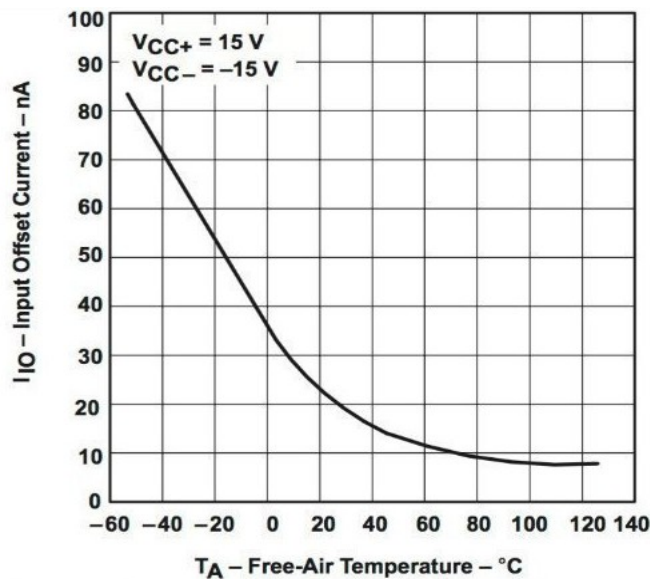


Figure 14: Input Offset Voltage v/s Temperature

3. What is the slew-rate of an op-amp? Read up the definition and explain it in your own words here. Could you suggest an experiment to measure slew-rate of op-amp 741?

Ans. Slew-rate of an op-amp specifies the maximum and minimum limit of rate of change of voltage per unit of time i.e. when the input is amplified, the output cannot rise to a large value, because of the upper limit slew-rate specification of op-amp.

We can use a non-inverting amplifier of gain one and give a square wave as input, as a square wave is discontinuous we expect the output to change its value in infinitesimal time which is not observed practically because of slew rate. So the slew rate would be voltage of the top level of the distorted square output voltage signal divided by time taken to reach that level from bottom level.

4. What is the role of capacitor C in the circuit you used in the second part of the lab (i.e. in figure 8 of the hand-out)? (Hint: there is a statement in the hand-out mentioning why C is connected; could you explain why that statement is true?)

Ans. The capacitor C prevents the circuit from oscillating. We see that coupled with R4 and R5, capacitor acts as an integrator. From the Bode plot (shown in Figure 10) of capacitor we observe that capacitor filters out the high frequency noise (which could have greatly affected in the measurement of AOL)

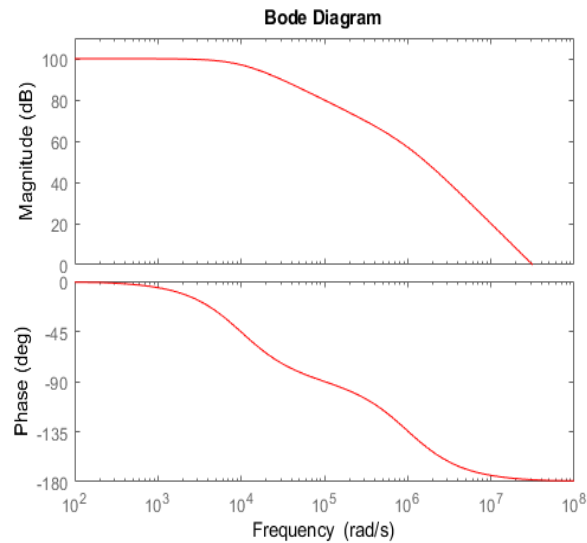


Figure 15: Bode Plot of an Integrator

References

- [1] Non-idealities of op-amp File
<https://moodle.iitb.ac.in/mod/resource/view.php?id=92663>
- [2] Datasheet of OpAmp UA741
<https://www.slideshare.net/YongHeuiCho/u-a741>