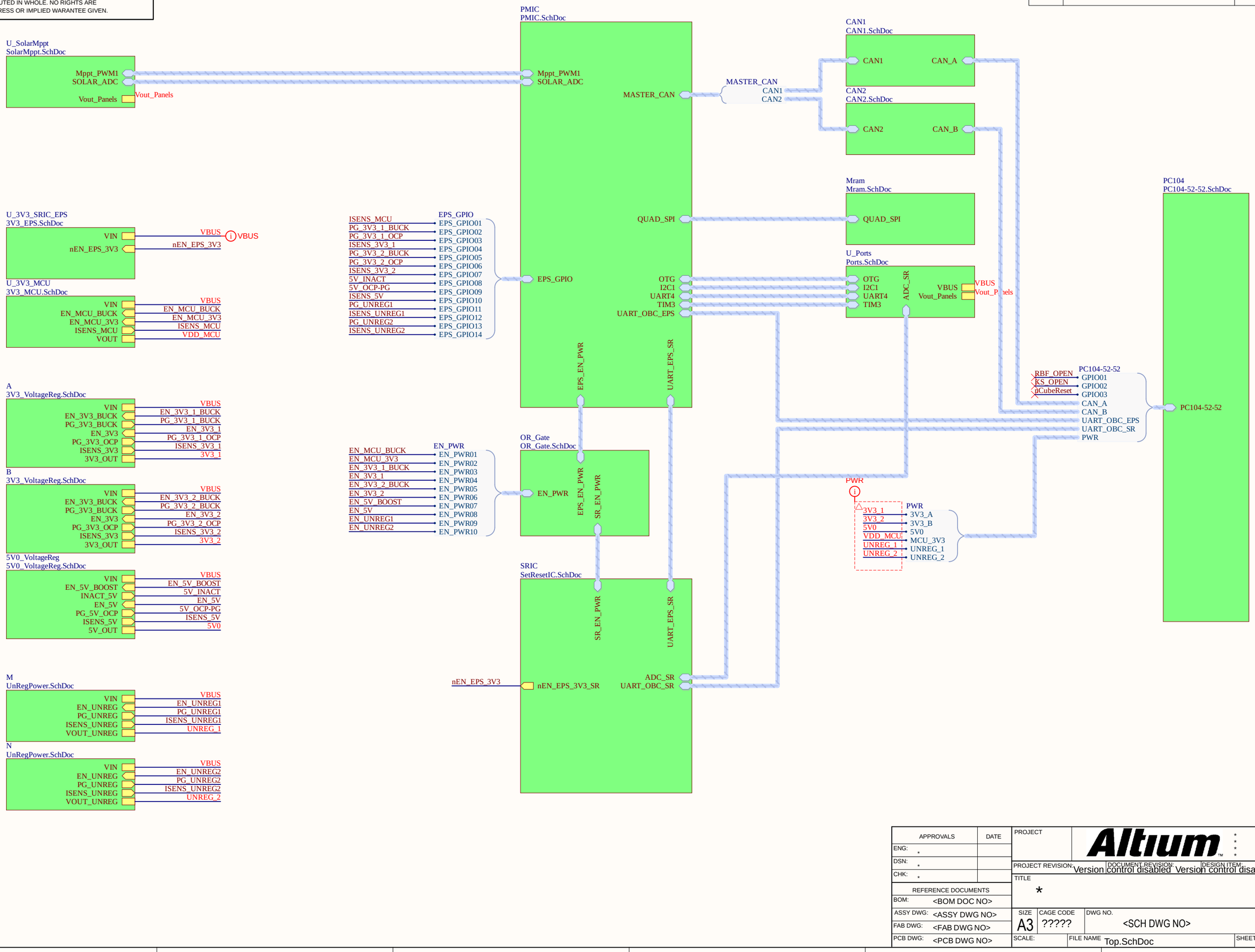
REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
ENG: *	
DSN: *	
CHK: *	

REFERENCE DOCUMENTS

BOM:	<BOM DOC NO>
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PCB DWG:	<PCB DWG NO>

PROJECT

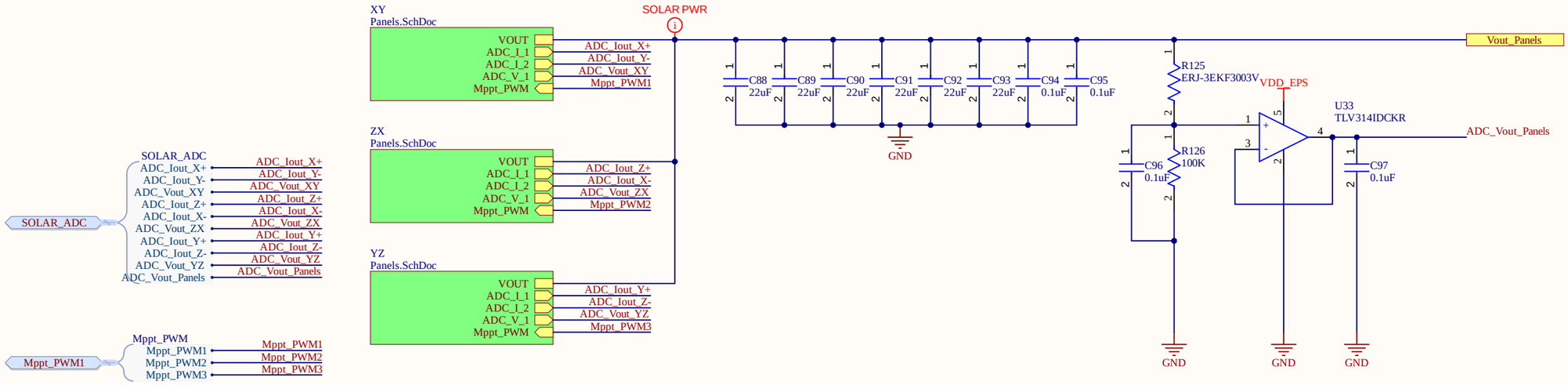
PROJECT REVISION: Version control disabled | DOCUMENT REVISION: | DESIGN ITEM: Version control disabled

TITLE *

SIZE	CAGE CODE	DWG NO.	REV
A3	?????	<SCH DWG NO>	

SCALE: | FILE NAME Top.SchDoc | SHEET 1 OF 21

REVISION	DESCRIPTION	DATE	APPROVED



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CHK: *	

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BOM:	<BOM DOC NO>
ASSY DWG:	<ASSY DWG NO>
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PCB DWG:	<PCB DWG NO>

PROJECT

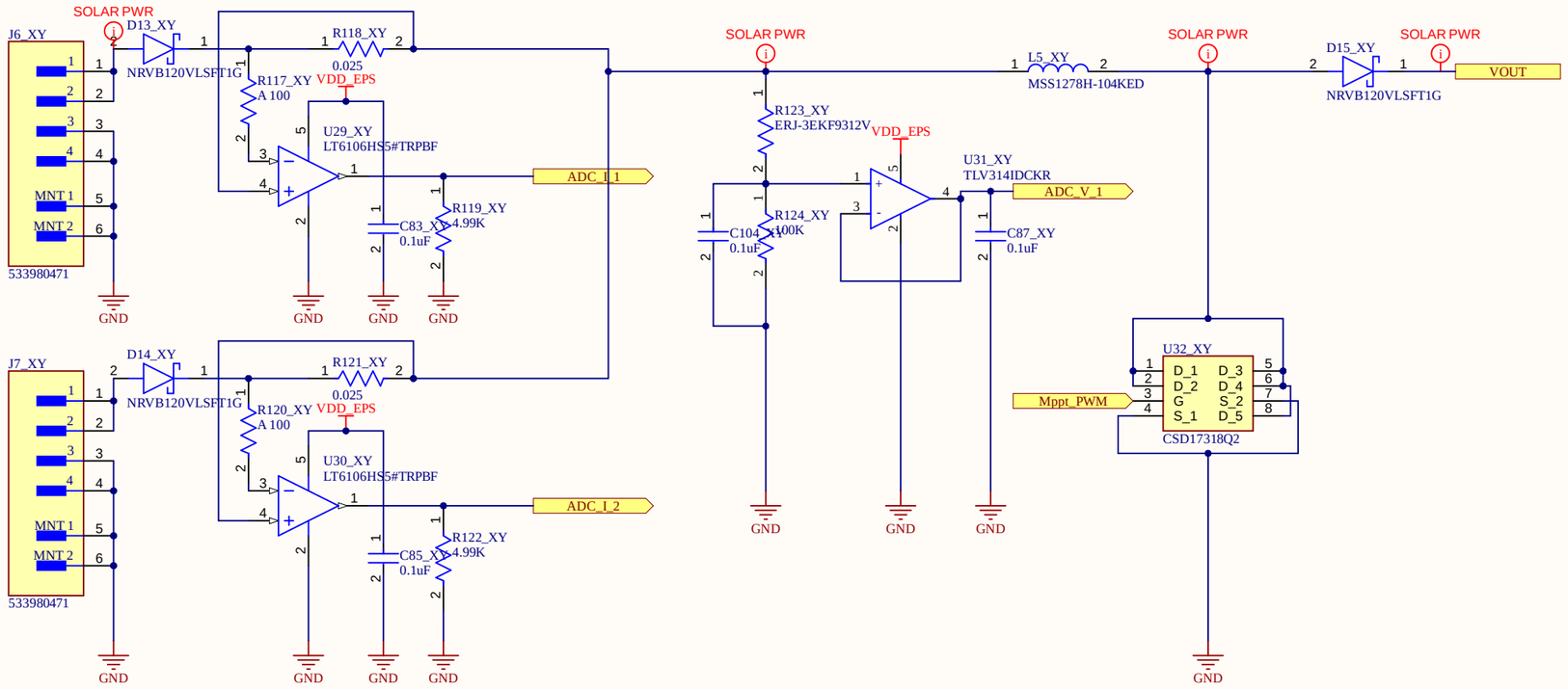
PROJECT REVISION: Version control disabled | DOCUMENT REVISION: | DESIGN ITEM: Version control disabled

TITLE *

SIZE	CAGE CODE	DWG NO.	REV
A3	?????	<SCH DWG NO>	

SCALE: | FILE NAME SolarMppt.SchDoc | SHEET 2 OF 21

REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
ENG: *	
DSN: *	
CHK: *	

REFERENCE DOCUMENTS

BOM:	<BOM DOC NO>
ASSY DWG:	<ASSY DWG NO>
FAB DWG:	<FAB DWG NO>
PCB DWG:	<PCB DWG NO>

PROJECT

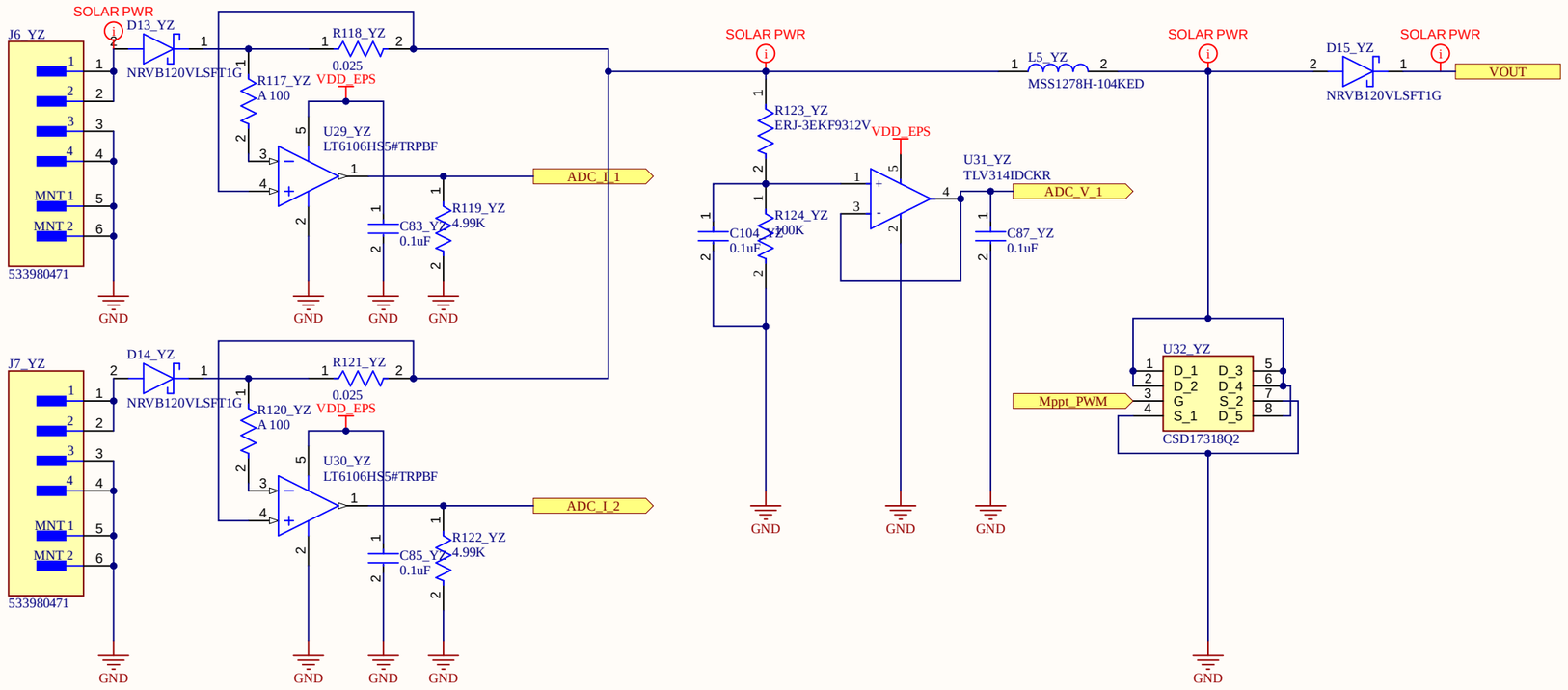
PROJECT REVISION: Version control disabled | DOCUMENT REVISION: | DESIGN ITEM: Version control disabled

TITLE *

SIZE	CAGE CODE	DWG NO.	REV
A3	?????	<SCH DWG NO>	

SCALE: | FILE NAME Panels.SchDoc | SHEET 3 OF 21

REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
ENG: *	
DSN: *	
CHK: *	

REFERENCE DOCUMENTS

BOM:	<BOM DOC NO>
ASSY DWG:	<ASSY DWG NO>
FAB DWG:	<FAB DWG NO>
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PROJECT

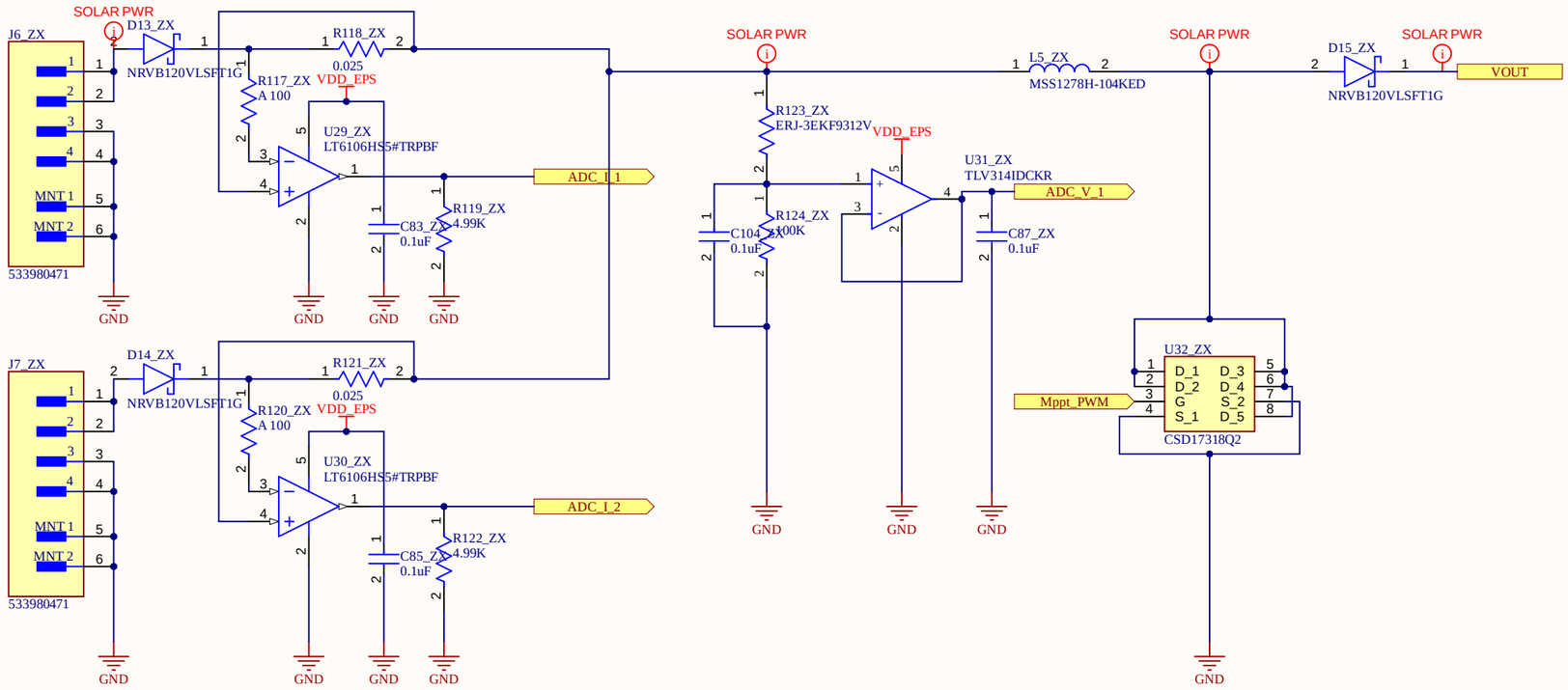
PROJECT REVISION: Version control disabled | DOCUMENT REVISION: Version control disabled | DESIGN ITEM:

TITLE *

SIZE	CAGE CODE	DWG NO.	REV
A3	?????	<SCH DWG NO>	

SCALE: | FILE NAME Panels.SchDoc | SHEET 3 OF 21

REVISION	DESCRIPTION	DATE	APPROVED



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ENG: *	
DSN: *	
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REFERENCE DOCUMENTS

BOM:	<BOM DOC NO>
ASSY DWG:	<ASSY DWG NO>
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PROJECT

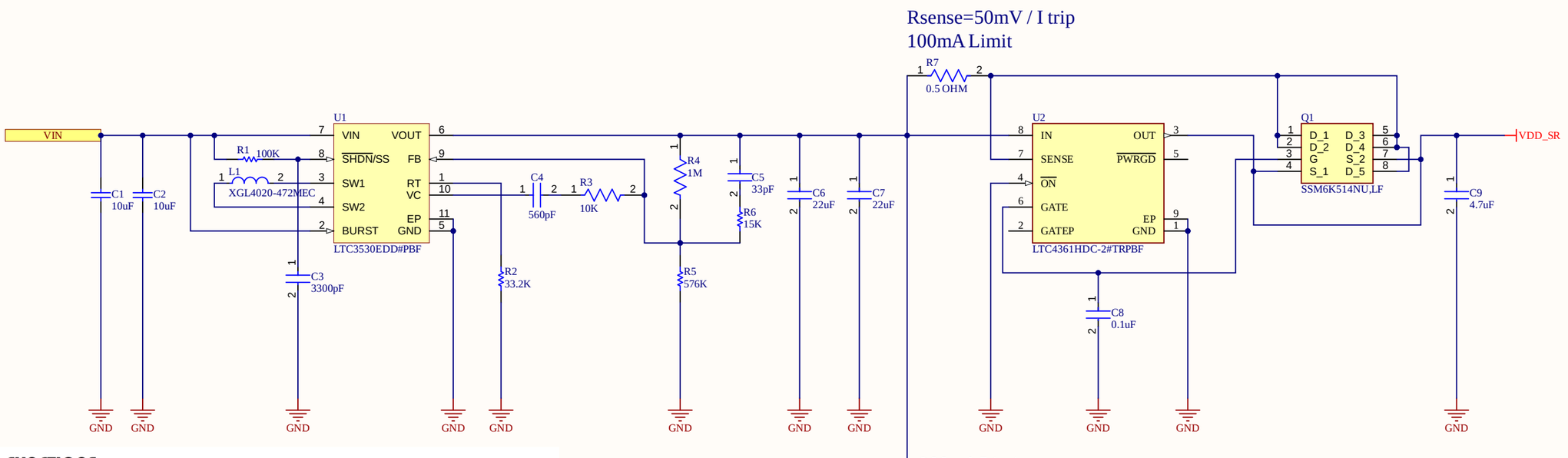
PROJECT REVISION: Version control disabled | DOCUMENT REVISION: Version control disabled | DESIGN ITEM:

TITLE *

SIZE	CAGE CODE	DWG NO.	REV
A3	?????	<SCH DWG NO>	

SCALE: | FILE NAME Panels.SchDoc | SHEET 3 OF 21

REVISION	DESCRIPTION	DATE	APPROVED



PIN FUNCTIONS

R_T (Pin 1): Programs the Frequency of the Internal Oscillator. Connect a resister from R_T to ground.

$f(kHz) = 33{,}170/R_T\ (k\Omega)$

BURST (Pin 2): Used to Set the Automatic Burst Mode Threshold. Connect a resistor and capacitor in parallel from this pin to ground. See the Applications Information section for component value selection. For manual control, ground the pin to force Burst Mode operation, connect to V_{IN} to force fixed frequency PWM mode.

SW1 (Pin 3): Switch Pin Where the Internal Switches A and B are Connected. Connect inductor from SW1 to SW2. An optional Schottky diode can be connnected from SW1 to ground for a moderate efficiency improvement. Minimize trace length to keep EMI down.

SW2 (Pin 4): Switch Pin Where the Internal Switches C and D are Connected. For applications with output voltages over 4.3V, a Schottky diode is required from SW2 to V_{OUT} to ensure the SW pin does not exhibit excessive voltage.

PIN FUNCTIONS

GND (Pin 5): Ground for the IC.

V_{OUT} (Pin 6): Output of the Synchronous Rectifier. A filter capacitor is placed from V_{OUT} to GND. A ceramic bypass capacitor is recommended as close to the V_{OUT} and GND pins as possible.

V_{IN} (Pin 7): Input Supply Voltage. Internal V_{CC} for the IC. A 10µF ceramic capacitor is recommended as close to the V_{IN} and GND pins as possible.

$\overline{SHDN}$/SS (Pin 8): Combined Soft-Start and Shutdown. Applied voltage <0.4V shuts down the IC. Tie to >1.4V to enable the IC and >1.6V to ensure the error amp is not clamped from soft-start. An R-C from the shutdown command signal to this pin will provide a soft-start function by limiting the rise time of V_C.

FB (Pin 9): Feedback Pin. Connect resistor divider tap here. The output voltage can be adjusted from 1.8V to 5.25V. The feedback reference is typically 1.215V.

$$V_{OUT} = 1.215V \bullet \left(1 + \frac{R1}{R2}\right)$$

V_C (Pin10): Error Amp Output. An R-C network is connected from this pin to FB for loop compensation. Refer to "Closing the Feedback Loop" section for component selection guidelines. During Burst Mode operation, V_C is internally clamped.

Exposed Pad (Pin 11, DD Package Only): Ground. This pin must be soldered to the PCB and electrically connected to ground.

APPROVALS	DATE
ENG: *	
DSN: *	
CHK: *	

REFERENCE DOCUMENTS

BOM: <BOM DOC NO>
ASSY DWG: <ASSY DWG NO>
FAB DWG: <FAB DWG NO>
PCB DWG: <PCB DWG NO>

PROJECT: Altium

PROJECT REVISION: Version control disabled | DOCUMENT REVISION: Version control disabled | DESIGN ITEM:

TITLE: *

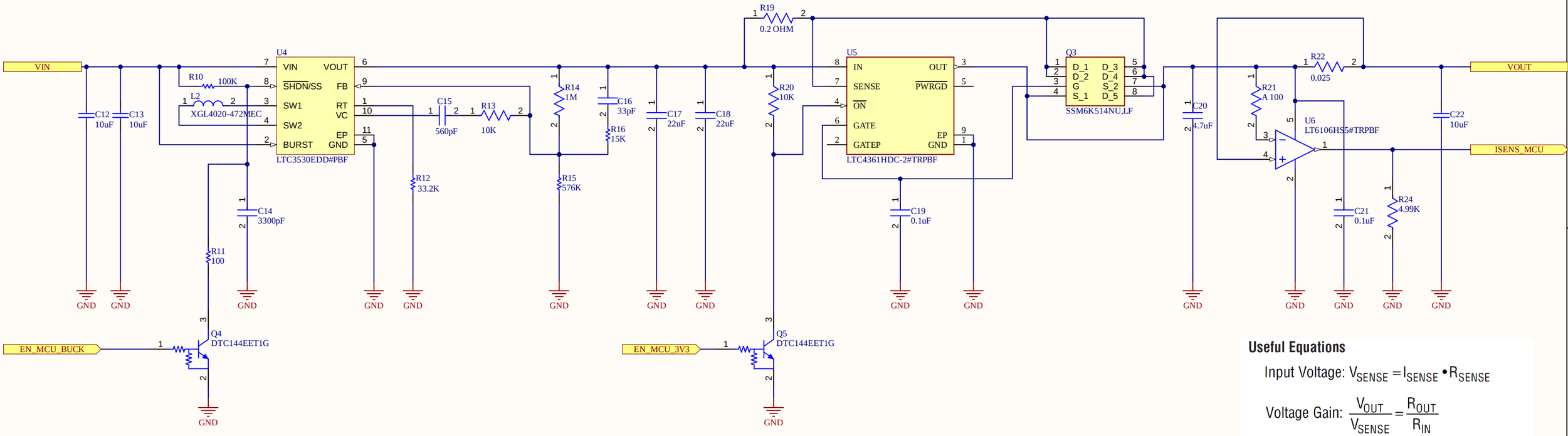
SIZE	CAGE CODE	DWG NO.	REV
A3	?????	<SCH DWG NO>	

SCALE: | FILE NAME: 3V3_EPS.SchDoc | SHEET 4 OF 21

REVISION	DESCRIPTION	DATE	APPROVED

<ASSY DWG NO>

Rsense=50mV / I trip
250mA Limit



Useful Equations

Input Voltage: $V_{SENSE} = I_{SENSE} \bullet R_{SENSE}$

Voltage Gain: $\frac{V_{OUT}}{V_{SENSE}} = \frac{R_{OUT}}{R_{IN}}$

Current Gain: $\frac{I_{OUT}}{I_{SENSE}} = \frac{R_{SENSE}}{R_{IN}}$

Transconductance: $\frac{I_{OUT}}{V_{SENSE}} = \frac{1}{R_{IN}}$

Transimpedance: $\frac{V_{OUT}}{I_{SENSE}} = R_{SENSE} \bullet \frac{R_{OUT}}{R_{IN}}$

APPROVALS	DATE
ENG: *	
DSN: *	
CHK: *	

REFERENCE DOCUMENTS

BOM:	<BOM DOC NO>
ASSY DWG:	<ASSY DWG NO>
FAB DWG:	<FAB DWG NO>
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PROJECT: Altium

PROJECT REVISION: Version control disabled | DOCUMENT REVISION: Version control disabled | DESIGN ITEM:

TITLE: *

SIZE	CAGE CODE	DWG NO.	REV
A3	?????	<SCH DWG NO>	

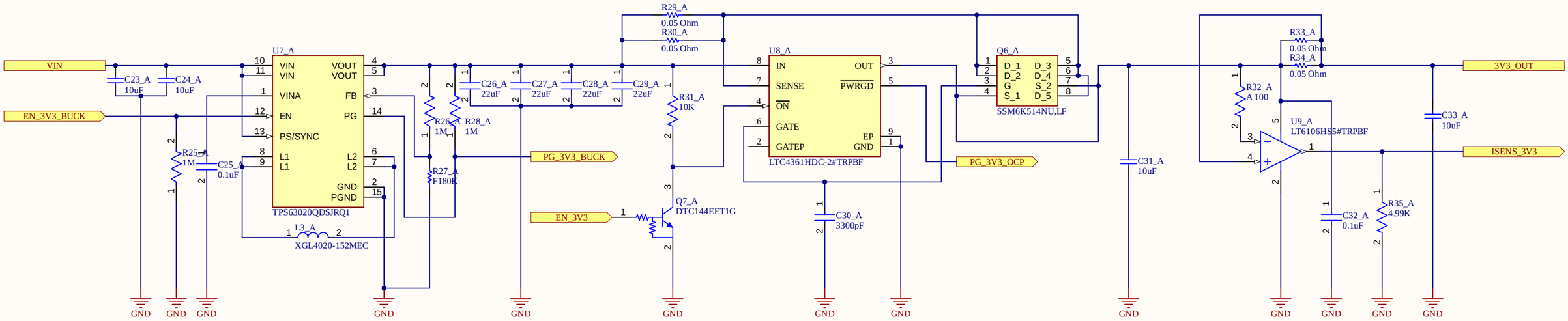
SCALE: | FILE NAME: 3V3_MCU.SchDoc | SHEET 5 OF 21

REVISION	DESCRIPTION	DATE	APPROVED

DWG NO <ASSY DWG NO>

REV

Rsense=50mV / I trip
2A Limit



APPROVALS	DATE
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DSN: *	
CHK: *	

REFERENCE DOCUMENTS

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PROJECT

Altium ™ * * * *

PROJECT REVISION: Version control disabled | DOCUMENT REVISION: Version control disabled | DESIGN ITEM:

TITLE

*

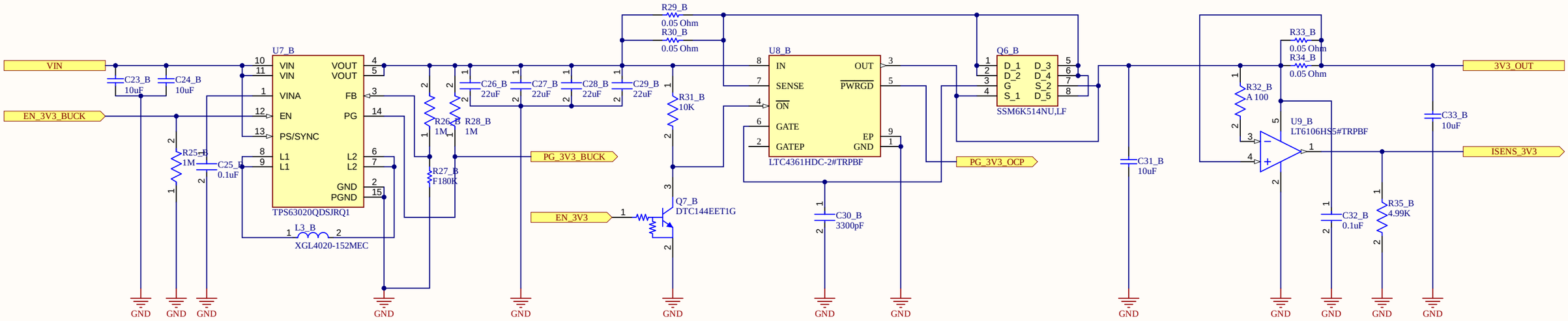
SIZE	CAGE CODE	DWG NO.	REV
A3	?????	<SCH DWG NO>	

SCALE: | FILE NAME 3V3_VoltageReg.SchDoc | SHEET 6 OF 21

REVISION	DESCRIPTION	DATE	APPROVED

ASSY DWG NO: <ASSY DWG NO>

Rsense=50mV / I trip
2A Limit



APPROVALS	DATE
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DSN: *	
CHK: *	

REFERENCE DOCUMENTS

BOM:	<BOM DOC NO>
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PCB DWG:	<PCB DWG NO>

PROJECT

Altium ™ * * * *

PROJECT REVISION: Version control disabled | DOCUMENT REVISION: Version control disabled | DESIGN ITEM:

TITLE

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SIZE	CAGE CODE	DWG NO.	REV
A3	?????	<SCH DWG NO>	

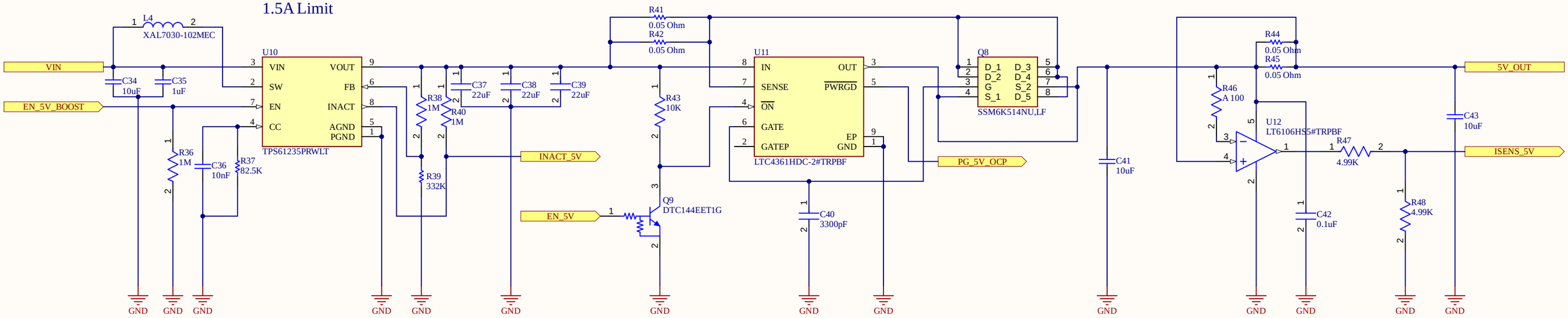
SCALE: | FILE NAME 3V3_VoltageReg.SchDoc | SHEET 6 OF 21

REVISION	DESCRIPTION	DATE	APPROVED

DWG NO <ASSY DWG NO>

Rsense=50mV / I trip
2A Limit

1.5A Limit



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PROJECT: Altium ™ * * * *

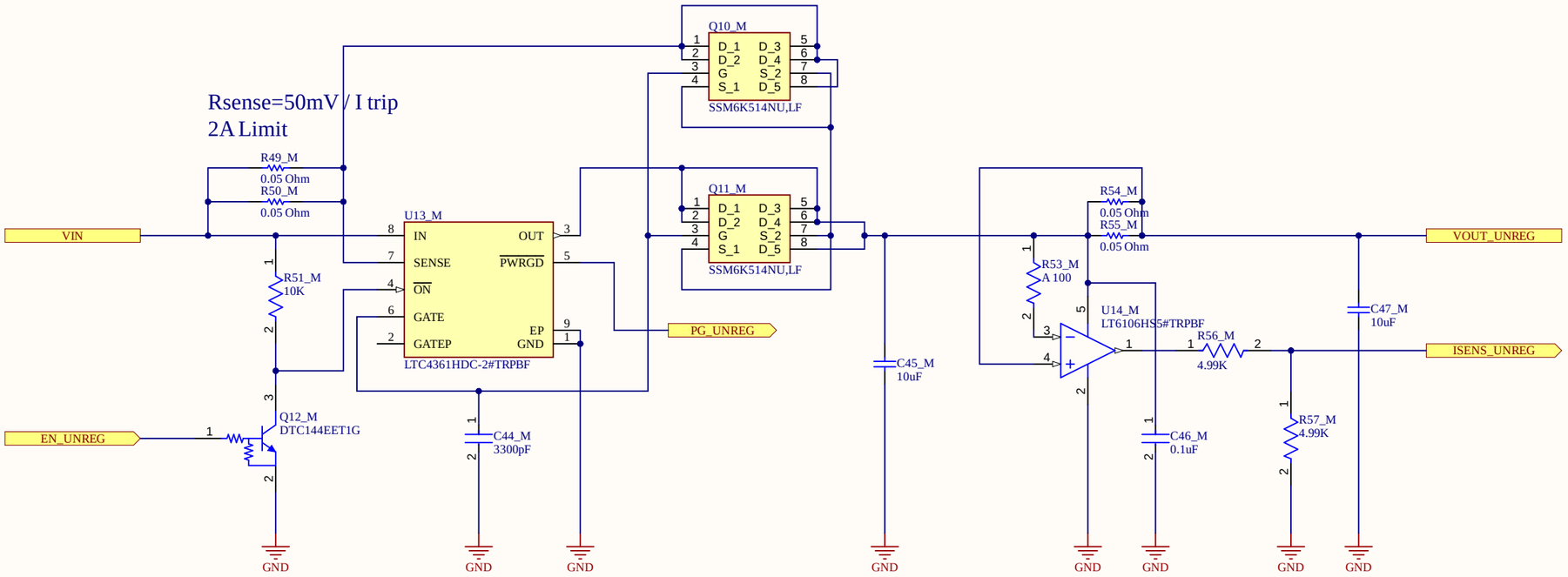
PROJECT REVISION: Version control disabled | DOCUMENT REVISION: | DESIGN ITEM: Version control disabled

TITLE: *

SIZE	CAGE CODE	DWG NO.	REV
A3	?????	<SCH DWG NO>	

SCALE: | FILE NAME: 5V0_VoltageReg.SchDoc | SHEET 7 OF 21

REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
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DSN: *	
CHK: *	

REFERENCE DOCUMENTS

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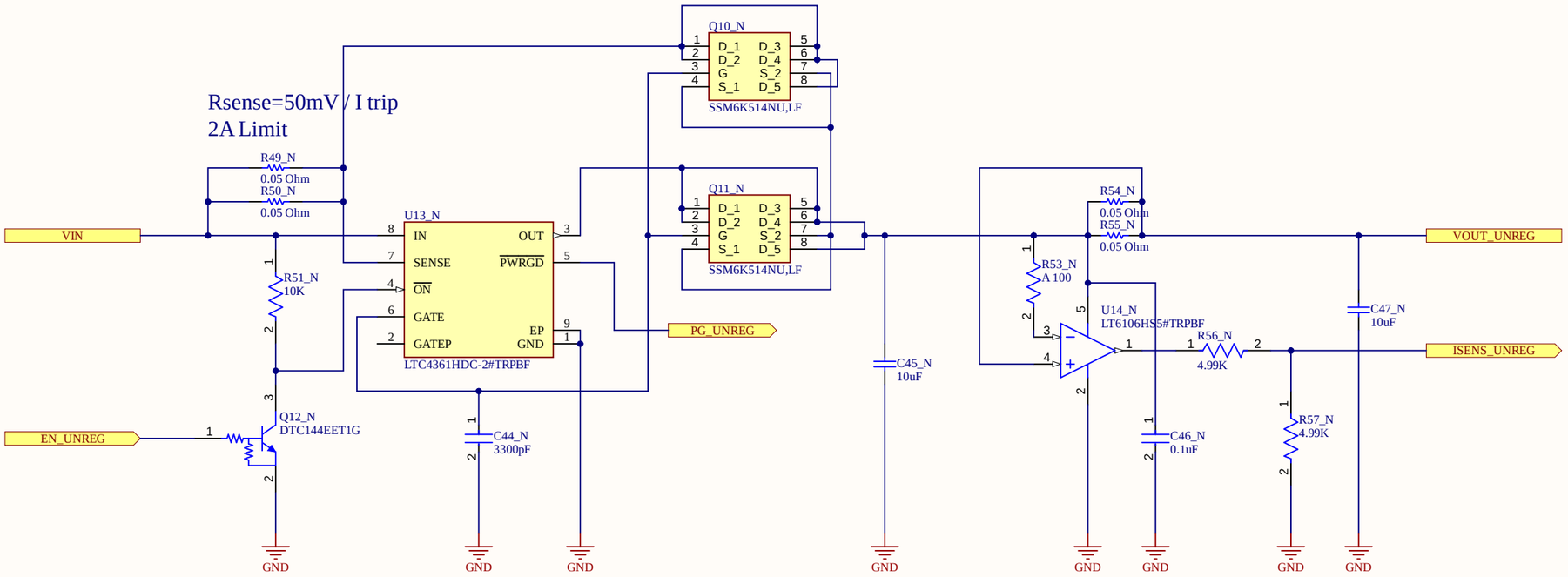
PCB DWG:	<PCB DWG NO>

PROJECT	Altium		
PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:	
TITLE	*		
SIZE: A3	CAGE CODE: ?????	DWG NO.: <SCH DWG NO>	REV:
SCALE:	FILE NAME: UnRegPower.SchDoc	SHEET: 8	OF: 21

Version control disabled Version control disabled

REVISION	DESCRIPTION	DATE	APPROVED



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REFERENCE DOCUMENTS

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PROJECT

PROJECT REVISION: Version control disabled DOCUMENT REVISION: Version control disabled DESIGN ITEM:

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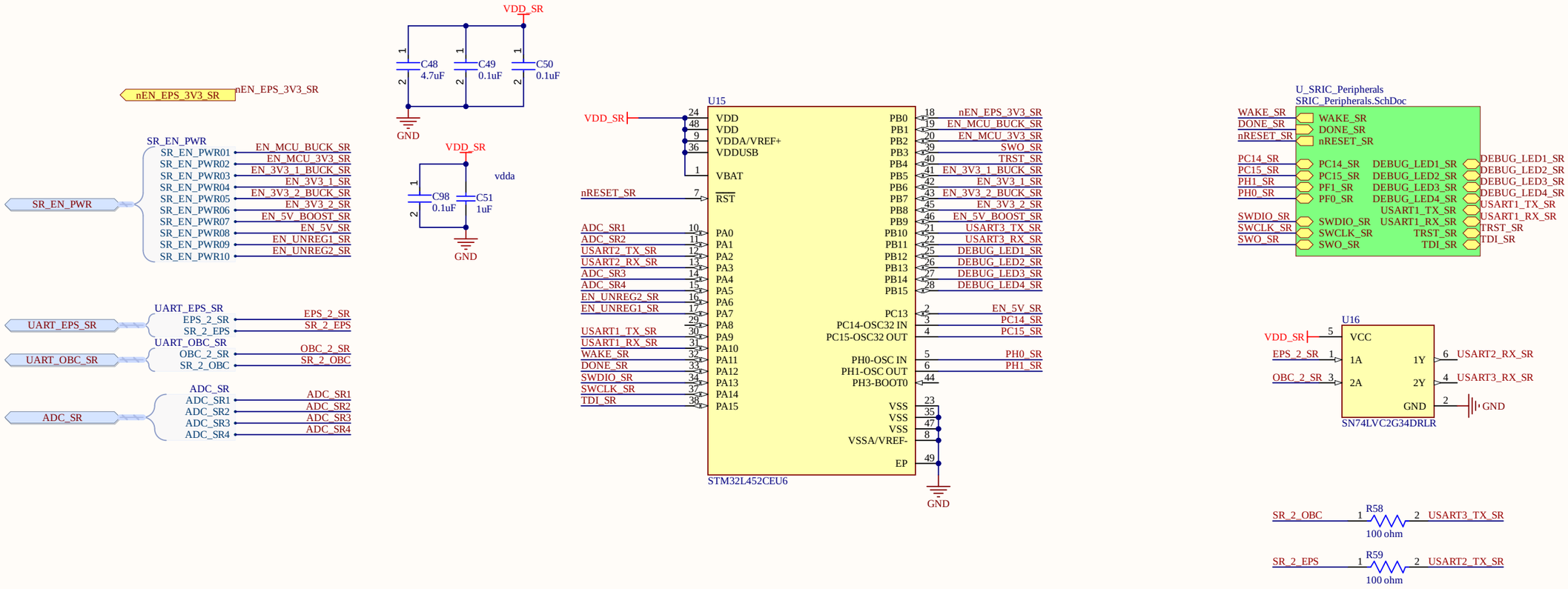
SIZE	CAGE CODE	DWG NO.	REV
A3	?????	<SCH DWG NO>	

SCALE: FILE NAME UnRegPower.SchDoc SHEET 8 OF 21

REVISION	DESCRIPTION	DATE	APPROVED

DWG NO <ASSY DWG NO>

REV



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PROJECT

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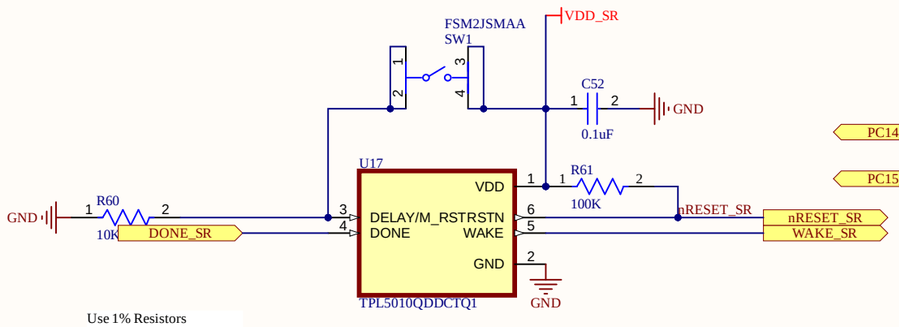
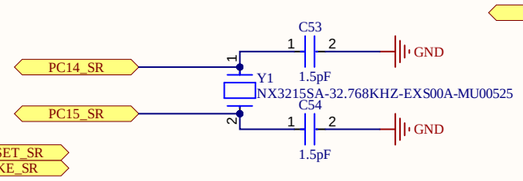
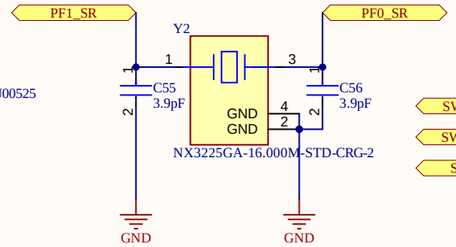
SIZE	CAGE CODE	DWG NO.	REV
A3	?????	<SCH DWG NO>	

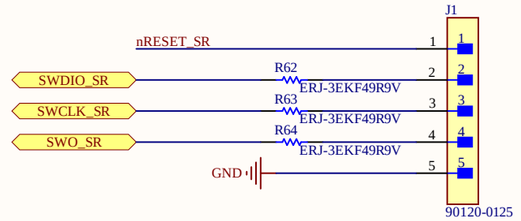
SCALE: FILE NAME SetResetIC.SchDoc SHEET 9 OF 21

REVISION	DESCRIPTION	DATE	APPROVED

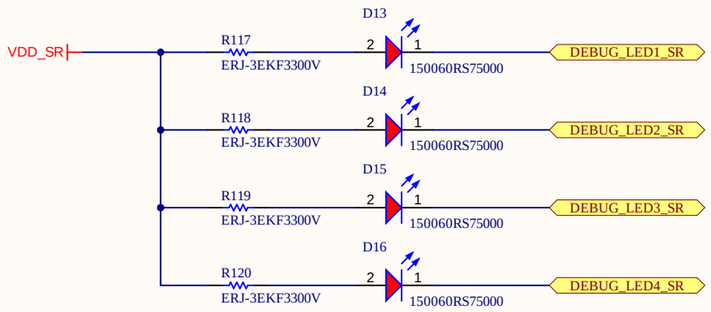


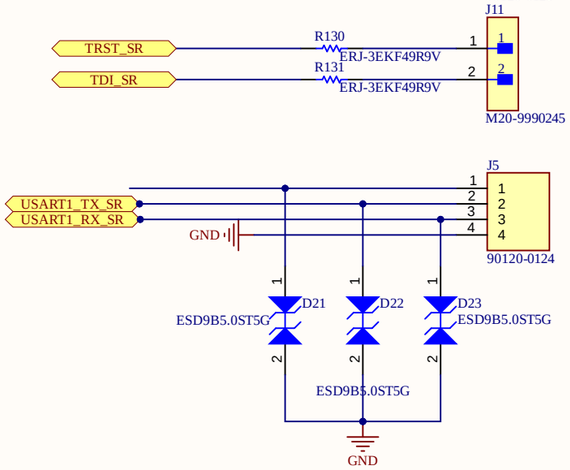






Use 1% Resistors
100 ms = 500 ohm
200 ms = 1000 ohm
300 ms = 1500 ohm
400 ms = 2000 ohm
500 ms = 2500 ohm
1 s = 5.2 Kohm
2 s = 6.79 Kohm
5 s = 8.85 Kohm
10 s = 11.20 Kohm





APPROVALS	DATE
ENG: *	
DSN: *	
CHK: *	

REFERENCE DOCUMENTS

BOM:	<BOM DOC NO>
ASSY DWG:	<ASSY DWG NO>
FAB DWG:	<FAB DWG NO>
PCB DWG:	<PCB DWG NO>

PROJECT: Altium *

PROJECT REVISION: Version control disabled | DOCUMENT REVISION: | DESIGN ITEM: Version control disabled

TITLE: *

SIZE	CAGE CODE	DWG NO.	REV
A3	?????	<SCH DWG NO>	

SCALE: | FILE NAME: SRIC_Peripherals.SchDoc | SHEET 10 OF 21

REVISION	DESCRIPTION	DATE	APPROVED

DWG NO <ASSY DWG NO>

PMIC_Watchdog
PMIC_Watchdog.SchDoc
DONE
nRESET
WAKE
DONE
nRST_WD
WAKE

PMIC_Power
PMIC_Power.SchDoc
nRESET
nRESET

MASTER_CAN
MASTER_CAN
CAN1
CAN1
RX
TX
CAN1_RX
CAN1_TX
CAN2
CAN2
RX
TX
CAN2_RX
CAN2_TX

QUAD_SPI
QUAD_SPI
IO0
IO1
CLK
NCS
QUADSPI_BK1_IO0
QUADSPI_BK1_IO1
QUADSPI_CLK
QUADSPI_BK1_NCS

UART_EPS_SR
UART_EPS_SR
SR_2_EPS
EPS_2_SR
SR_2_EPS
EPS_2_SR

UART_OBC_EPS
UART_OBC_EPS
OBC_2_EPS
EPS_2_OBC
OBC_2_EPS
EPS_2_OBC

UART4
UART4
RX
TX
UART4_RX
UART4_TX

EPS_EN_PWR
EPS_EN_PWR
EPS_EN_PWR01
EPS_EN_PWR02
EPS_EN_PWR03
EPS_EN_PWR04
EPS_EN_PWR05
EPS_EN_PWR06
EPS_EN_PWR07
EPS_EN_PWR08
EPS_EN_PWR09
EPS_EN_PWR10
EN_MCU_BUCK_EPS
EN_MCU_3V3_EPS
EN_3V3_1_BUCK_EPS
EN_3V3_1_EPS
EN_3V3_2_BUCK_EPS
EN_3V3_2_EPS
EN_5V_BOOST_EPS
EN_5V_EPS
EN_UNREG1_EPS
EN_UNREG2_EPS

I2C1
I2C1
SCL
SDA
I2C1_SCL
I2C1_SDA

OTG
OTG
DM
DP
ID
OTG_DM
OTG_DP
OTG_ID

TIM3
TIM3
TIM3_CH1
TIM3_CH2
TIM3_CH1
TIM3_CH2

U19
VDD_EPS
5
VCC
SR_2_EPS
1
1A
OBC_2_EPS
3
2A
1Y
6
USART2_RX
2Y
4
USART3_RX
GND
2
GND
SN74LVC2G34DRLR

EPS_2_SR
R65
1
2
USART2_TX
100 ohm
EPS_2_OBC
R66
1
2
USART3_TX
100 ohm

U18B
ADC1_IN5 23 PA0
ADC1_IN6 24 PA1
ADC1_IN7 25 PA2
ADC1_IN8 26 PA3
ADC1_IN9 29 PA4
ADC1_IN10 30 PA5
ADC1_IN11 31 PA6
ADC1_IN12 32 PA7
WAKE 67 PA8
USART1_TX 68 PA9
OTG_ID 69 PA10
OTG_DM 70 PA11
OTG_DP 71 PA12
SWDIO 72 PA13
SWCLK 76 PA14
TDI 77 PA15
ADC1_IN15 35 PB0
ADC1_IN16 36 PB1
DONE 37 PB2
SWO 89 PB3
TRST 90 PB4
91 PB5
I2C1_SCL 92 PB6
USART1_RX 93 PB7
95 PB8
I2C1_SDA 96 PB9
USART3_TX 47 PB10
USART3_RX 48 PB11
CAN2_RX 51 PB12
CAN2_TX 52 PB13
SPI2_MISO 53 PB14
SPI2_MOSI 54 PB15
PC0 15 ADC3_IN1
PC1 16 ADC3_IN2
PC2 17 ADC3_IN3
PC3 18 ADC3_IN4
PC4 33 ADC1_IN13
PC5 34 ADC1_IN14
PC6 63 TIM3_CH1
PC7 64 TIM3_CH2
PC8 65 PG_3V3_1_BUCK
PC9 66 PG_3V3_1_OCP
PC10 78 UART4_TX
PC11 79 UART4_RX
PC12 80 PG_3V3_2_BUCK
PC13 7 PG_3V3_2_OCP
PC14-OSC32 IN 8 PC14
PC15-OSC32 OUT 9 PC15
PD0 81 CAN1_RX
PD1 82 CAN1_TX
PD2 83 5V_INACT
PD3 84 SPI2_SCK
PD4 85 5V_OCP-PG
PD5 86 USART2_TX
PD6 87 USART2_RX
PD7 88 DEBUG_LED1
PD8 55 DEBUG_LED2
PD9 56 DEBUG_LED3
PD10 57 DEBUG_LED4
PD11 58 DEBUG_LED5
PD12 59 TIM4_CH1
PD13 60 TIM4_CH2
PD14 61 TIM4_CH3
PD15 62
STM32L496VGT6

U18C
EN_MCU_BUCK_EPS 97 PE0
EN_MCU_3V3_EPS 98 PE1
EN_3V3_1_BUCK_EPS 2 PE2
EN_3V3_1_EPS 3 PE3
EN_3V3_2_BUCK_EPS 4 PE4
EN_3V3_2_EPS 5 PE5
EN_5V_BOOST_EPS 36 PE6
EN_5V_EPS 39 PE7
EN_UNREG1_EPS 40 PE8
EN_UNREG2_EPS 41 PE9
QUADSPI_CLK 42 PE10
QUADSPI_BK1_NCS 43 PE11
QUADSPI_BK1_IO0 44 PE12
QUADSPI_BK1_IO1 45 PE13
PG_UNREG1 46 PE14
PG_UNREG2 PE15
PH0-OSC IN 12 PH0
PH1-OSC OUT 13 PH1
PH3-BOOT0 94
STM32L496VGT6

EPS_GPIO
ADC3_IN1 ISENS_MCU EPS_GPIO01
PG_3V3_1_BUCK EPS_GPIO02
PG_3V3_1_OCP EPS_GPIO03
ADC3_IN2 ISENS_3V3_1 EPS_GPIO04
PG_3V3_2_BUCK EPS_GPIO05
PG_3V3_2_OCP EPS_GPIO06
ADC3_IN3 ISENS_3V3_2 EPS_GPIO07
5V_INACT EPS_GPIO08
5V_OCP-PG EPS_GPIO09
ADC3_IN4 ISENS_5V EPS_GPIO10
PG_UNREG1 EPS_GPIO11
ADC1_IN5 ISENS_UNREG1 EPS_GPIO12
PG_UNREG2 EPS_GPIO13
ADC1_IN6 ISENS_UNREG2 EPS_GPIO14
EPS_GPIO

DEBUG
JTAG
nRESET
SWCLK
SWDIO
SWO
TRST
TDI
JTAG
USART1
USART1_TX
USART1_RX
TX
RX
DEBUG_UART
DEBUG_LED
DEBUG_LED1
DEBUG_LED2
DEBUG_LED3
DEBUG_LED4
DEBUG_LED5
DEBUG_LED
PMIC_Debug
PMIC_Debug.SchDoc
DEBUG

SOLAR_ADC
ADC1_IN8 ADC_Iout_X+
ADC1_IN9 ADC_Iout_Y-
ADC1_IN10 ADC_Vout_XY
ADC1_IN11 ADC_Iout_Z+
ADC1_IN12 ADC_Iout_X-
ADC1_IN13 ADC_Vout_ZX
ADC1_IN14 ADC_Iout_Y+
ADC1_IN15 ADC_Iout_Z-
ADC1_IN16 ADC_Vout_YZ
ADC1_IN7 ADC_Vout_Panels
SOLAR_ADC

Mppt_PWM
TIM4_CH1 Mppt_PWM1
TIM4_CH2 Mppt_PWM2
TIM4_CH3 Mppt_PWM3
Mppt_PWM1

PMIC_Crystal
PMIC_Crystal.SchDoc
PC14
PC15
PC14
PC15
PH0
PH1
PH0
PH1

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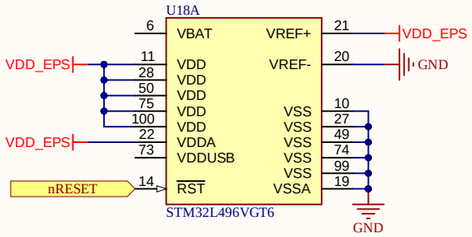

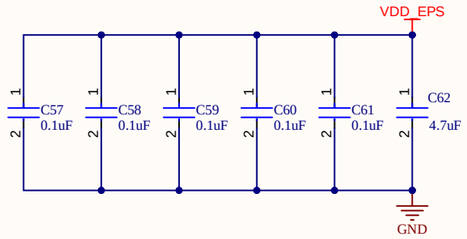

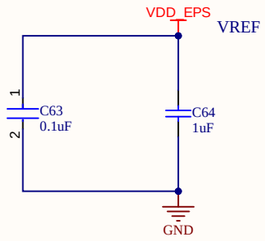

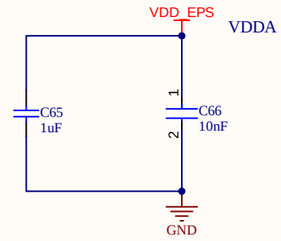

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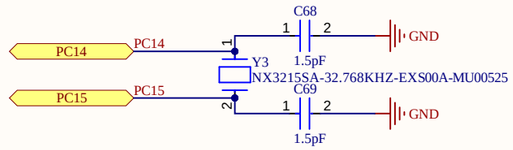

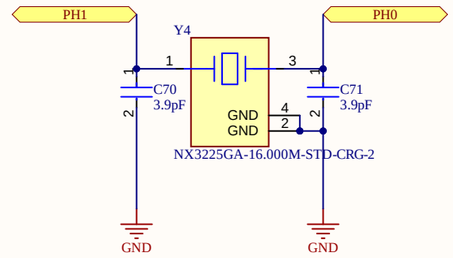

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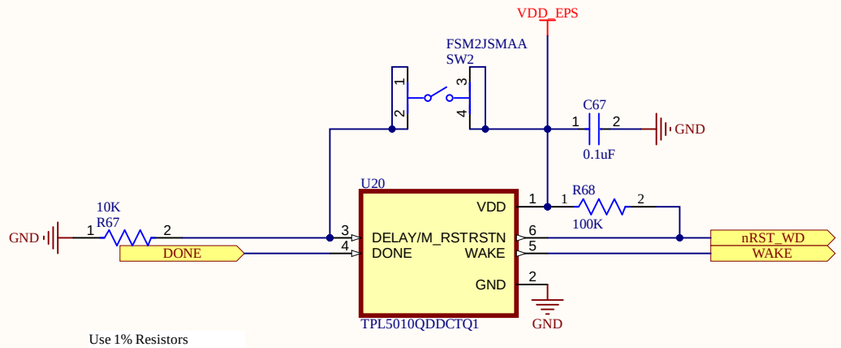

Use 1% Resistors
100 ms = 500 ohm
200 ms = 1000 ohm
300 ms = 1500 ohm
400 ms = 2000 ohm
500 ms = 2500 ohm
1 s = 5.2 Kohm
2 s = 6.79 Kohm
5 s = 8.85 Kohm
10 s = 11.20 Kohm

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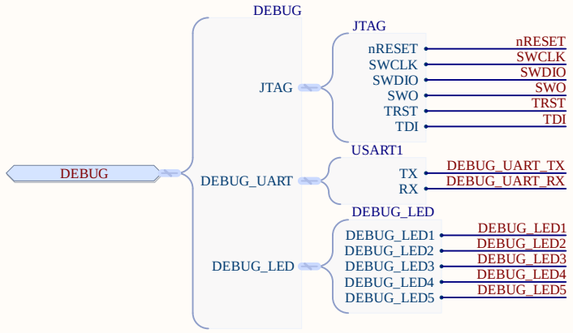

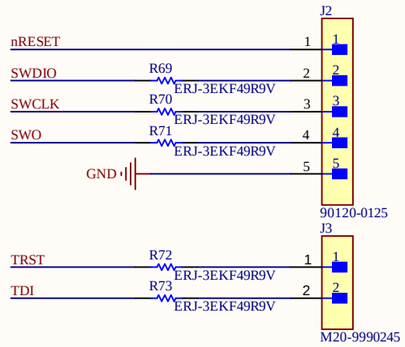

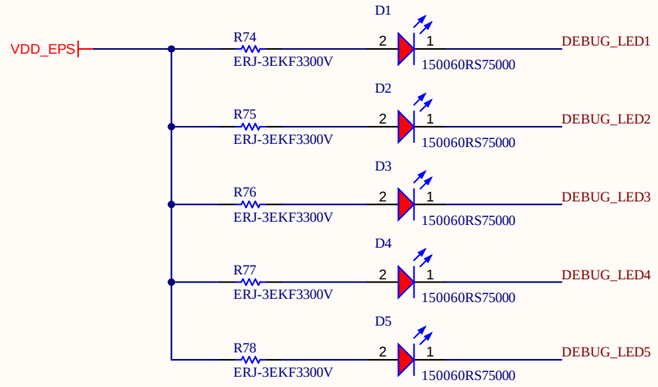

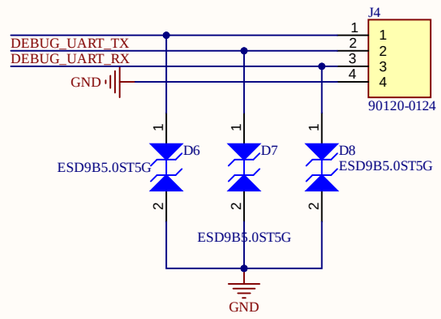

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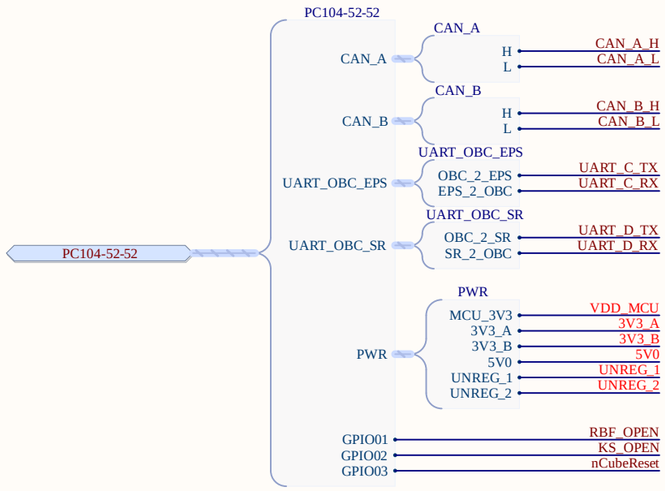

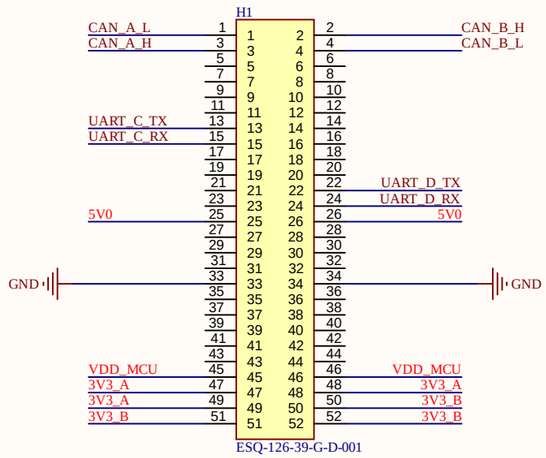

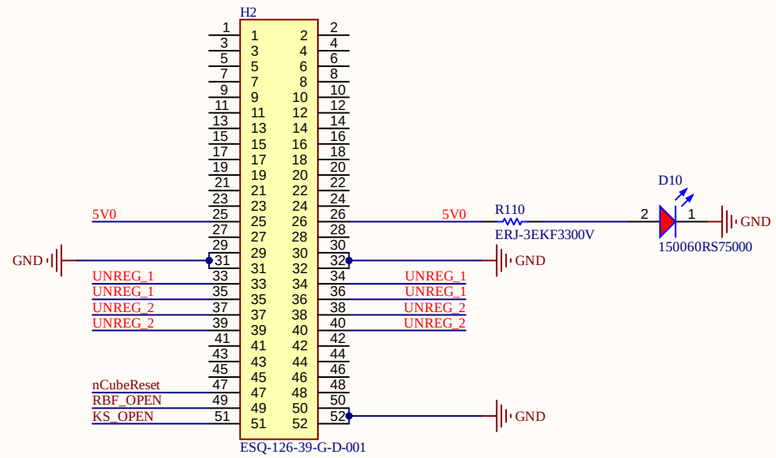

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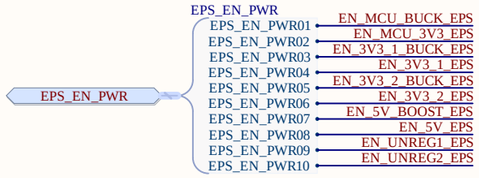

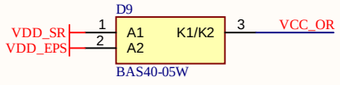

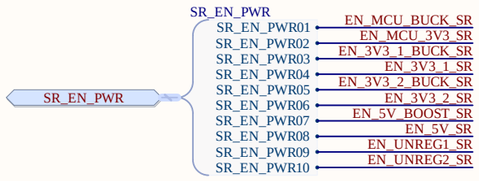

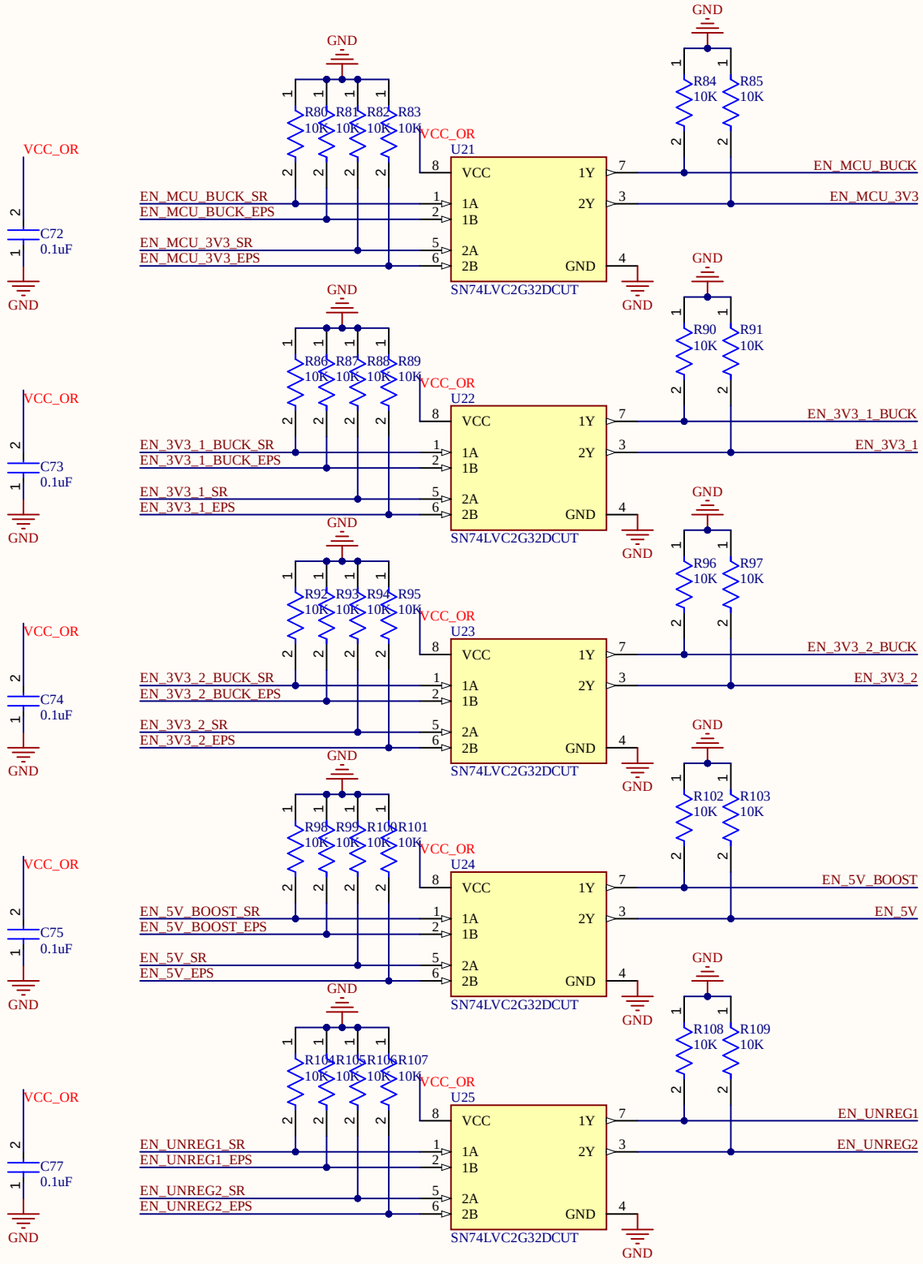

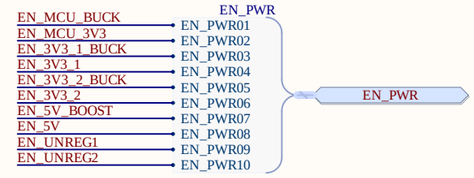

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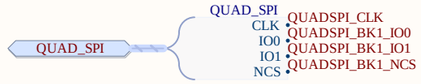

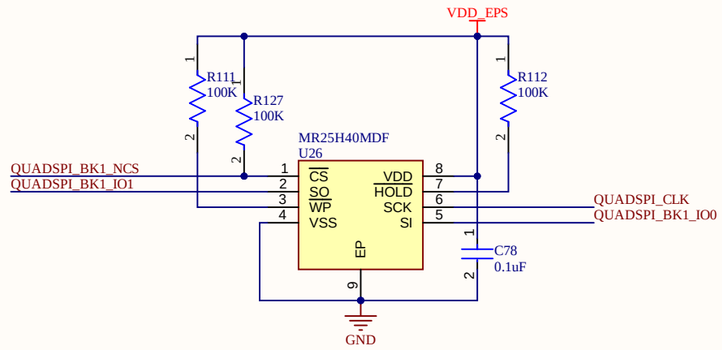

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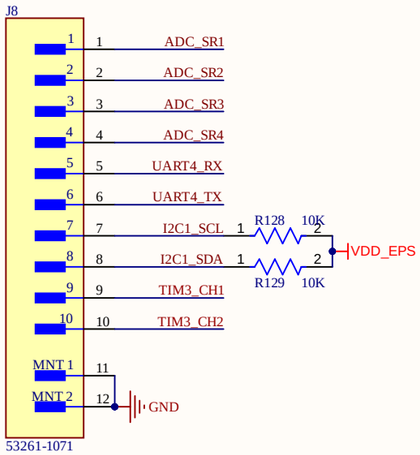

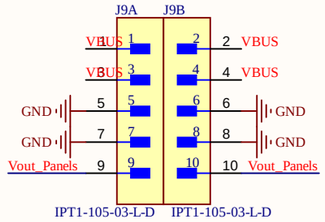

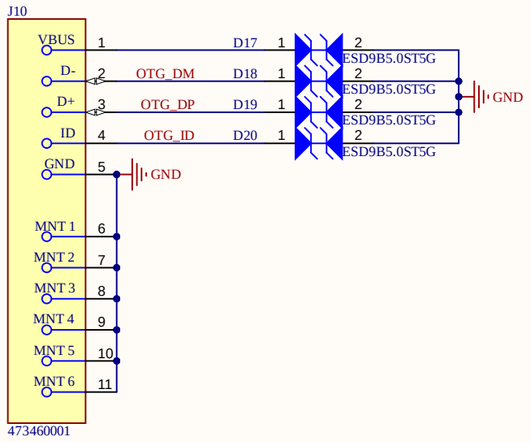

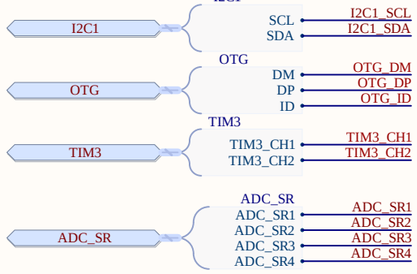

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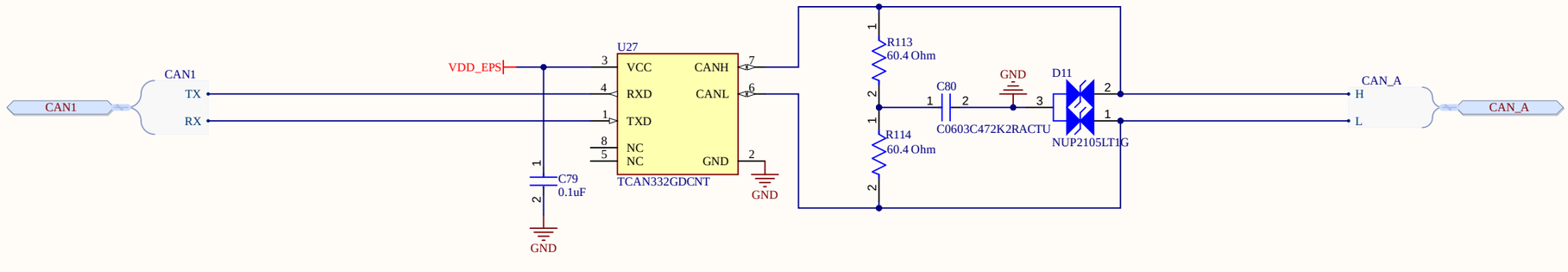

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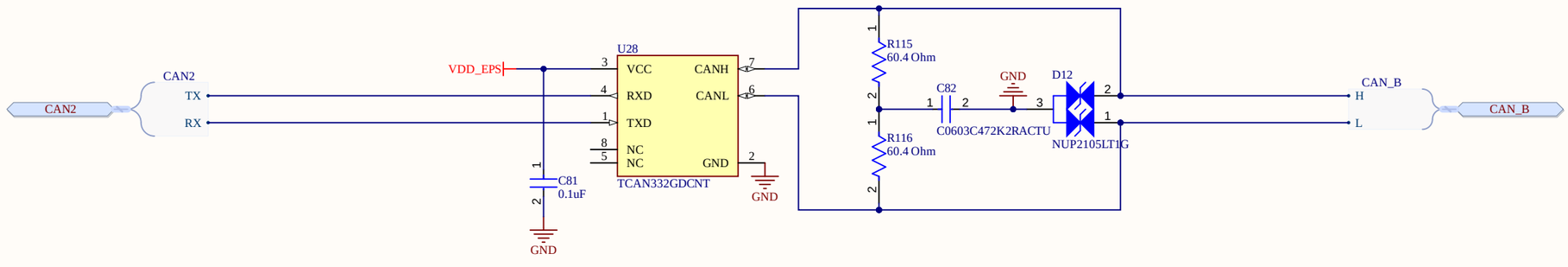

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