Practical Report - 6 IE1024 - Computer Organization and Architecture 1st year 2nd semester - 2024

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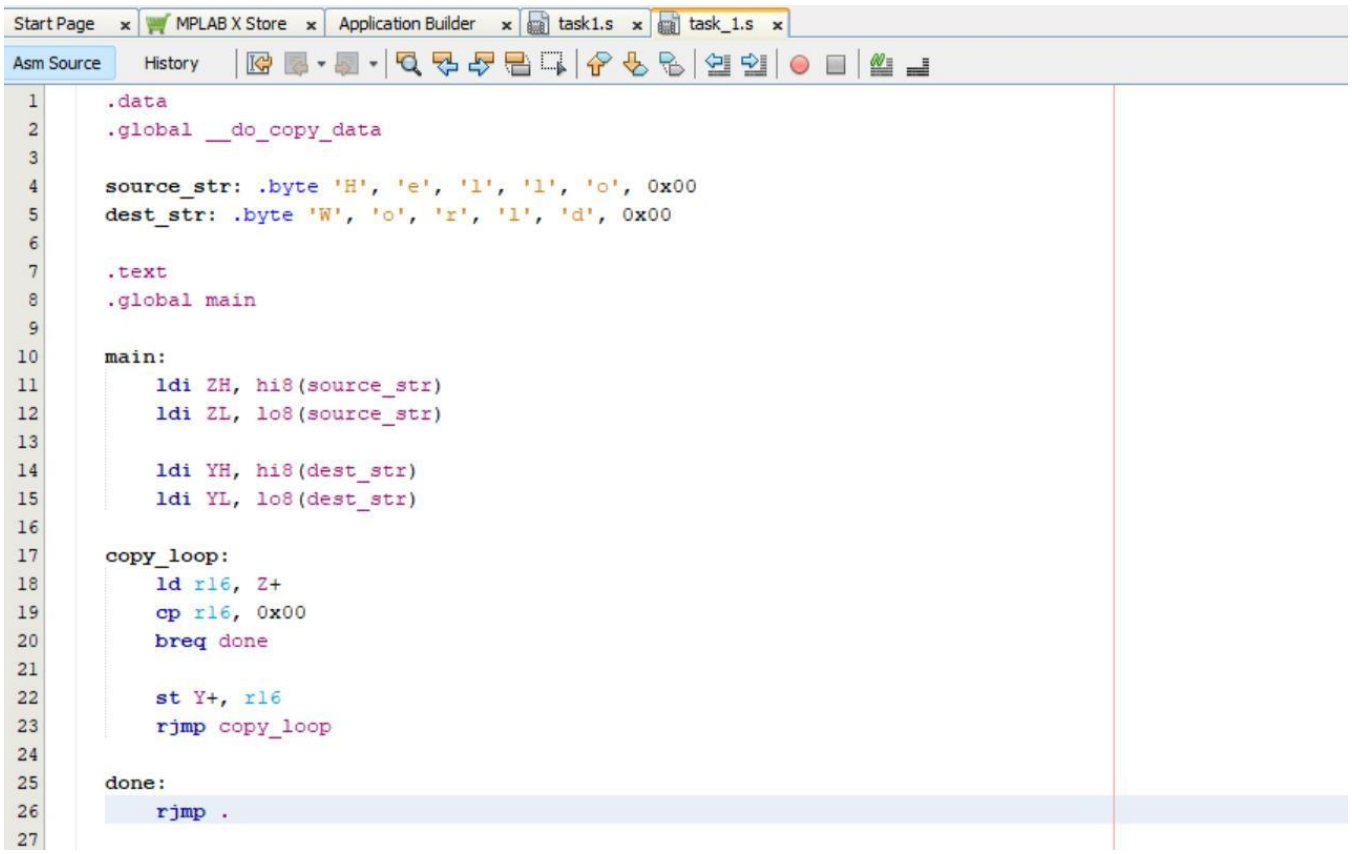
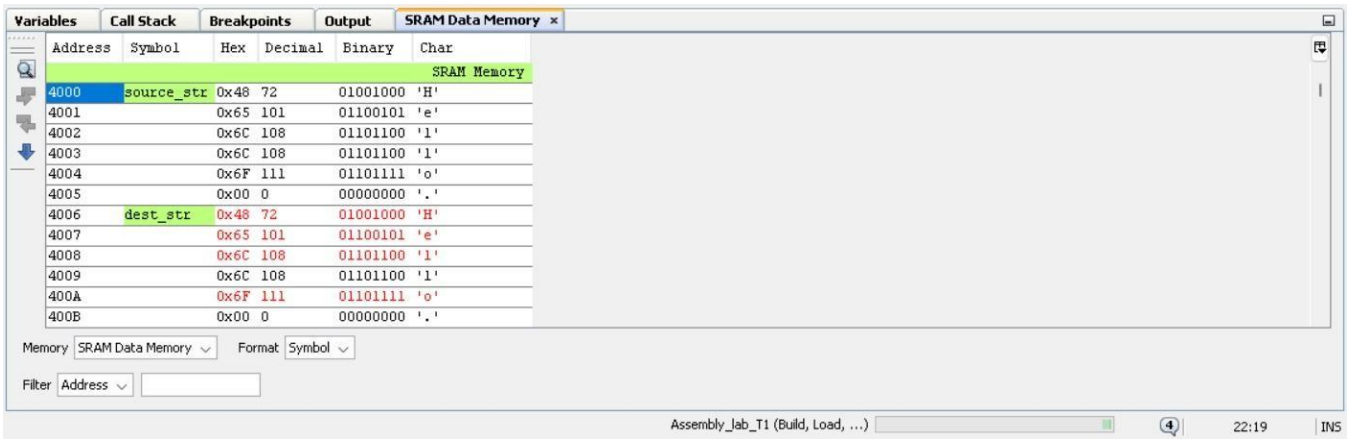
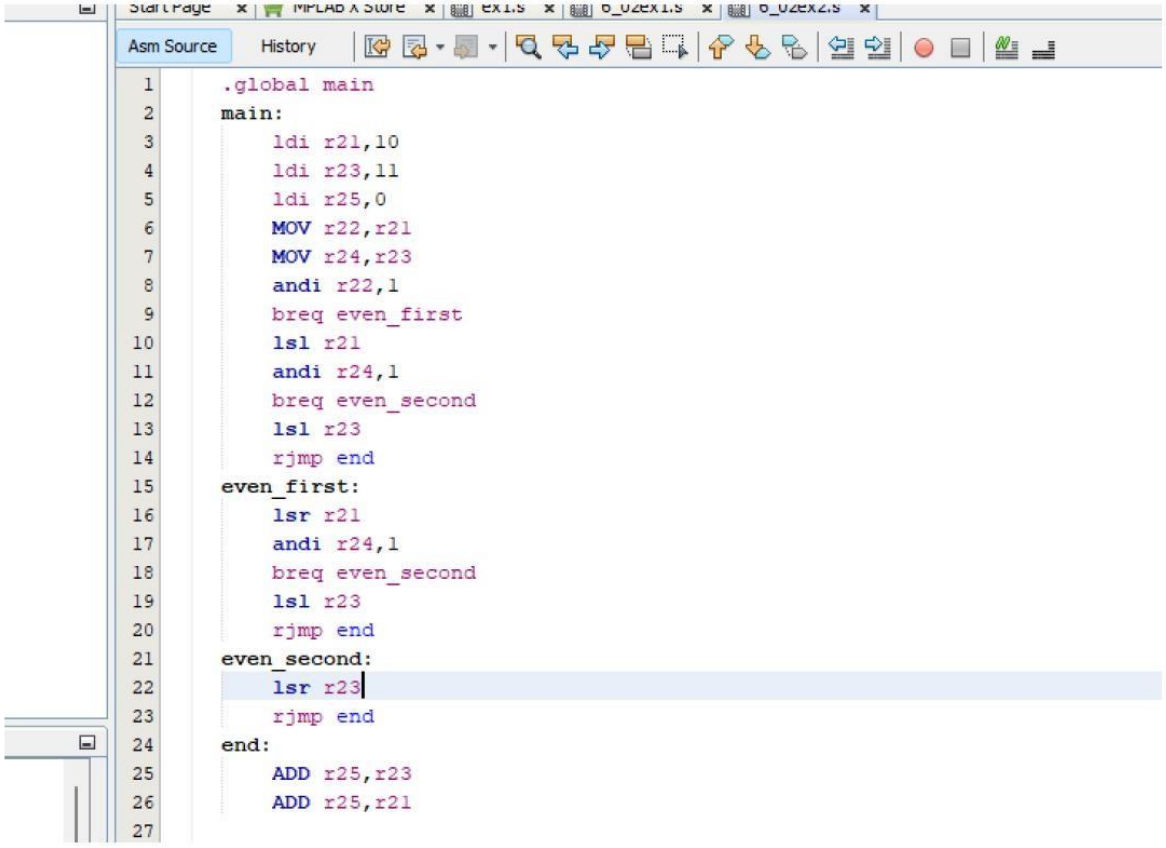
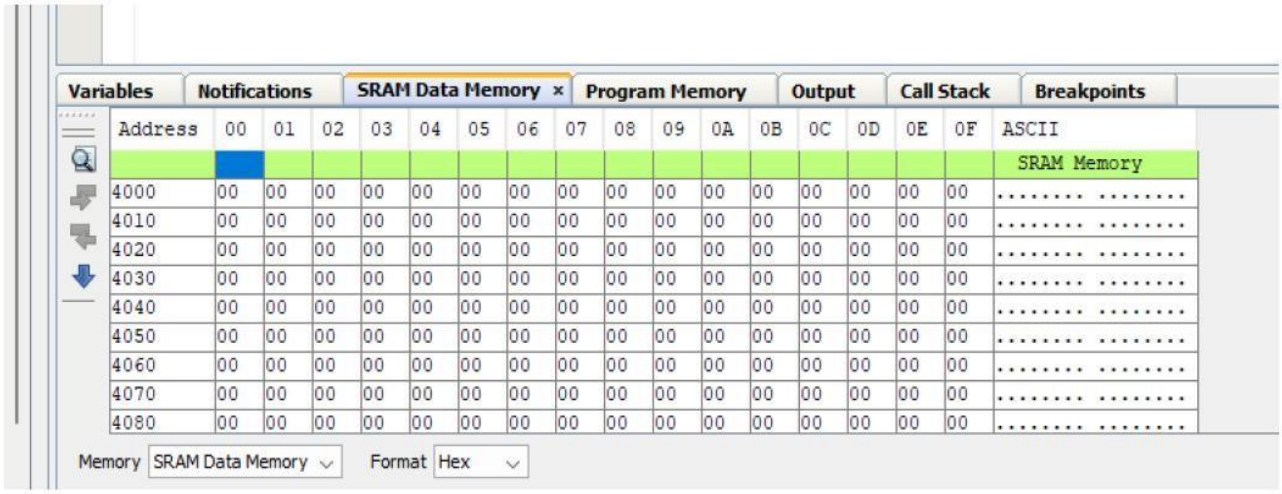
Task-01


Start Page
MPLAB X Store
Application Builder
task1.s
task_1.s
Asm Source
History
.data
.global __do_copy_data
source_str: .byte 'H', 'e', 'l', 'l', 'o', 0x00
dest_str: .byte 'W', 'o', 'r', 'l', 'd', 0x00
.text
.global main
main:
ldi ZH, hi8(source_str)
ldi ZL, lo8(source_str)
ldi YH, hi8(dest_str)
ldi YL, lo8(dest_str)
copy_loop:
ld r16, Z+
cp r16, 0x00
breq done
st Y+, r16
rjmp copy_loop
done:
rjmp .


Variables
Call Stack
Breakpoints
Output
SRAM Data Memory
Address Symbol Hex Decimal Binary Char
SRAM Memory
4000 source_str 0x48 72 01001000 'H'
4001 0x65 101 01100101 'e'
4002 0x6C 108 01101100 'l'
4003 0x6C 108 01101100 'l'
4004 0x6F 111 01101111 'o'
4005 0x00 0 00000000 '.'
4006 dest_str 0x48 72 01001000 'H'
4007 0x65 101 01100101 'e'
4008 0x6C 108 01101100 'l'
4009 0x6C 108 01101100 'l'
400A 0x6F 111 01101111 'o'
400B 0x00 0 00000000 '.'
Memory SRAM Data Memory
Format Symbol
Filter Address
Assembly_lab_T1 (Build, Load, ...)
22:19
INS

Task-02


Asm Source
History
1 .global main
2 main:
3 ldi r21,10
4 ldi r23,11
5 ldi r25,0
6 MOV r22,r21
7 MOV r24,r23
8 andi r22,1
9 breq even_first
10 lsl r21
11 andi r24,1
12 breq even_second
13 lsl r23
14 rjmp end
15 even_first:
16 lsr r21
17 andi r24,1
18 breq even_second
19 lsl r23
20 rjmp end
21 even_second:
22 lsr r23
23 rjmp end
24 end:
25 ADD r25,r23
26 ADD r25,r21
27


Variables
Notifications
SRAM Data Memory ×
Program Memory
Output
Call Stack
Breakpoints
Address 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F ASCII
SRAM Memory
4000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 ....
4010 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 ....
4020 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 ....
4030 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 ....
4040 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 ....
4050 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 ....
4060 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 ....
4070 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 ....
4080 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 ....
Memory SRAM Data Memory
Format Hex