# Electronics/Mechanics

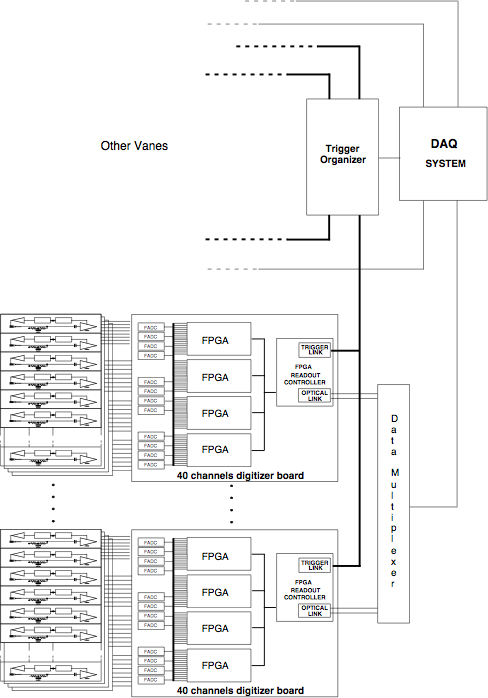


Figure 1.5.1 *Overall scheme of the calorimeter electronics*.

The overall scheme for the calorimeter readout electronics is shown in **Error! Reference source not found.**. The front end electronics, FEE, consists of two discrete and independent chips, Amp-HV, for each crystal, directly connected to the back of the photo-sensor pins, providing both the amplification stage and a local linear regulation for the photo-sensor bias voltage. For each crystal, the Amp-HV are named and organized differently (Left or Right) depending on their positioning with respect to the crystal center. Each disk is subdivided in twelve similar sectors along the azimuthal angle; each sector corresponding to 78 crystals. Groups of 16 Left (Right) Amp-HV chips are controlled by a dedicated ARM controller that distributes the LV and the HV reference value, while setting and reading back the locally regulated voltage. Each sector is therefore controlled by a 2 x 5 ARMs. Groups of 16 amplified signals are then sent to a digitizer module, where they are sampled and processed before being optically transferred to the DAQ system.

The requirements for the preamplifier are the following: (i) to provide a high amplification of the signal while maintaining a fast signal in output to keep the required performance in timing, energy and in pileup rejection, (ii) to keep a low detection threshold at the MeV level, (iii) to work in a rate environment of 200 kHz/channel while sustaining the rate coming from the beam flash and (iv) to have a reduced power consumption.

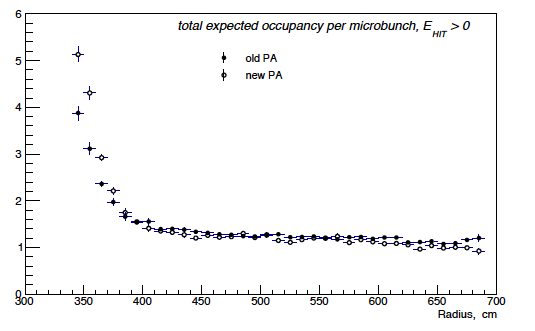
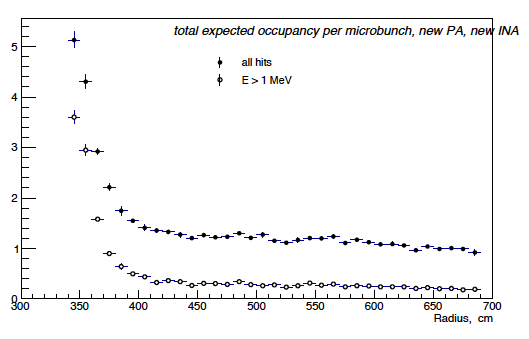


Figure 1.5.2 *(Left) Occupancy plot/crystal/microbunch as a function of the calorimeter radius, (right) dependence of the occupancy from the applied threshold.*

The distribution of hits in the calorimeter is due to two sources: (i) a flash of particles produced, within 200 ns from the proton generation, by the interaction of the beam in the production target and by the following decays and interactions with the surrounding material and (ii) the background events generated by the muon beam interacting with the target and the beam-dump. From our simulation, the sum of the *prompt* beam flash hits per channel corresponds to an equivalent energy deposition of ~ 5 MeV for each micro-bunch. For the second background source, the arrival time of the related beam background follows an exponential decay curve with a τ similar to the signal. The most abundant background source is that from the neutrons generated by the muon capture, that originates occupancy larger than 1 hit/channel. In Figure 1.5.2.left, the calorimeter cell occupancy as a function of the radius is shown. In Figure 1.5.2.right, the occupancy get reduced to ~ 10% when applying a 1 MeV threshold. From the electronics point of view, the contribution of this environmental background corresponds to an average current, in input to the photo-sensors, which is dominated by the beam flash and is equivalent to: I = Npe ⋅MBR⋅ e, where Npe is the average number of photoelectrons, NVR is the Micro-bunch rate and e is the elementary electrical charge. In the Lyso case, using Npe= 5 MeV x ( 2000 p.e,/MeV) = 10000, MBR = 200 x103 Hz, we obtain I=200 pA; this translates to 10 pA in the BaF2 case. The typical APD dark current ranges from 10 to 100 nA when working at the operation point of gain = 50. For the Lyso case the beam flash related current is comparable to the leakage current while it is practically negligible for the BaF2. In case of a much higher beam flash dose, we foresee to implement a scheme of regulating the bias voltage with respect to the micro-bunch gating to lower by 10 V the setting in the first 200 ns and ramping back to full bias in the next 100 ns.

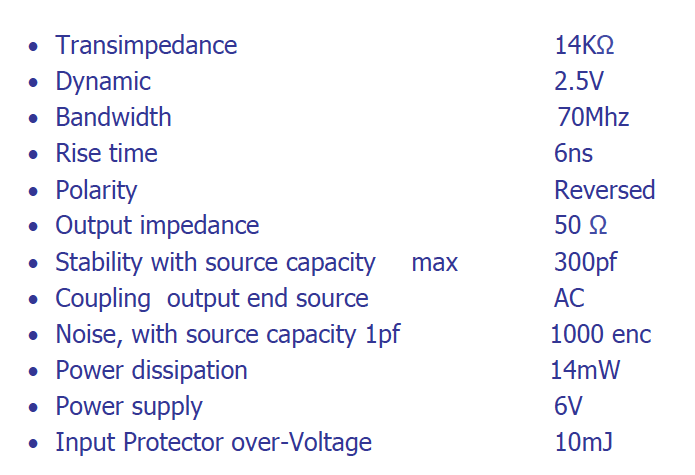
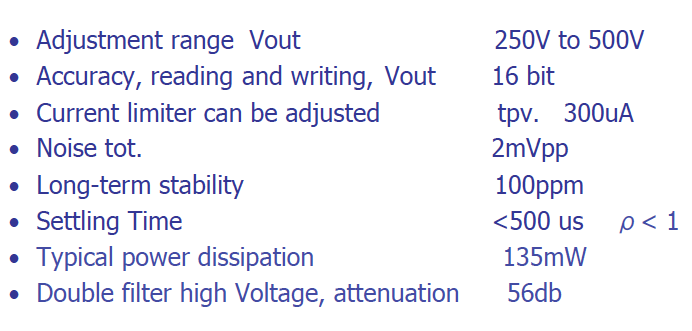
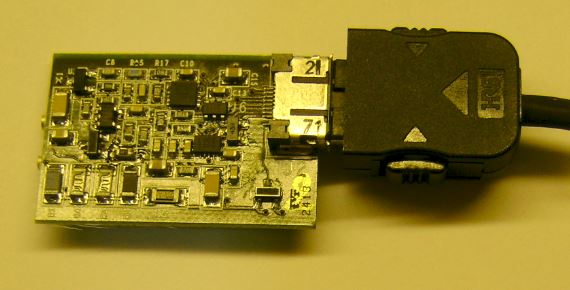
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Table *Characteristics of the Amp-HV chip (Left) for the amplification side and (right) for the linear regulator side.*

**1.5.1 The Amp-HV chip**

The Amp-HV is a multi-layer double sided, discrete components, that carries out the double work of amplifying the photo-sensor signal while providing and locally regulating the bias voltage to the photo-sensor, significantly reducing the noise loop-area. The two functions are independently in a single layer of the chip, named Amp and HV sides.

The project and the development of the chip have been done at LNF by the SEA electronic department; a detailed description of the system can be found in ref [LNF-Note]. 40 prototypes have been built during 2013 and have been used for the test of the LYSO matrix prototype and for the characterization of the BaF2 crystals. A picture of one prototype is shown in Figure 1.5.3.



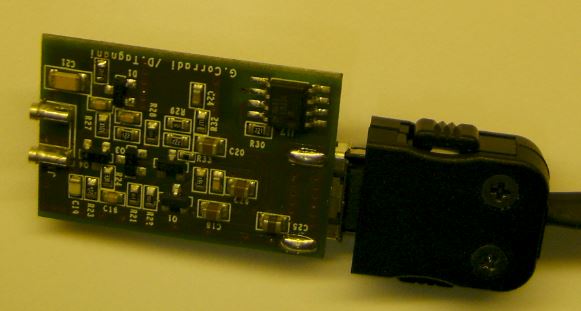


Figure 1.5.3 *Picture of one Amp-HV prototype (Left) amplification (right) HV side.*

**The amplification layer**

The specifications for the amplification layer has been developed and tuned to work with the photo-sensor connected to a LYSO crystal, however minor adjustment to the parameters of the gain and power dissipation, can be carried out in the next production. The scheme is that of a double stage Trans-impedance preamplifier, with a final Trans-impedance gain of 14kΩ (voltage equivalent, Vout/Vin of 300) while keeping a very good equivalent noise charge (ENC) level of about 1000 electrons, without capacitor source. The basic characteristics are described in Table 1, while a sketch of the preamplifier circuit is presented in Figure 1.5.4.

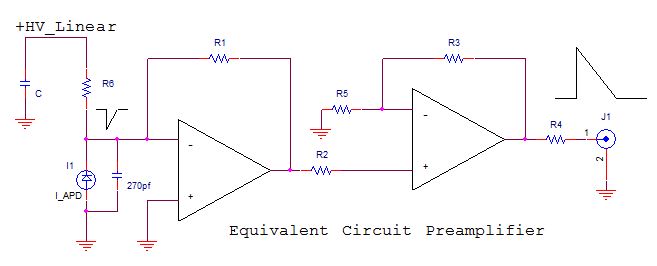


Figure 1.5.4 *Simplified scheme of the Amp-HV amplifier.*

**The linear regulator layer**

The basic requirements for the linear regulator are that of an extreme precision in the regulation (16 bit) voltage and long-Term stability, better than 100 ppm. The current limit on the jersey of the APD, at the moment is conservatively set to about 300 uA; this value will be optimized in a latter stage. In Tab.1.right, the list of measurement characteristics done with the prototype are summarized. In Figure 1.5.5, the basic scheme for the linear regulator is shown. The high voltage required for the APD, is produced by a primary generator in switching technology, with very low noise, residing on the controller board, which generates a voltage of 530 V, a current of 5.5 mA, sufficient to power in parallel 16 channels. The ON and OFF of the channel is controlled by the ARM processor, as described later. The input voltage of 530 V, is followed by a constant current generator, programmable through appropriate adjustment resistors, which provides the current to the next stage in parallel way. This provides a stabilized voltage to the leaders of the APD detector, with local feedback. The output voltage is regulated by a DAC and is then readout again via an ADC, with 16-bit accuracy.

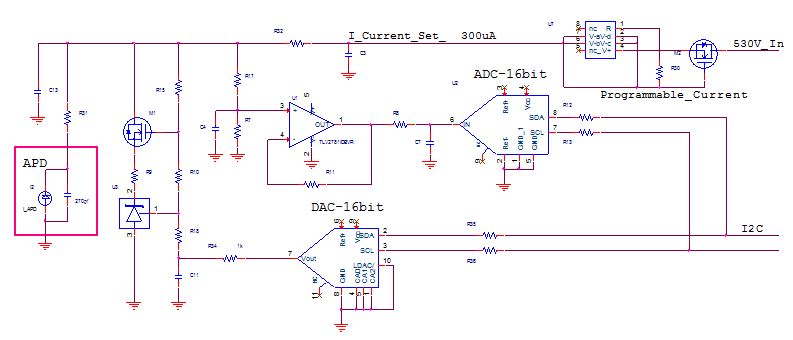


Figure 1.5.5 *Simplified scheme for the Linear Regulator*

**Amp-UV cooling**

At the moment, the issue of integrating the cooling with the mechanics has not been yet fully addressed for the Amp-HV chip but a viable solution is being designed. Since the average power to be dissipated is of ~ 150 mW per channel, the ground can not be connected directly to the shielding surface or to the cold fingers. The usage of a Bridge Resistor Bulk, capable of transferring heat from the Amp-HV chip to the nearby mechanics is foreseen. The bridge resistor will do that with 1 pf coupling leaving to the mechanical support the duty to exchange heat via cold fingers.

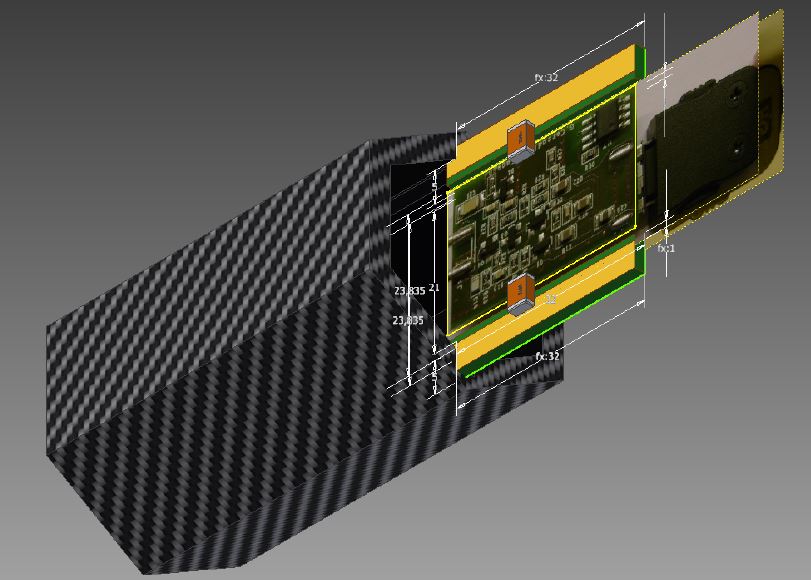


Figure 1.5.6 *CAD drawing of the Amp-HV chip with Bridge resistors inserted inside the brass shielding box.*

In Figure 1.5.6, a first CAD of how this solution can be implemented is shown. In the actual scheme, we foresee to connect at least 16 channels together, and then connect each of them to a single cold finger. Details are being studied together with the mechanical engineering integration, since they must be defined taking into account the operating temperatures and the overall maximum power consumption.

**1.5.2 The ARM controller**

**- Circuit description**

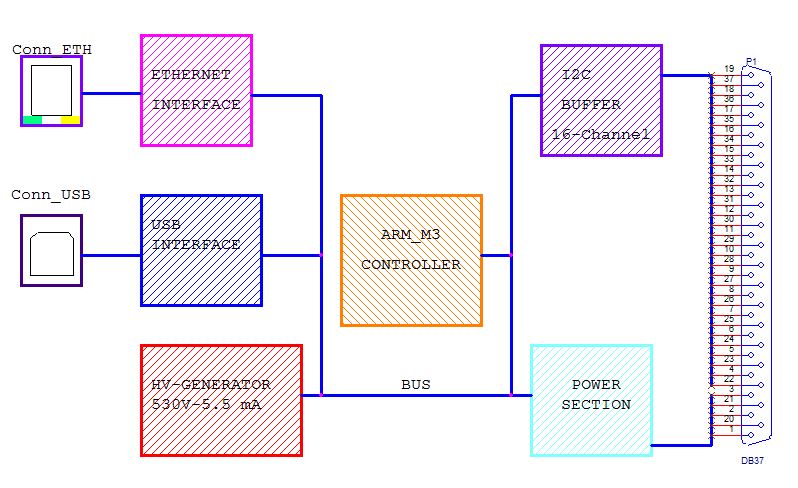


Figure 1.5.7 Design of the M3-ARM controller

The design of the CPU system architecture, consisting of a series of Cortex M3-ARM processor technology, is shown in Figure 1.5.7. The ARM processor is used to control each of the 16 connected Amp-HV cards. The HV-card is used for setting and reading back the APD bias voltage itself after receiving the voltage, HVmax, from the primary generator. The HV-card can regulate the APD bias voltages with a drop of up to 250 V. At the end, it is possible to adjust the bias from HVmax – 250 V, with a 16 bit range. The settings can then be directly read, channel by channel, with a 16-bit ADC .

The primary HV generator is switched ON under CPU control. It is also possible to monitor the primary power supply, which feeds the 6 Volt for the preamplifiers and 12-Volt generator that powers the primary high voltage generator. This is done through a special firmware in the CPU, which requires a standard Ethernet cable connection. The connection of multiple systems is done at the moment via an HUB. In the near future this will be implemented via optical link.

The final version of the controller will collect also the measurement of the temperature of each APD detector and of its Amp-HV card, as well as the CPU temperature. Each Amp-HV chip is connected to the ARM controller through a multiple cable of length varying from 50 to 200 cm. The cables are required for the transport of feeds for low and high voltage, as well as for the signals of the I2C control.

At the moment, the power dissipation of the controller board is about 5 Watt, and requires two powers: +8 V--100 mA (to power all cards Amp-HV, and 12 V--300 mA for the high voltage primary generator. The prototype of the M3-ARM CPU is shown in Figure 1.5.8.

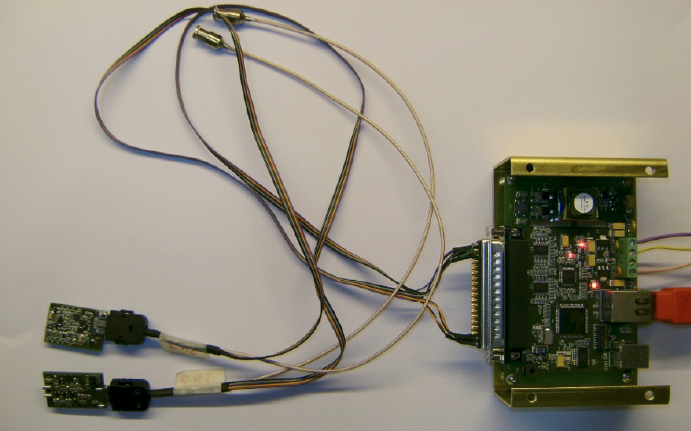
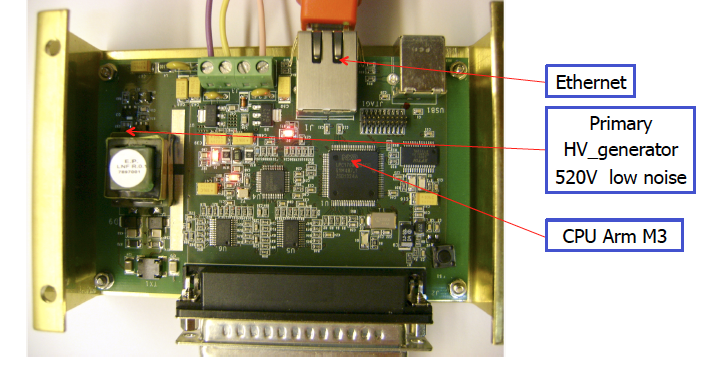


Figure 1.5.8 *(Left) cable connection between ARM controller and Amp\_HV chips, (right) picture of the ARM controller board.*

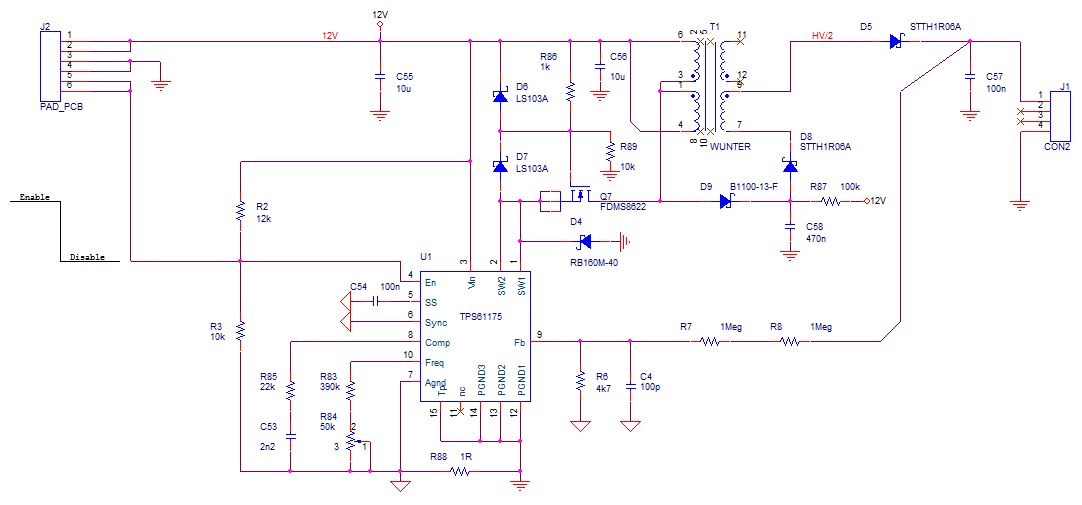
**- HV Generator Circuit Description**

Figure 1.5.9 *Scheme of the HV generator*

The architecture of the switching power is an assembly Bust Fly-back. This configuration allows to get a good power with low-noise output. The circuit diagram of the HV-generator is shown in Figure 1.5.9. The working frequency is about 250 kHz, with excellent stability at long times of about 0.5%, and a peak noise of less 50 mV-pp at maximum load. The performance is better than 85%. The described circuit is used to test the prototypes, but will not work in magnetic field. Two options are being followed: (i) accomplish the same design without using the transformer or (ii) separate the HV generator outside the DS and bring the HV signal by cables through the end-plate feed-throughs. In this latter case, each HV cable will serve 4 boards, i.e. 64 channels.

**1.5.3 Measurement of signal characteristics**

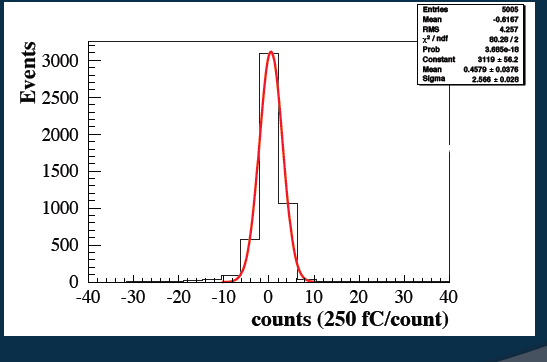
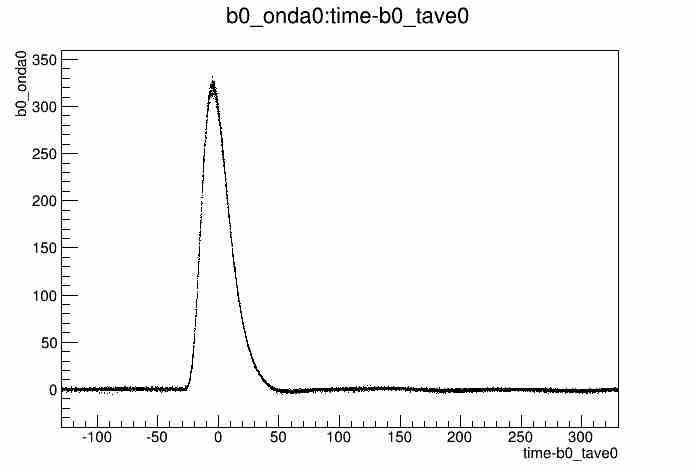
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Figure 1.5. *(Left) Pulse shape for one APD + amplification system fired with a green laser, (right) noise distribution for a Lyso crystal read out by APD+amplifier*

The pre-amplifier has a bandwidth of 70 MHz that corresponds to a signal rise time of 14 ns. To check this with the complete electronic chain, the photo-sensitive APD area is illuminated with a green laser narrow pulse of 2 ns width. The signal output from the pre-amplifier is shown in Figure 1.5.10.left. A rise time of 16 ns has been measured in agreement with expectations.

|  |  |  |
| --- | --- | --- |
| Conditions | Gate width (μsec) | r.m.s. Noise (Counts) |
| LV off | 0,5 or > 1 ec | 1 |
| LV on | 0.5 | 2.2 |
| LV on | 1 | 2.8(HV off), 3.5 (HV on) |
| LV on | 1.5 | 3.6 (HV off), 3.9 (HV on) |

**Gain measurement ???**

Table : *measurement of the amplifier ENC for different running conditions*

The baseline photo-sensor, the large area APD, S8664-1010, has an area of 10x10 mm2 resulting in a high detector capacitance of 270 pF that is the highest source of noise in the apparatus and therefore requires a low-noise amplification stage. To reach a good detection efficiency at the MeV level, the noise performance of the preamplifier is therefore crucial and has to be determined. ENC measurements have been carried out at a bench in different configurations: with everything off, with low voltage on and with/ without the high voltage on. For each configuration the ENC is measured by estimating the RMS of the output distribution. We determined the ENC to be of ~ 1000 e- with a negligible input capacitance while growing almost linearly up to 270 pF. In Table 2, the ENC measurement is shown for different configuration. The one related to the Amplifier itself is that with LV on and HV off which corresponds to ~ 11500 e- for a reasonable integration window.

To confirm such a measurement, we have extracted the ENC from the noise term found when testing, with a Na22 source, a LYSO crystal readout by the S8664-1010 APD followed by the AmpHV chip . The APD gain was set to M=150 and the light yield, LY, has been measured to be ~ 2400 photoelectrons/MeV. In Figure 1.5.10.right the distribution of the noise in count is shown. The RMS is of 2.6 counts, which corresponds to 36 keV after correcting for the Na22 energy peaks. To extract the ENC(e-), the ENC(MeV) has to be multiplied for the LY and for M. We obtained ENC of 13.000 e-. In the BaF2 case, assuming to obtain a LY of 100 pe/MeV this noise level will translate in a noise of ~ 800 keV/channel.

**1.5.3 The Digitizer modules**

**1.5.4 Prototypes of the Digitizer modules**

The Mu2e Calorimeter Waveform Digitizer Prototype Electronics (Cal\_WFD\_Proto) subsystem is the prototype version of an electronic printed circuit board that digitizes analog data from the Calorimeter Front End Electronics, and sends it upstream to the Mu2e Trigger and Data Acquisition (DAQ). Specifically, the Cal\_WFD\_Proto digitizes, serializes, and sends data out of a fiber optic transceiver to the DAQ.

The Cal\_WFD\_Proto is comprised of two subsystems: Data Acquisition and Readout Controller. Data acquisition converts the analog signals to digital, zero-suppresses, adds metadata, and combines the channels into a single block of data. The Readout Controller serializes, translates the data into the correct protocol, and sends the data out the optical transceivers to the DAQ.

Knowledge gained from using the prototype board will be essential to help understand what is needed for the production version. While the production version needs to operate in a difficult environment (high radiation/high magnetic flux), much of the work done on the prototype can be applied to the production board.

**Requirements**

* Create a hardware software development platform that incorporates the Texas Instruments ADS58C48 Analog to Digital Converter (ADC), a Waveform Digitizer (WFD), and a Readout Controller into a single printed circuit board. The Cal\_WFD\_Proto will aid the development of VHDL coding, Slow Controls coding, and an understanding of what is needed to be done to have a functional production WFD and Readout Controller.

**Technical Design**

**Hardware:**

* Figure 1.2.1 shows the block diagram of the Cal\_WFD\_Proto. See figure 1.2.1 at the end of this section. The Cal\_WFD\_Proto is an electronic printed circuit board that measures 25.4 cm wide x 25.4 cm high (10 in wide x 10 in high).
* **Analog Inputs:**
* The Cal\_WFD\_Proto has eight, differentially-ended, analog channels that are digitized. Each channel has two SMA connectors that provide the differentially-ended, analog signal to the board. The analog channels design was based on the Texas Instruments (TI) ADS58C48EVM, Evaluation Module.
* **ADC EVM Connector:**
* A Samtec, high speed ground plane socket is mounted on the bottom side of the Cal\_WFD\_Proto board to allow the TI ADS58C48EVM evaluation module to be used. The ADS58C48 has an additional four channels which also goes to the same Xilinx Spartan-6 FPA as the analog inputs. Using the ADS58C48EVM allows us to compare the signal chain in the analog inputs with this board.
* **External Trigger Input:**
* Digitizing the analog signals coming from the ADC, is started by a differentially-ended, external trigger clock. The external trigger clock is connected to the Cal\_WFD\_Proto using 2 SMA connectors. The first rising edge of the external trigger clock initiates the digitization of analog signals.
* **Optical Transceivers:**
* Optical transceivers on the board take the outputted, serialized data from the FGPA and convert it to an optical signal to be passed up to the Data Acquisition System (DAQ). Two optical transceivers allow for redundancy in the data path to the DAQ. In the event one of the transceivers fails, the other can continue sending data without having to repair or swap out the Cal\_WFD\_Proto board.
* The other role for the optical transceivers is for slow controls communication. Slow controls communication will allow the Cal\_WFD\_Proto board to be configured by the DAQ remotely and be interrogated to monitor system voltages and other environmental issues.
* The optical transceivers are a class 1, multimode, 850nm device. The data rate for the transceivers is 1.25 Gbps up to 2.5 Gbps, using gigabit Ethernet protocol with 8b/10b encoding.
* **Mobile Low Power Dual Data Rate (LPDDR) SDRAM:**
* A Micron, MT46H64M16LFBF, 1Gb, mobile, lpddr, sdram is attached to the FPGA. It can store up to one second of digitized data that can be buffered, if needed, before sent up to the DAQ.
* **Test Points:**
* Test points and a couple of leds are connected to the FPGA. The leds can be used to indicate proper operation or other feedback. The test points help aid debugging the Cal\_WFD\_Proto board.
* **CAN Transceiver Module:**
* The CAN Transceiver module is a redundant communications path for the slow controls in the event that the fiber optics fail or the FPGA programming becomes corrupt. The CAN module is connected to a 16 bit flash based microcontroller that implements the CAN protocol. An external PC or controller communicates with the microcontroller through the CAN Interface.
* **Temperature Sensor:**
* A Texas Instruments LM82 Local Digital Temperature Sensor is attached to the microcontroller via a two-wire serial interface. The temperature sensor measures the board temperature.
* **Microcontroller:**
* A general purpose, 16 bit, flash based, microcontroller is connected to the FPGA. The microprocessor communicates with the FPGA to provide environmental data (Temperature) as well as configuration data (slow controls) through the CAN Interface. The microcontroller uses ANSI C as the programming language. It uses a 10 Mhz discreet crystal as the clock for operation.
* **Field Programmable Gate Array (FPGA):**
* The Xilinx Spartan-6 Field Programmable Gate Array (FPGA) has a few responsibilities:
* Translation, Zero-Suppression, Serializing, and outputting serial data to the optical transceivers.
* Default method for configuring the Cal\_WFD\_Proto board.
* Communicates with microcontroller for environmental data (temperature) and as a secondary path for slow controls.
* The FPGA uses the VHDL programming language to implement the Waveform Digitizer and the Readout Controller. Separate clocks drive various aspects of the FPGA. One clock is used for the gigabit transceivers on the FPGA. Another clock is used for the main system clock. A third clock is provided for redundancy and to allow other parts of the FPGA to be driven from a different clock domain.
* **Clocks:**
* Clocks are generated on the Cal\_WFD\_Proto board. All clocks are differentially-ended and a/c coupled to each device. Four sets of clocks are generated on the board:
* ADC clocks – Clocks that drive the ADCs.
* FPGA Global Clocks –Clocks that drive the FPGA .
* Multi-Gigabit Transceiver (MGT) Clocks – Clocks that drive the MGTs on the FPGA.
* High Speed Clock – Clock to drive other potential high-speed logic in the FPGA.



Figure .2.1 – Block Diagram of Cal\_WFD\_Proto Board.

**Prototype Board Costing:**

There will be five prototype boards made. Each board measures 10 inches wide by 10 inches long (25.4cm wide by 25.4 cm long). Total cost to manufacture the boards (x5), procure components, assemble boards, and debug boards is approximately $25,000, or $5000 per board.

**1.5.5 Conceptual design of final Digitizer modules**