1. **Mu2e Calorimeter Waveform Digitizer Prototype Electronics**

The Mu2e Calorimeter Waveform Digitizer Prototype Electronics (Cal\_WFD\_Proto) subsystem is the prototype version of an electronic printed circuit board that digitizes analog data from the Calorimeter Front End Electronics, and sends it upstream to the Mu2e Trigger and Data Acquisition (DAQ). Specifically, the Cal\_WFD\_Proto digitizes, serializes, and sends data out of a fiber optic transceiver to the DAQ.

The Cal\_WFD\_Proto is comprised of two subsystems: Data Acquisition and Readout Controller. Data acquisition converts the analog signals to digital, zero-suppresses, adds metadata, and combines the channels into a single block of data. The Readout Controller serializes, translates the data into the correct protocol, and sends the data out the optical transceivers to the DAQ.

Knowledge gained from using the prototype board will be essential to help understand what is needed for the production version. While the production version needs to operate in a difficult environment (high radiation/high magnetic flux), much of the work done on the prototype can be applied to the production board.

* 1. **Requirements**

Create a hardware software development platform that incorporates the Texas Instruments ADS58C48 Analog to Digital Converter (ADC), a Waveform Digitizer (WFD), and a Readout Controller into a single printed circuit board. The Cal\_WFD\_Proto will aid the development of VHDL coding, Slow Controls coding, and an understanding of what is needed to be done to have a functional production WFD and Readout Controller.

* 1. **Technical Design**
     1. **Hardware:**

Figure 1.2.1 shows the block diagram of the Cal\_WFD\_Proto. See figure 1.2.1 at the end of this section. The Cal\_WFD\_Proto is an electronic printed circuit board that measures 25.4 cm wide x 25.4 cm high (10 in wide x 10 in high).

**Analog Inputs:**

The Cal\_WFD\_Proto has eight, differentially-ended, analog channels that are digitized. Each channel has two SMA connectors that provide the differentially-ended, analog signal to the board. The analog channels design was based on the Texas Instruments (TI) ADS58C48EVM, Evaluation Module.

**ADC EVM Connector:**

A Samtec, high speed ground plane socket is mounted on the bottom side of the Cal\_WFD\_Proto board to allow the TI ADS58C48EVM evaluation module to be used. The ADS58C48 has an additional four channels which also goes to the same Xilinx Spartan-6 FPA as the analog inputs. Using the ADS58C48EVM allows us to compare the signal chain in the analog inputs with this board.

**External Trigger Input:**

Digitizing the analog signals coming from the ADC, is started by a differentially-ended, external trigger clock. The external trigger clock is connected to the Cal\_WFD\_Proto using 2 SMA connectors. The first rising edge of the external trigger clock initiates the digitization of analog signals.

**Optical Transceivers:**

Optical transceivers on the board take the outputted, serialized data from the FGPA and convert it to an optical signal to be passed up to the Data Acquisition System (DAQ). Two optical transceivers allow for redundancy in the data path to the DAQ. In the event one of the transceivers fails, the other can continue sending data without having to repair or swap out the Cal\_WFD\_Proto board.

The other role for the optical transceivers is for slow controls communication. Slow controls communication will allow the Cal\_WFD\_Proto board to be configured by the DAQ remotely and be interrogated to monitor system voltages and other environmental issues.

The optical transceivers are a class 1, multimode, 850nm device. The data rate for the transceivers is 1.25 Gbps up to 2.5 Gbps, using gigabit Ethernet protocol with 8b/10b encoding.

**Mobile Low Power Dual Data Rate (LPDDR) SDRAM:**

A Micron, MT46H64M16LFBF, 1Gb, mobile, lpddr, sdram is attached to the FPGA. It can store up to one second of digitized data that can be buffered, if needed, before sent up to the DAQ.

**Test Points:**

Test points and a couple of leds are connected to the FPGA. The leds can be used to indicate proper operation or other feedback. The test points help aid debugging the Cal\_WFD\_Proto board.

**CAN Transceiver Module:**

The CAN Transceiver module is a redundant communications path for the slow controls in the event that the fiber optics fail or the FPGA programming becomes corrupt. The CAN module is connected to a 16 bit flash based microcontroller that implements the CAN protocol. An external PC or controller communicates with the microcontroller through the CAN Interface.

**Temperature Sensor:**

A Texas Instruments LM82 Local Digital Temperature Sensor is attached to the microcontroller via a two-wire serial interface. The temperature sensor measures the board temperature.

**Microcontroller:**

A general purpose, 16 bit, flash based, microcontroller is connected to the FPGA. The microprocessor communicates with the FPGA to provide environmental data (Temperature) as well as configuration data (slow controls) through the CAN Interface. The microcontroller uses ANSI C as the programming language. It uses a 10 Mhz discreet crystal as the clock for operation.

**Field Programmable Gate Array (FPGA):**

The Xilinx Spartan-6 Field Programmable Gate Array (FPGA) has a few responsibilities:

* Translation, Zero-Suppression, Serializing, and outputting serial data to the optical transceivers.
* Default method for configuring the Cal\_WFD\_Proto board.
* Communicates with microcontroller for environmental data (temperature) and as a secondary path for slow controls.

The FPGA uses the VHDL programming language to implement the Waveform Digitizer and the Readout Controller. Separate clocks drive various aspects of the FPGA. One clock is used for the gigabit transceivers on the FPGA. Another clock is used for the main system clock. A third clock is provided for redundancy and to allow other parts of the FPGA to be driven from a different clock domain.

**Clocks:**

Clocks are generated on the Cal\_WFD\_Proto board. All clocks are differentially-ended and a/c coupled to each device. Four sets of clocks are generated on the board:

* ADC clocks – Clocks that drive the ADCs.
* FPGA Global Clocks –Clocks that drive the FPGA .
* Multi-Gigabit Transceiver (MGT) Clocks – Clocks that drive the MGTs on the FPGA.
* High Speed Clock – Clock to drive other potential high-speed logic in the FPGA.



Figure .2.1 – Block Diagram of Cal\_WFD\_Proto Board.

* 1. **Prototype Board Costing:**

There will be five prototype boards made. Each board measures 10 inches wide by 10 inches long (25.4cm wide by 25.4 cm long). Total cost to manufacture the boards (x5), procure components, assemble boards, and debug boards is approximately $25,000, or $5000 per board.