FAST NATIONAL UNIVERSITY
School of Computing
Fall 2022

Course Title:	Computer Organization and Assembly Language
Task:	Quiz 5
Section:	BCS-3B
Date:	30th Nov, 2022

Q1 (2 Points): Find at least 3 data hazards in following pipelined instructions. Each stage takes only 1 cycle.

Assembly code in MIPS Architecture	
Pipeline Stages	FI, DI , EX, Mem , WB
Instruction 1:	load R2, 0(R1)
Instruction 2:	load R4, 0(R2)
Instruction 3:	add R2, R4, R3

Use following method to write hazard between two instructions.
For Example: Instruction X & Instruction Y on register Z, Instruction X & Instruction Z on register A

RAW: I2 & I3 on R4
WAR: I2 & I3 on R2
WAW:I1 & I3 on R2

Q2 (2 Points): Add stall cycles in given table to remove the hazards from instructions given in **Q1**.

	Clock Cycle																			
Instruction no	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

Q3 (2 Points): Find the corresponding address in RAM if Index, tag and offset number is given for differently mapped caches. Show calculations. Index and Tags are given in hex.

- Fully Associative Mapped Cache
  Index= 10 Tag= 4095
  Address in RAM?

  Tag 100 0000 1001 0101
  Index 0001 0000
  Physical Address: 100 0000 1001 0101 0001 0000 (Assuming the size of index is 8 bits)