EECE 444

Lab 7

VGA Controller Design

Introduction

In this lab you will design a VGA controller to output graphics to a monitor connected to the Nexys 4DDR board.

A VGA monitor operates using an electron beam that scans the screen row by row, starting at the upper left corner and ending at the lower-right corner. This beam moves using two synchronization signals: the horizontal sync HS (*hsync*) and the vertical synch VS (*vsync*). The *hsync* signal tells the beam when to move to the next row, and the *hsync* tells the beam when to move back to the top of the screen. To display a picture on the screen the VGA controller needs to generate the two synchronization signals, *hsync* and *vsync*, and provide the color signal (Red, Green, and Blue). A VGA monitor works on the basis of emitting energy in the red, green, and blue spectrum proportional to the voltage on the corresponding R, G, or B signal input to the screen. Each colored dot on the screen is called a pixel (short of picture element). The screen starts displaying pixels from the top left corner of the screen moving toward the right and transitions, line-by-line in a direction moving towards the bottom of the screen. The horizontal sync signal *hsync* synchronizes each new line. Once it reaches the bottom of the screen, the vertical sync signal *vsync* causes it to start over again from the top left corner. To display a picture on the screen, we simply generate these synchronization signals and provide the pixel color to display on the screen. The VGA system signals in shown in figure 1.

In this lab, you are going to create a 640 x 480 pixel screen display using a 25 MHz pixel clock.

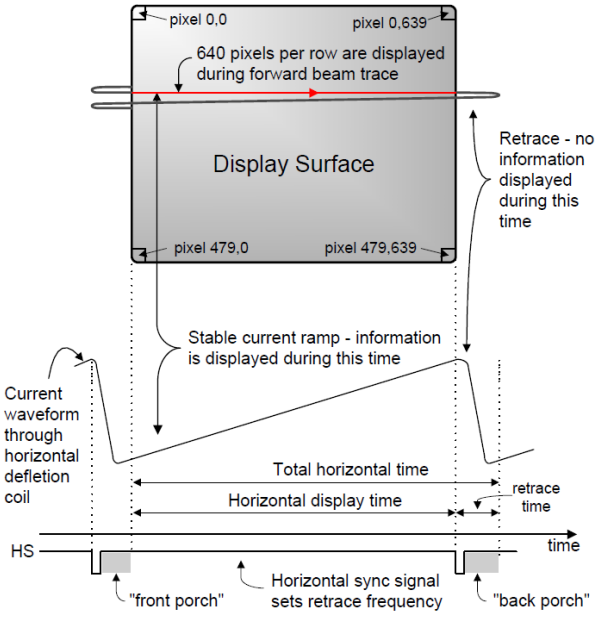


Figure 1: VGA system display

Please read and follow the instructions in this lab carefully.

1. VGA port

The VGA port has 5 active signals, the horizontal and vertical synchronization ***hsync*** and ***vsync***, and three video signals for the ***red***, ***green*** and ***blue*** beams. A video signal is an analog signal and the video controller uses a DAC to convert the digital output to the desired analog level. The Nexys 4DDR boards use a simple 4-resistor circuit to convert a 4-bit red signal to a 16-level analog signal. It uses a similar circuit to convert 4-bit of red and 4-bit of blue to corresponding analog signals. Thus the Nexys 4DDR boards support 12-bit VGA color (4 red, 4 green and 4 blue). This will produce 4096 (2^{12}) different colors.

2. Video Controller

A video controller generates the synchronization signals and outputs data pixels serially. Figure 2 shows a block diagram of a VGA controller.

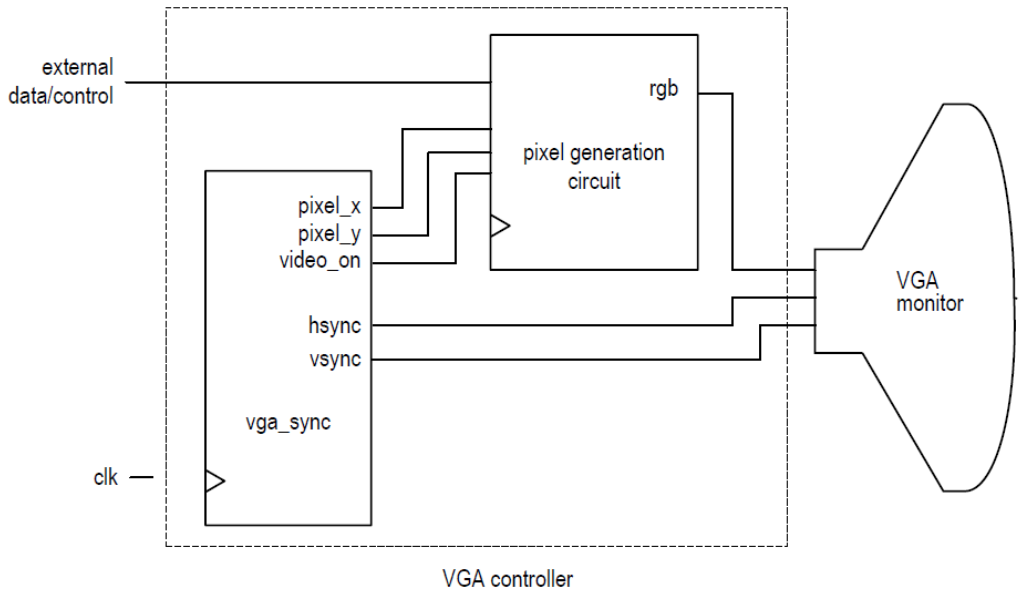


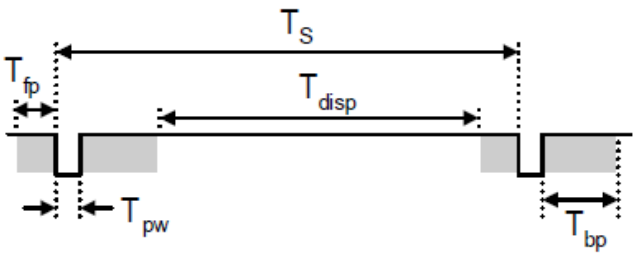
Figure 2

The controller contains two circuits: the synchronization circuit vga_sync and a pixel generation circuit.

I. VGA Synchronization

The video synchronization circuit generates the hsync, vsync, video_on, pixel_x, and pixel_y. The circuit will have two inputs: clk inpt and clr clear signal.

1. ***hsync:*** the hsync signal specifies the required time to scan a row. A timing diagram of one horizontal scan is shown in Figure 3.



Symbol	Parameter	Vertical Sync			Horiz. Sync	
		Time	Clocks	Lines	Time	Clks
T_S	Sync pulse	16.7ms	416,800	521	32 us	800
T_{disp}	Display time	15.36ms	384,000	480	25.6 us	640
T_{pw}	Pulse width	64 us	1,600	2	3.84 us	96
T_{fp}	Front porch	320 us	8,000	10	640 ns	16
T_{bp}	Back porch	928 us	23,200	29	1.92 us	48

Figure 3

A period of the hsync signal contains 800 pixels (Ts in figure 3) and is divided into 4 regions:

- Display (640 pixels, Tdisp in Figure 3): region where the pixels are actually displayed on the screen. The video signal should be enabled.
- Retrace or pulse width (96 pixels, Tpw in Figure 3): region in which the electron beams return to the left edge. The video signal should be disabled.
- Right border or Front Porch (16 pixels, Tfp in Figure 3): region forms the right border. The video signal should be disabled.
- Left border or Back Porch (48 pixels, Tbp in Figure 3): region forms the left border. The video signal should be disabled.

You can obtain the hsync signal by generating a mod-800 counter.

2. ***vsync:*** during vertical scan, the beam move gradually from top to bottom and then return to the top. The format of the vsync signal is shown in Figure 3.

A period of the vsync signal is 521 lines (Ts in Figure 3) and is divided into four regions:

- Display (480 lines, T_{disp} in figure 3): region where the horizontal lines are actually displayed on the screen.
- Retrace or pulse width (2 lines, T_{pw} in figure 3): regions where the beams return to the top of the screen. The video signal should be disabled.
- Bottom border or Front Porch (10 lines, T_{fp} in figure 3): regions that form the bottom border of the display region. The video signal should be disabled.

- Top border or Back Porch (33 lines, T_{bp} in figure 3): regions that form the top border. Video should be disabled.

The vsync signal can be obtained by creating a mod-525 counter.

3. ***video_on:*** this signal is asserted when in the 640x480 region
4. ***pixel_x*:** this output can be constituted using the mod-800 counter.
5. ***pixel_y*:** this output can be constituted using the mod-521 counter.

II. Timing Calculation of VGA synchronization signals.

To achieve a 60Hz refresh rate, a pixel rate of 25 MHz. The pixel rate is determined using three parameters: the number of pixels in a horizontal scan line *p*, the number of lines in a screen *l*, and the number of screens per second *s*.

- *p* = 800 pixels/line
- *l = 525 lines/screen*
- *s = 60 screens/second*

*pixel rate = p * l * s = 25 M pixels/second*

III. Pixel Generation Circuit

The pixel generation circuit generates the 12-bit rgb signal (4 bits red, 4 bits green and 4 bits blue) for the VGA port. The pixel_x and pixel_y signals provide the current coordinate of the pixel. When the pixel is in the visible region, output the pixel color value rgb, otherwise when in the blanking region, output rgb=12'h000. You may use the video on signal to determine the area of display. There is an additional 3-bit switch input (the external data/control in figure 2), that will specify the color displayed on the screen. Refer to table 1 for the selected colors.

Table 1

Switch Input	Color on VGA display
0	Black
1	Blue
2	Green
3	Cyan
4	Red
5	Magenta
6	Yellow
7	White
none	Black

Procedure:

- Use 2 counters to store the values of pixel_x and pixel_y
- Generate a 25 MHz pixel clock by dividing the 100 MHz FPGA clock
- On the rising edge of the pixel clock, increment the pixel_x count. Increment the pixel_y count when the pixel_x count reaches the end of the row.
- Generate the hsync signal based on the value of the pixel_x count as illustrated in figure 3.
- Generate the vsync signal based on the value of the pixel_y count as illustrated in figure 3.
- Generate the video_on signal to indicate if the pixel is in the visible region.
- When in the visible region, output the pixel color value rgb, otherwise output 0.
- Put all of the outputs {rgb, hsync, vsync} thru flip-flops to ensure no combinational logic delay will interfere with the output display.
- Refer to table 1 to specify the displayed colors according to the switches input.
- To generate different color, you can refer to the 12-bit VGA color codes where each R, G and B is encoded in 12 bits.
- Create a top module to connect the two circuits. You will need to download and test this circuit on your FPGA. Refer to the board for the hsync, vsync and rgb pin numbers.

What to Turn In

Include the following elements **in the following order** in your final submission. Clearly label each part by number. Poorly organized submissions will lose points.

1. **Please indicate how many hours you spent on this lab.** This will not affect your grade but will be helpful for calibrating the workload for next semester's labs.
2. Verilog code of the Pixel generation circuit and the synchronization circuit.
3. Snapshot of the VGA screen displaying one of the outputs.
4. You need to demonstrate this lab to your TA for full credit.
5. For extra credit store a picture on the RAM and display it.