**EECE 343 Computer Interface Circuits**

**Lab 4**

**Counter and Slow Clock**

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**Objectives**

The purpose of this exercise is to learn how to design an 8-bit Counter and connect simple input and output devices to an FPGA chip and implement a circuit that uses these devices. We will use the switches SW9-0 on the DE2 board as inputs to the circuit, and outputs to Seven Segment Display.

**Project**

# Please design an 8-bit Counter with VHDL programming and implement the design with the DE 2 board.

# The minimum requirements of the Counter are

# operated at 4HZ or slower,

# displayed by 8 LEDs and 2 Seven-Segment Displays,

# counted up or down,

# loaded an 8-bit data with a control pin. Bonus points will be awarded if designed counter displays some special functions and/or patterns.

**Procedure**

Perform the following steps to implement a circuit for the project on the DE2 board.

1. Create a new Quartus II project for your circuit. If using the Altera DE2 board, select Cyclone II EP2C35F672C6 as the target chip, which is its FPGA chip.
2. Create a VHDL entity for the code of the lab project.
3. Include in your project the required pin assignments for the DE2-series board, as discussed above. Compile the project.
4. Download the compiled circuit into the FPGA chip. Test the functionality of the circuit.
5. Turn in your lab report on the day you demonstrate your project in class.