**EECE 343 Computer Interface Circuits**

**Lab 2**

**Seven Segment Display**

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**Objective**

The purpose of this exercise is to learn how to connect simple input and output devices to an FPGA chip and implement a circuit that uses these devices. We will use the switches SW17-0 on the DE2 board as inputs to the circuit. We will use Seven Segment Display.

**Project**

Design a seven segment decoder module that has the three-bit input c2c1c0. This decoder produces seven outputs that are used to display a character on a seven segment display. Develop a table that lists the characters that should be displayed for each valuation of c2c1c0. To keep the design simple, only four characters are included in the table (plus the ‘blank’ character, which is selected for codes 100 - 111).

You are to write a VHDL entity that implements logic functions that represent circuits needed to activate each of the seven segments. Use only simple VHDL assignment statements in your code to specify each logic function using a Boolean expression.

**Procedure**

Perform the following steps to implement a circuit for the project on the DE2 board.

1. Create a new Quartus II project for your circuit. If using the Altera DE2 board, select Cyclone II EP2C35F672C6 as the target chip, which is its FPGA chip.
2. Create a VHDL entity for the code of the lab project.
3. Include in your project the required pin assignments for the DE2-series board, as discussed above. Compile the project.
4. Download the compiled circuit into the FPGA chip. Test the functionality of the circuit.
5. Turn in your lab report on the day you demonstrate your project in class.