**EECE 343 Computer Interface Circuits**

**Lab 3**

**8-Bit Adder and Seven Segment Display**

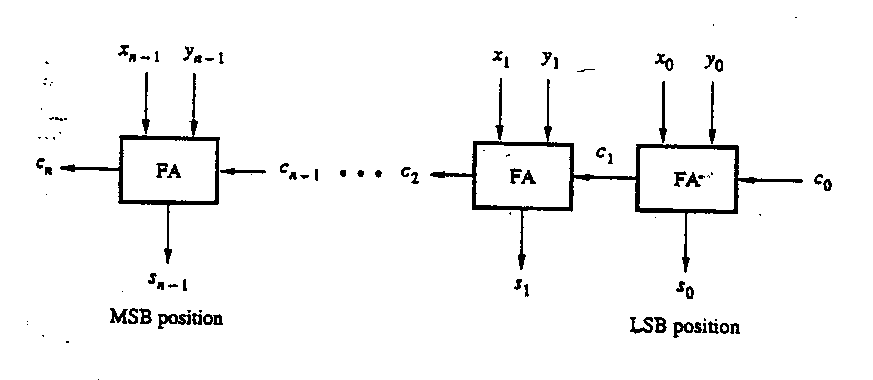
Dr. Hede Ma

**Objectives**

The purpose of this exercise is to learn how to design an 8-bit Adder and connect simple input and output devices to an FPGA chip and implement a circuit that uses these devices. We will use the switches SW16-0 on the DE2 board as inputs to the circuit. We will use Seven Segment Display.

**Project**

Please write a VHDL program for the 8-bit adder with a structural description. Simulate the design and finally implement the circuit with the DE 2 board.Demonstrate your designs with LEDs and Seven Segment Display.



**Procedure**

Perform the following steps to implement a circuit for the project on the DE2 board.

1. Create a new Quartus II project for your circuit. If using the Altera DE2 board, select Cyclone II EP2C35F672C6 as the target chip, which is its FPGA chip.
2. Create a VHDL entity for the code of the lab project.
3. Include in your project the required pin assignments for the DE2-series board, as discussed above. Compile the project.
4. Download the compiled circuit into the FPGA chip. Test the functionality of the circuit.
5. Turn in your lab report on the day you demonstrate your project in class.